OPERATING AND SERVICE MANUAL

HEWLETT-PACKARD

8116A PROGRAMMABLE PULSE/FUNCTION GENERATOR 50 MHz

(Including Option 001)

SERIAL NUMBERS

This manual applies directly to instrument with serial number **2334G02896** and higher. Any changes made in instruments having serial numbers higher than the above number will be found in a "Manual Changes" supplement supplied with this manual. Be sure to examine this supplement for any changes which apply to your instrument and record these changes in the manual. Backdating information for instruments with lower serial numbers can be found in Section 7 (yellow pages).

HERRENBERGER STR. 110, D-7030 BÖBLINGEN
FEDERAL REPUBLIC OF GERMANY

MANUAL PART NO. 08116–90002
MICROFICHE PART NO. 08116–95002

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HEWLETT PACKARD

MANUAL CHANGES

Manual for Model Number	8116A
Manual printed on	June 1984
Manual Part Number	08116-90002

Make all ERRATA corrections.

Check the following table for your instrument serial prefix/serial number and make the listed changes to your manual.

▶ New Item

Serial Prefix or Serial Number		Manual Changes
ERRATA		
2332G03121	and above	1
2334G03171	and above	1-2
2334G03221	and above	1-3
2334G03223	and above	1-4
2334G03396	and above	1-5
2334G03546	and above	1-6
2334G03571	and above	1-7
2334G03696	and above	1-8
2510G03746	and above	1-9
2520G03921	and above	1-10
2520G04046	and above	1-11
2520G04121	and above	1-12
2520G04390	and above	1-13
see Note Page 12!		
2520G04421	and above	1-14
2520G04446	and above	1-15
2520G04621	and above	1-16
2520G04796	and above	1-17
2632G05071	and above	1-18
2632G05096	and above	1-19
2632G05171	and above	1-20
2632G05196	and above	1-21
2632G05421	and above	1-22
2632G05446	and above	1-23
2632G05471	and above	1-24

Januar 1987

MODEL 8116A

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MANUAL CHANGE	MISCELLANEOUS	FRAME	A1	A2	A3	A4	A5	A6
ERRATA	Page 8-16 Page1-4,4-3,4-4 4-14,4-18 4-19,4-21	C230*,R220* R223*,R406 R408			R16,W2			
1	Page 8-16		C409*,CR401,402 R454					
2			R219*, 222*					
3	Page 8-16		C305,306,307, Cr303,304 R310,311,U300					
4	Page 8-16, 8-18		Q210,216,R202,215 R273,274,275,276, R277					
5			Q401					
6	Page 8-8/9				R21 U10,11,39			
7	Page 6-9		R400*,436*					

MODEL 811C

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MANUAL CHANGE	MISCELLANEOUS	FRAME	A1	A2	A3	A4	A5	A6
8			C100,101,103,106, C108,152,153,212, C214,215,220,224, C231,241,260,261, C263,301,302,403, C405,408,512 thru C518,526,533 thru C537,550,523,524	C5,17,18 C19,23,26 C29	C3,4,5,9 C11 thru C28,30,31 C32,33,34 C36			
9	MP4,7,8, MP12,13,17,18							
10	Page 8-9	F1			A3 W5			
11			*R242					
12	Page 8-18		C406,409,410,540					
13	Page 6-10,11			K1,2,3,4 CR1,2,3,4 R68, CR20				
14	Page 6-7 Page 6-10	*L502 R558						
15	Page 6-8	*R220						

MODEL 8116A

INDEX OF MANUAL CHANGES

MANUAL CHANGE	Miscellaneous	FRAME	A1	A2	A3	A4	A5	A6
16	Table 6-3.		K201,202, K501-506, CR 513,514 *C409, *C502 R19,24 CR 515,516 VR 504-507 W 12,13,14 C551,552,553 *L 506,507 CR 201,202, CR 507-512, R20 R21 *C409 *R558 R593,594*C554					
17	Table 6-3.		*C409, C539, *C502, *C555 C553					
18	Page 8-9		MP501		CR5, Q1, R 22,23			
19	Page 6-7		L260,261					
20	Page 6-3		J2		J1,2			
21		MP8	*C300, *R309					
22	Page 6-9		*R423,*R427 R436 , R226					
23	Table 6-3		*C525,*R423, *R427					
24	Table 6-3	MP8						

SERVICE BLOCK 6

VCO, WIDTH GENERATOR THEORY OF OPERATION

General

The bulk of the Slope Generation and Timing circuitry is to be found on the Main Board A1 Assy. A small part is also located on Control Board A2 Assy.

The Overall operation may be generally divided into the following functions:

1. Trigger Input Circuits
2. Control Input Circuits
3. Slope Generator IC
4. Timing IC
5. Error Feedback and Vernier Feedback

1. Trigger Input Functions

There are three distinct trigger input functions.

The first stage (Trigger Level Circuit) receives both the trigger input and trigger level adjust directly from the instrument frontpanel, and is designed to provide the required trigger level to the second stage without imposing it on the trigger input signal (thereby not disrupting the trigger source). Figure 8–6–1 shows the principle of operation of the circuit. Op-Amp U101A is configured to provide a fixed voltage source of –1.25V, and U101B is an inverting amplifier of unity gain used to provide a voltage of equal magnitude but opposite polarity to the level selected.

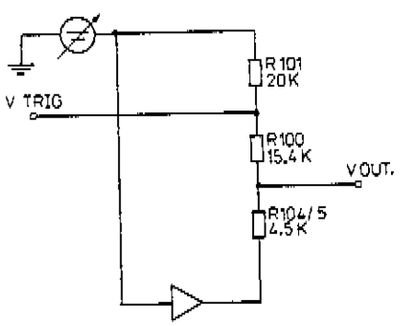


Figure 8–6–1. Trigger input circuit simplified

By varying the voltage across the divider chain, the DC component (or DC shift) of Vout will change accordingly. Vout is now passed through high-to-low impedance converter Q100/Q101 and on to the second trigger output function. The trigger input amplifier is a three-stage ECL circuit with Schmitt trigger characteristics. Each operational amplifier stage has a main and complementary output – both of which are pulled down to –5.2 V via a 470 Ohm resistor. The circuit feedback resistor (R113) provides a hysteresis path to the input in order to overcome any noise which may be present. The threshold of this Schmitt Trigger circuit is fixed at –1.3 V. The third trigger input function is a wired-OR configuration for trigger slope/MAN selection. INT BURST or MAN selection at the frontpanel results in the Trigger Mode Latch U103 outputting a TTL high to one of four ECL NOR gates via the TTL/ECL converter R116/R117/R118. In the wired-OR configuration, a logic high prevails (logic low is, in fact, a high impedance output stage). Auto Vernier FF U203 is clocked by this high-going signal, eventually providing an Auto Vernier Feedback signal, after having been reset as a result of Auto Vernier selection at the frontpanel.

2. Control Input Circuits

The control input signal from the instrument frontpanel is routed to the Main Board A1 Assy. The circuit input has voltage protection diodes CR151 and CR152 to clamp incoming levels outside the ± 15 V window. Operational amplifier U151 is configured as a unity-gain, non-inverting buffer – the output being limited within a –5.2 V to +5 V window – which provides the input to the Control Mode Selector U152. Frequency and Amplitude Modulation, Pulse Width Modulation and Voltage controlled oscillator modes are selected via logic signals M1 and M2 at U152. For FM mode, the control signal is output from U152 pin 14. VCO mode control signal is output at pin 12, and PWM control signal at pin 4 (via pin 11). When AM has been selected, U152 pin 13 becomes earthed via pin 15, and U151 output is processed by the Amplitude modulator. See Service Block 7.

ERRATA

Page 6-6/6-15, change the Table of Replaceable Parts to read :

A1C230*	0160-4386	C-FXD 33PF 5% 200V
A1R220*,223*	0698-3152	R-FXD 3.48K 1%
A1R406	0757-0421	R-FXD 825 1% .125W
A1R408	0698-4447	R-FXD 280 1% .125W
A3R16	1810-0280	R-NETWORK 9x10K
A3W2	8159-0005	JUMPER
Opt.001: A2R30	0698-3152	R-FXD 3.48K 1%
A2R33	0757-0458	R-FXD 51.1K 1%
A2R43	2100-3252	R-VAR 5K 10%

Delete: A2C31

Page 8-16, Service Sheet 6 :

The value of R220*, R223* should read 3.48K.

Page 1-4,

change the description for the Pulse width ranges in PWM CONTROL MODE to read:

Pulse width ranges: eight decade ranges from 10ns to 1s

Page 4-3, change step 7 to read:

Set sampling scope such that one cycle fills the display. Verify that width is (= 10ns.

Page 4-4, change step 3 to read:

Use Figure 4-1 test setup and set counter to TOT A and MANUAL GATE mode. Reset the counter and enable the GATE.

Page 4-14, change the description for the Pulse width ranges in paragraph 4-19 to read:

Pulse width ranges: eight decade ranges from 10ns to 1s.

Page 4-18,

delete the Pulse Generator from Figure 4-17 and from the list of test equipment.

Page 4-19, change step 8 (OPT 001 only) to read:

Press the 1 CYCLE key on the 8116A frontpanel. Confirm that the counter reading increments by one step. (124)

Page 4-21,

delete the Min.Result (7.5ns) in paragraph 4-11 (Pulse width) of the Performance Test Record for the 8ns setting.

ERRATA (Cont.)

On Page 4-19, step 6. change to read:

HIL.....4.0V LOL 0.0V

On Page 4-19, step 9. change to read:

Select the HIL parameter on the 8116A.....

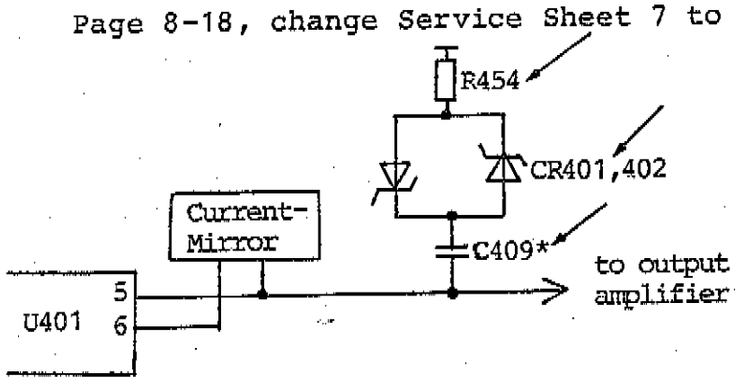
Similarly, when LOL is selected, ...

MANUAL CHANGE 1

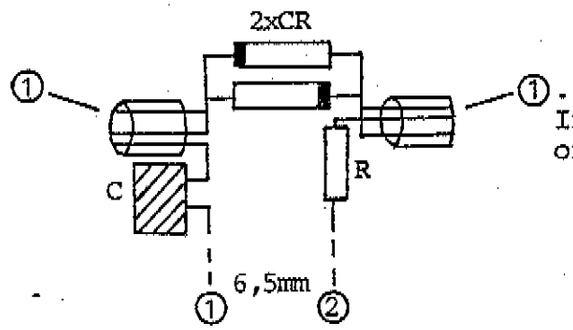
Page 6-6/6-7/6-9, Replaceable Parts List :

Add:	A1C409*	0160-3875	C-FXD 22PF 5% 200V
	A1CR401,402	1901-0518	DIODE SCHOTTKY SM SIG
	A1R454	0757-0276	R-FXD 61,9 1% .125W

Page 8-18, change Service Sheet 7 to read :



The clamp should be wired and soldered as shown below :



①...Eyelet funnel flange
Install the clamp as shown
on the Component Locator !

On Component Locator the C409, CR401,402 and R454 are located between C402 and Q402.

In Ref.Des. Table and Grid Location add as follows :

C409
CR401,402
R454
} LM - 5/6

MANUAL CHANGE 2

Page 6-8, change the Table of Replaceable Parts to read :

A1R219*,222*	0757-0442	R-FXD 10K 1% .125W

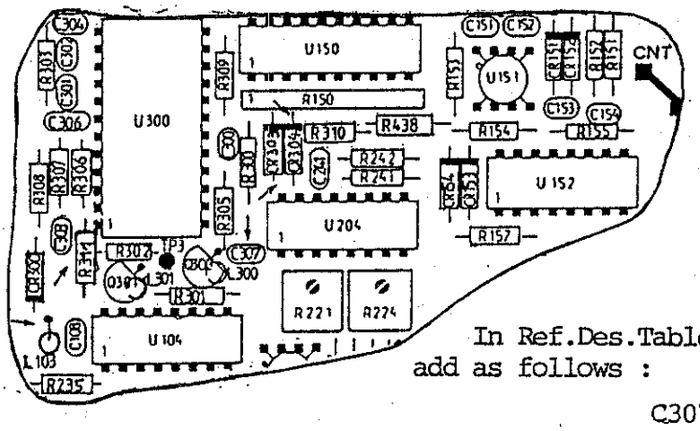
MANUAL CHANGE 3

Page 6-6/-7/-9/-10, change the Table of Replaceable Parts to read :

A1C306	0160-0575	C-FXD .047 20% 50 VDC
A1R310	0698-3441	R-FXD 215 1% .125W F
A1U300	1826-0984	IC-TIMING
Add: A1C307	0160-0575	C-FXD .047 20% 50 VDC
A1CR303,304	1901-1068	DIODE-SCHOTTKY SM
A1R311	0698-3160	R-FXD 31.6 KOHM 1% .125W

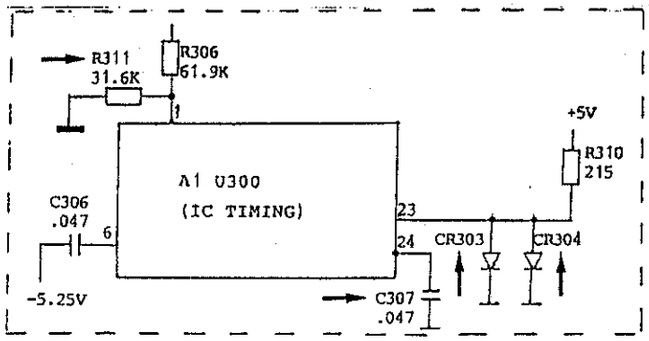
Delete: A1C305

On Page 8-16, Service Sheet 6, change the Component Locator and Diagram of A1 to read :



In Ref.Des.Table and Grid Location add as follows :

	C307	J4
	CR303	J/K 3/4
	CR304	
A1	R311	I4
Delete:	C305	J4

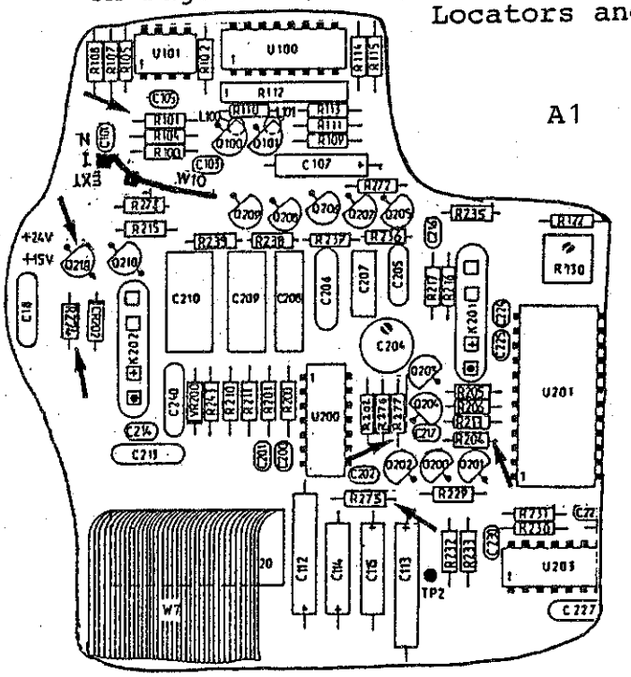


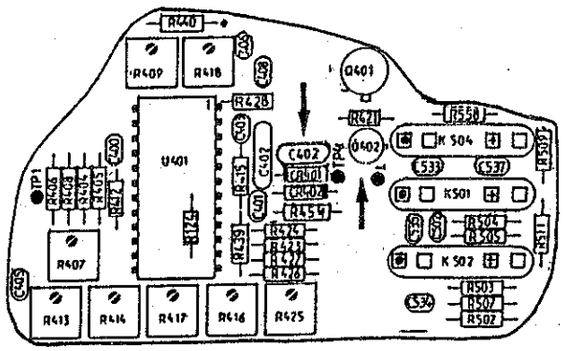
MANUAL CHANGE 4

On Page 6-7/-8/-9, change the Table of Replaceable Parts to read

	A1Q210	1854-0215	TRANSISTOR SI 2N3904
	A1R202,215	0757-0419	R-FXD 681 1% .125W
Add:	A1Q216	1853-0036	TRANSISTOR SI 2N3906
	A1R273	0757-0280	R-FXD 1K 1% .125W
	A1R274	0757-0407	R-FXD 200 1% .125W
	A1R275	0698-4416	R-FXD 169 1% .125W
	A1R276,277	0757-0419	R-FXD 681 1% .125W

On Page 8-16/8-18, Service Sheet 6/7, change the Component Locators and Diagram of A1 to read :



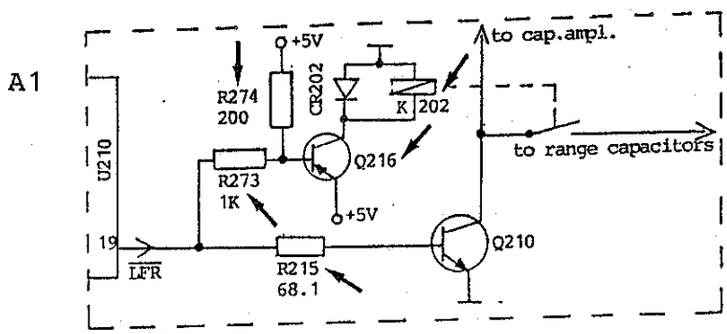


Page 8-18. In Ref.Des.Table and Grid Location add as follows :

C402 CR401 CR402 R454	L6

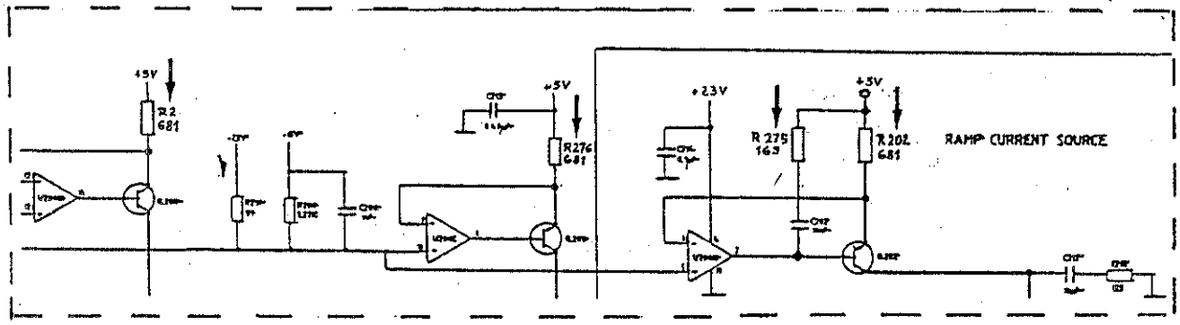
Page 8-16. In Ref.Des.Table and Grid Location add as follows :

Q216		R275	H4
R273	G5	R276	H/16
R274		R277	



MANUAL CHANGE 4 (Cont.)

On Page 8-16, Service Sheet 6, change the Diagram of A1 to read :



MANUAL CHANGE 5

Page 6-7, change the Table of Replaceable Parts to read:

	A1Q401	1853-0589	Trans Dual MD 4260

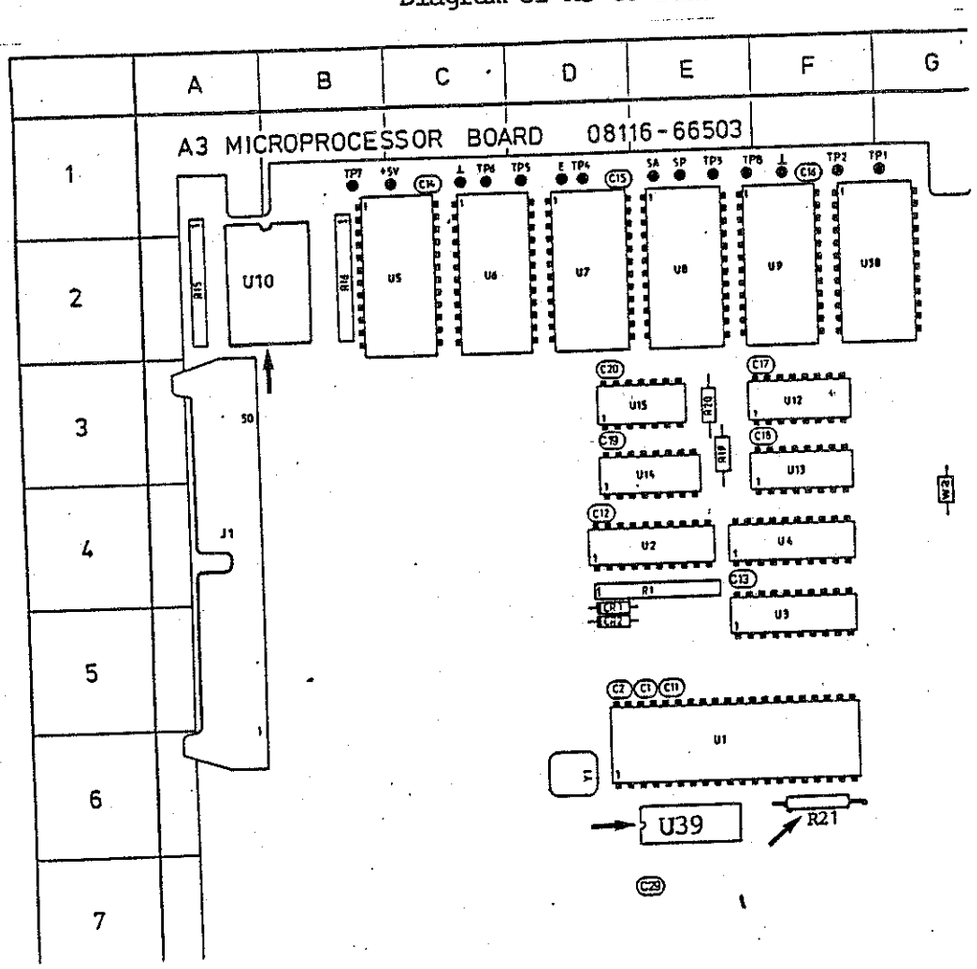
MANUAL CHANGE 6

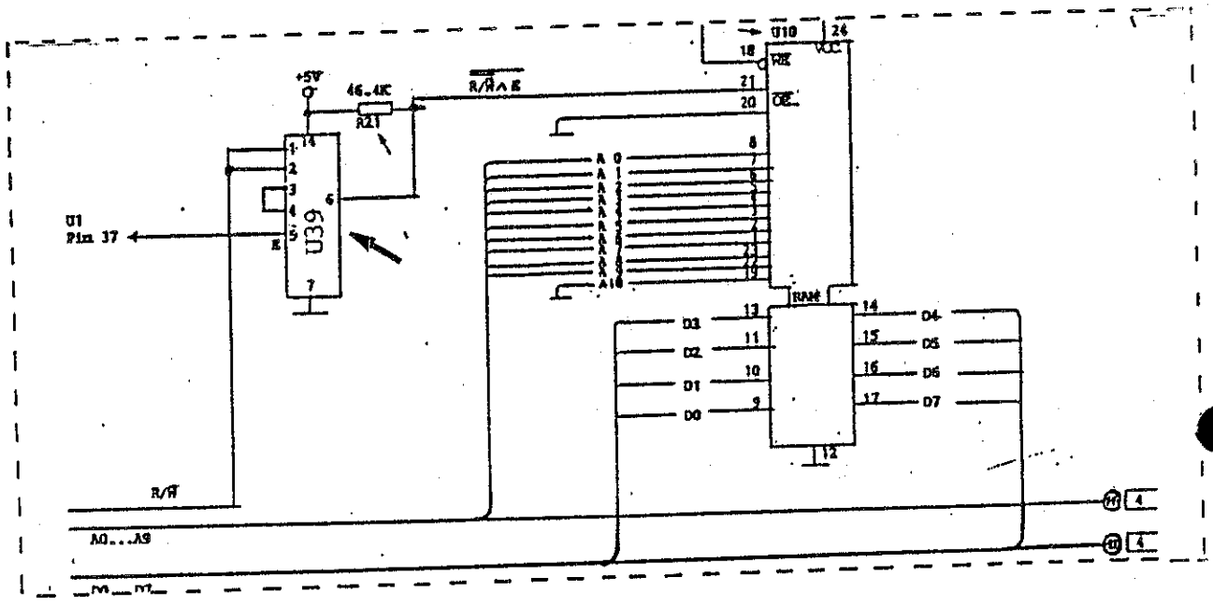
Page 6-12, change the Table of Replaceable Parts to read:

	A3U10	1818-1768	IC HM6116LP-3
Add:	A3R21	0698-3162	R-FXD 46.4K 1% .125W
	A3U39	1820-1197	IC SN74LS00N
Delete:	A3U11		

MANUAL CHANGE 6 (Cont.)

On Page 8-8/9, Service Sheet 3, change the Component Locator and Diagram of A3 to read:





MANUAL CHANGE 6 (Cont.)

On Page 8-8/9, Service Sheet 3:

On Ref.Des.Table and Grid Location:

Add:	R21	F6	Delete: U11
	U39	E6	

MANUAL CHANGE 7

On Page 6-9, change the Table of Replaceable Parts to read:

A1R400*	0698-3540	R-FXD 15.4 K 1%
A1R436*	0698-3258	R-FXD 5.36 K 1%

MANUAL CHANGE 8

On Page 6-6 thru 6-11, change the Table of Replaceable Parts to read:

A1C523,524	5180-0582	C-SELECTED
A1C100,101,103,106, C108,152,153,212, C214,215,220,224, C231,241,260,261, C263,301,302,403, C405,408, C512 thru 518,526 C533 thru 537,550	0160-5746	C-FXD 0.1 UF 20%
A2C5-17,18,19,23,26,29		
A3C3,4,5,9 C11 thru 28 C30 thru 34,36		

On Page 6-15, change the Table of Replaceable Parts to read:

Option 001:

A2C5,		
C17 thru 19 C22 thru 30	0160-5746	C-FXD 0.1 UF 20%

MANUAL CHANGE 9

IMPORTANT NOTE: New part numbers assigned to the following items since all threaded holes or screws are now METRIC!

On Page 6-5, change the Table of Replaceable Parts to read:

MP 4	08116-00204	PNL SUB
MP 7	5021-5813	FRAME FRONT
MP 8	5021-0512	FRAME REAR
MP12,13	5021-5831	SIDE STRUT
MP17	5001-1227	CVR BOTTOM
MP18	08116-04102	CVR TOP

MANUAL CHANGE 10

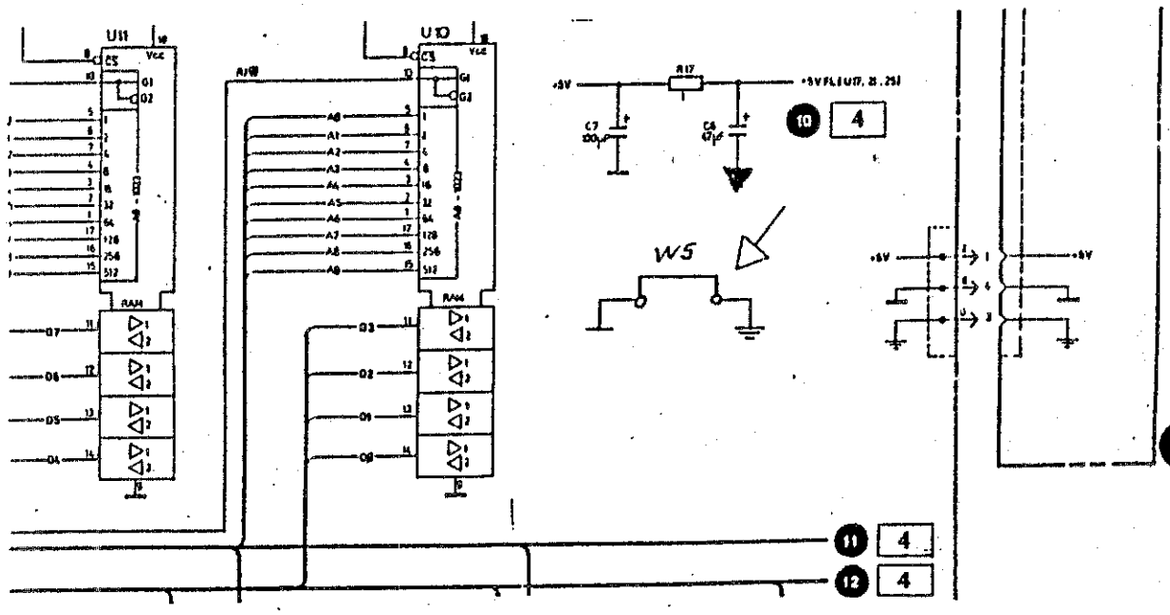
On Page 6-5 and 6-11, change the Table of Replaceable Parts to read:

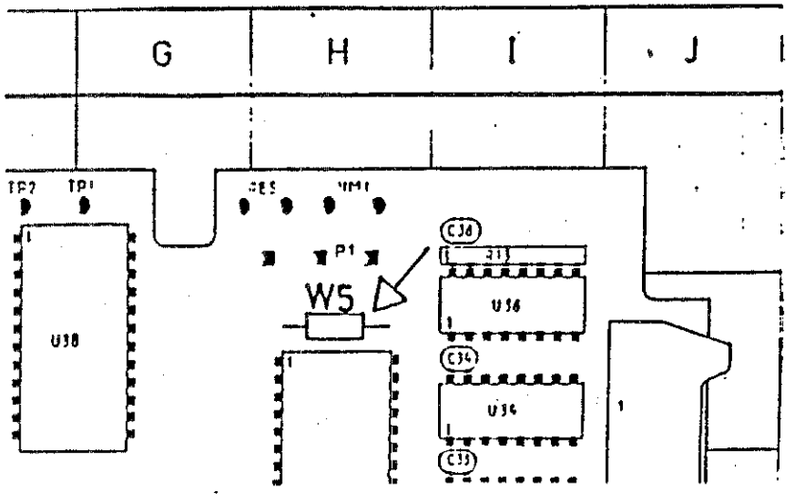
A3	08116-66513	BD AY MICROPRCR

On Page 6-12, Replaceable Parts List:

Add:	A3W5	8159-0005	RESISTOR ZERO OHMS

On Page 8-9, on Schematic and Component Layout add:





On Ref. Des Table and Grid Loc add:

W5	H2

MANUAL CHANGE 10 (Cont.)

On Page 6-5, change the Table of Replaceable Parts to read:

	F1 (2110-0063)	2110-0360	FUSE 750mA

MANUAL CHANGE 11

On Page 6-8, change the Table of Replaceable Parts to read:

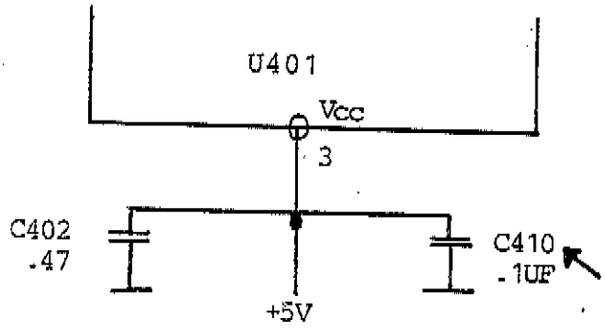
	A1*R242	0698-4467	R-FXD 1.05K 1% .125W

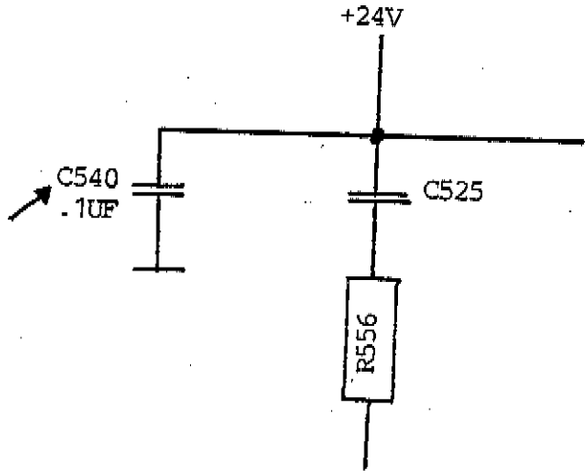
MANUAL CHANGE 12

On Page 6-6 and 6-7, change the Table of Replaceable Parts to read:

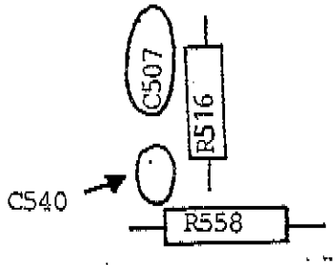
	A1 C406	0160-5730	C-FXD	100 PF
	A1*C409	0160-5739	C-FXD	15 PF
Add:	A1 C410	0160-5746	C-FXD	.1 UF
Add:	A1 C540			

On Page 8-18, on Schematic and Component Layout add:





Layout Page 8-18



On Ref. Des Table and Grid Loc add:

C540 M6
C410

The C410 will be backloaded until the next Board Rev. will be available.

MANUAL CHANGE 13

NOTE: The valid Run for the Option 001 remains 031569 but beginning with Ser.-No. 2520G04378. The valid Run for the Standard-Instrument is 031571 beginning with Ser.-No. 2520G04425.

On Page 6-5, change the Table of Replaceable Parts List to read:

	A2	08116-66522	BD AY-CONTROL

On Page 6-10/11, change the Table of Replaceable Parts List to read:

	A2 K1,2,3,4	0490-1412	RELAY REED
ADD:	A2 R68	0757-0442	F-FXD 10K 1% .125W
	A2 CR20	1901-0376	DIO LOW LEAKAGE
DEL:	A2 CR1,2,3,4		

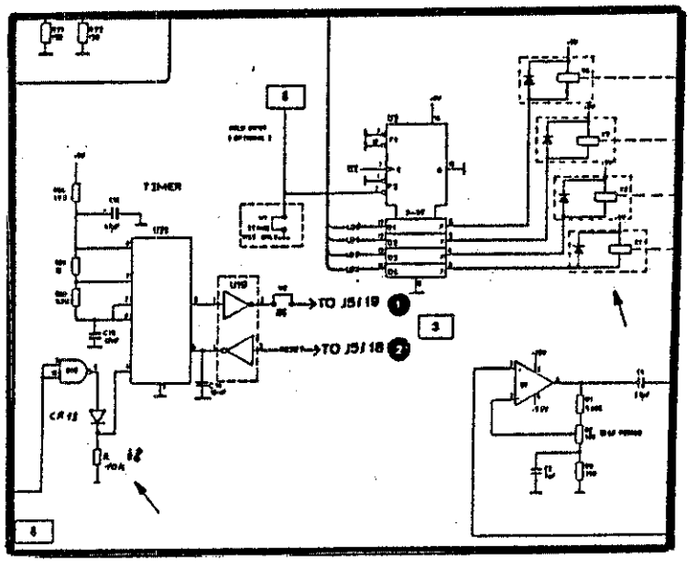
On Page 6-15, change the Table of Replaceable Parts List to read:

Option 001:

	A2	08116-66532	BD AY-CONTR.OPT.
	A2 K1,2,3,4	0490-1412	RELAY REED
ADD:	A2 R68	0757-0442	R-FXD 10K 1% .125W
	A2 CR20	1901-0376	DIO LOW LEAKAGE
DEL:	A2 CR 1,2,3,4		

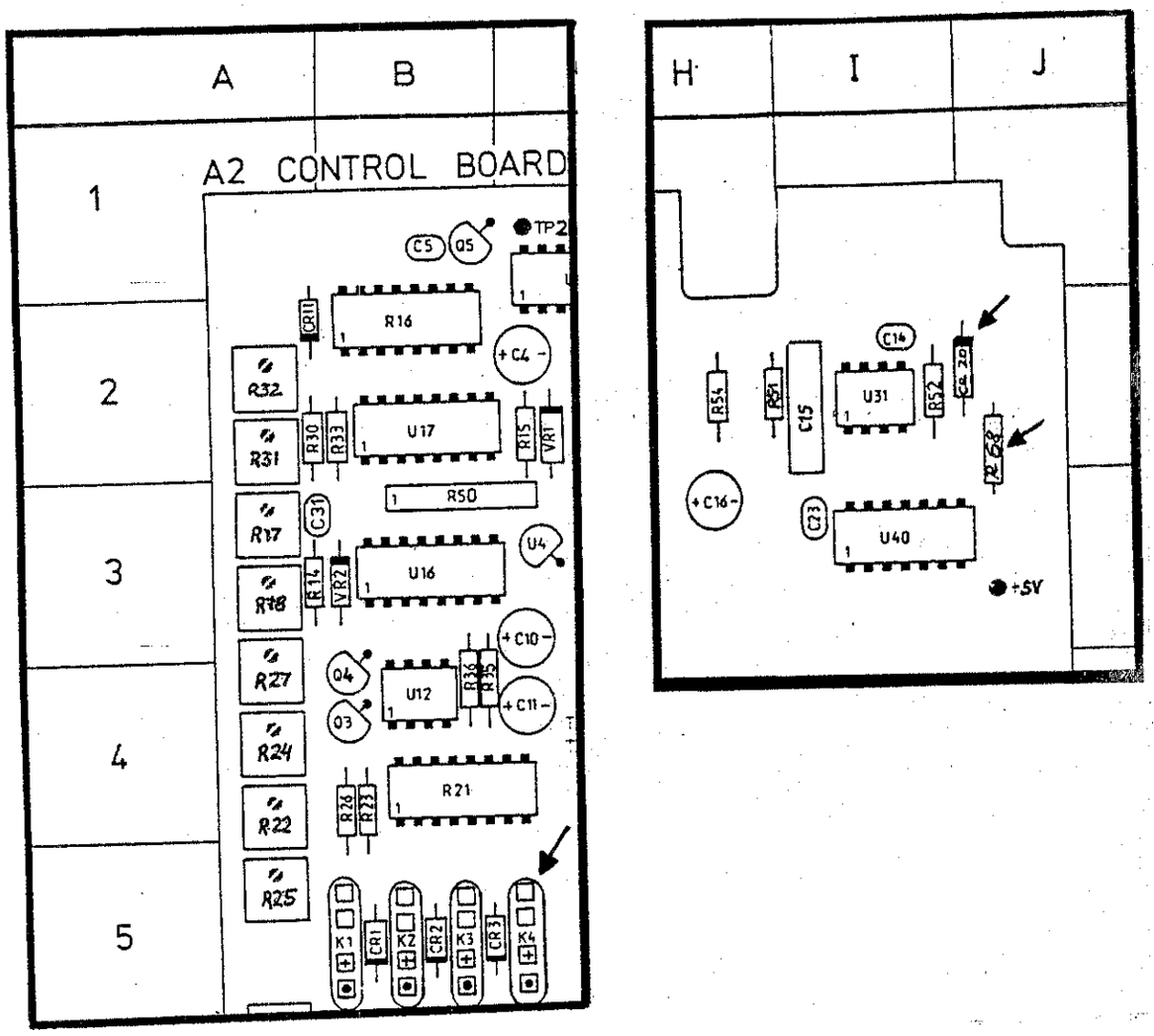
On Page 8-13, on Schematic add:

Control 5:



MANUAL CHANGE 13 (Cont.)

On Page 8-13, on Component Layout add:



MANUAL CHANGE 14

On Page 6-7, change the Table of Replaceable Parts to read:

A1	*L502	9170-0894	BEAD INDUCTIVE

On Page 6-10,

Delete: R558

MANUAL CHANGE 15

On Page 6-8, change the Table of Replaceable Parts to read:

A1 *R220	0757-0279	R-FXD 3.16K 1%

MANUAL CHANGE 16

On Table 6-3., Replaceable Parts List change to read:

A1	08116-66521	BD AY-MAIN
MP18	08116-04103	COVER TOP
A1 K201,202, A1 K501-506	0490-1412	RELAY REED
A1 CR513,514	1901-0050	SWITCH. DIO
A1 *C409	0160-5736	C-FXD 22PF
A1 *C502	0160-4389	C-FXD 150PF
A1 R19,24	2100-3089	R-TRMR 5K

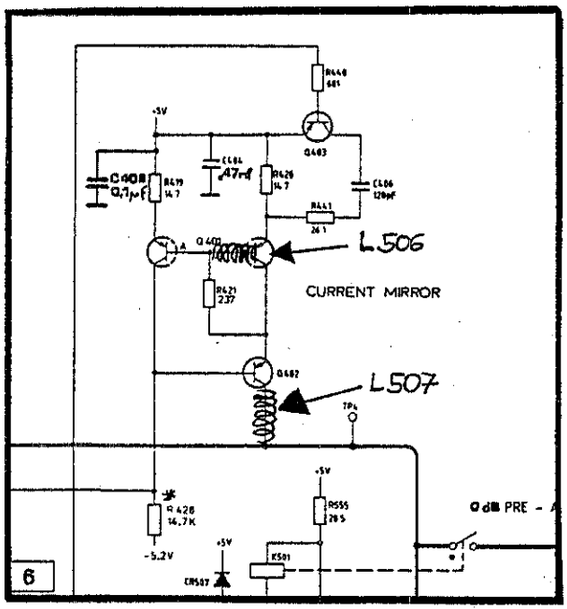
ADD:

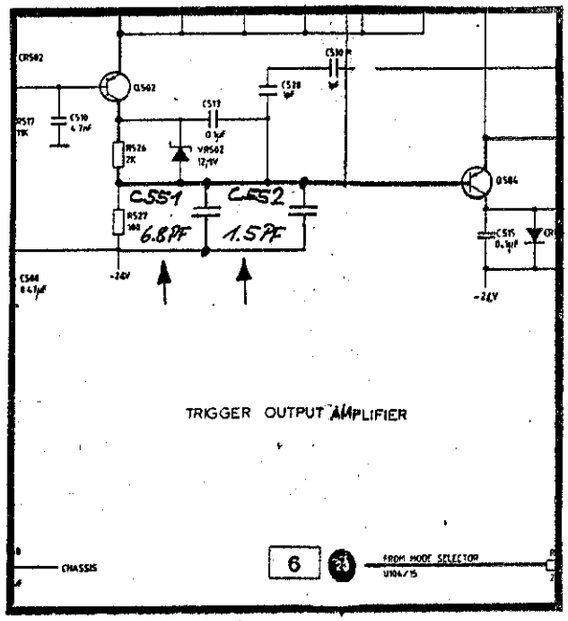
A1 CR515,516	1901-0050	SWITCH.DIO
A1 CR504-507	1902-1340	DIO 18V
A1 W 12,13,14	8159-0005	RESISTOR
A1 C551	0160-5738	C-FXD 6.8PF
A1 C552,553	0160-4381	C-FXD 1.5PF
A1 *L506,507	9170-0894	CORE MAGNETIC

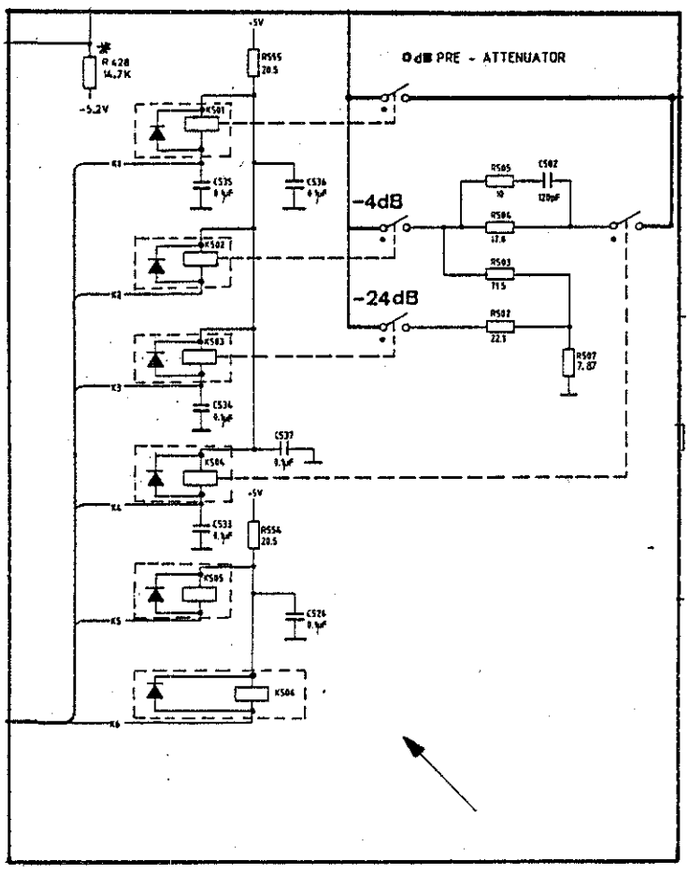
DELETE: A1 CR201,202,507-512
A1 R20
A1 R21

MANUAL CHANGE 16 (Cont.)

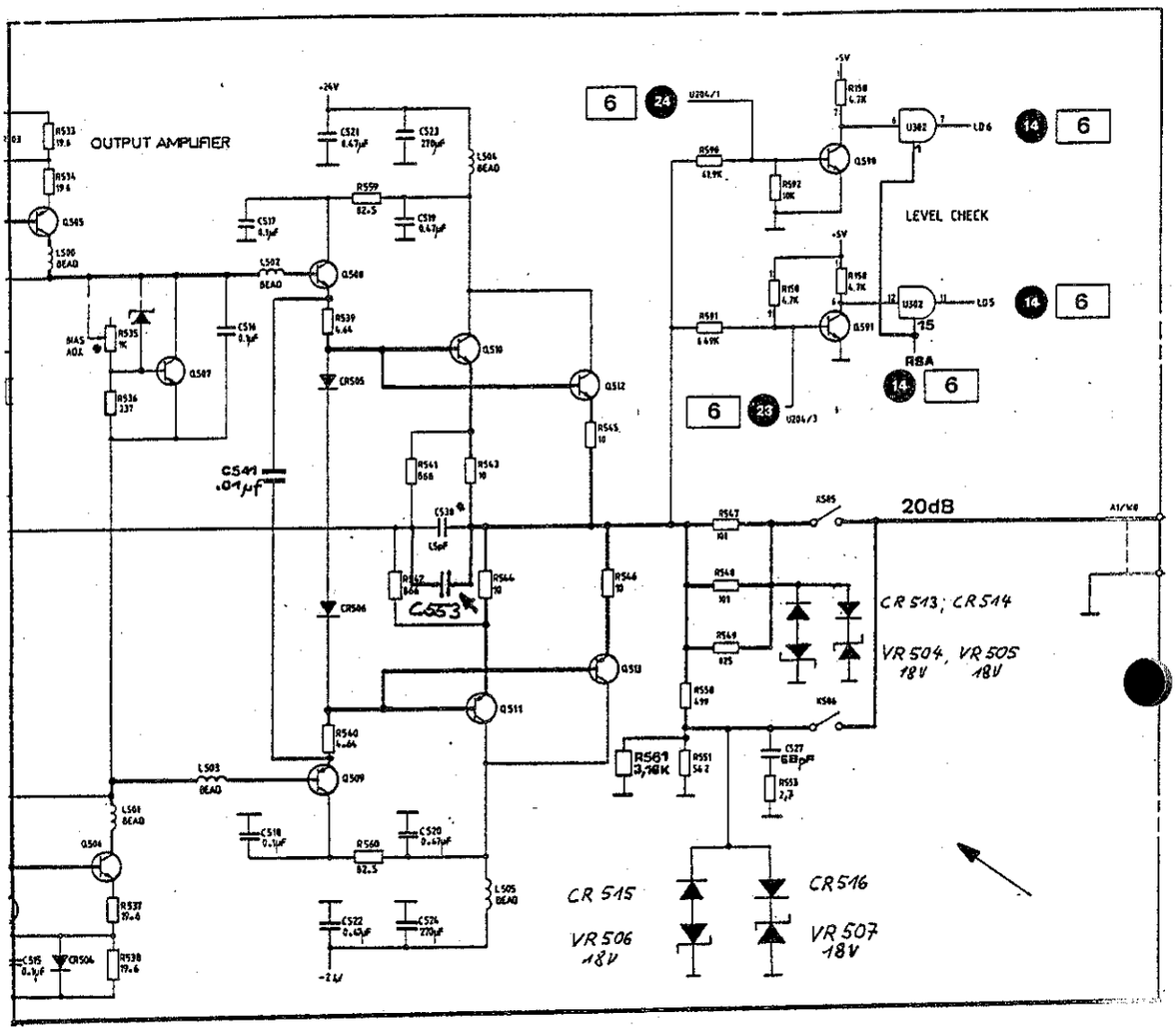
On Schematic, Page 8-18, ADD:



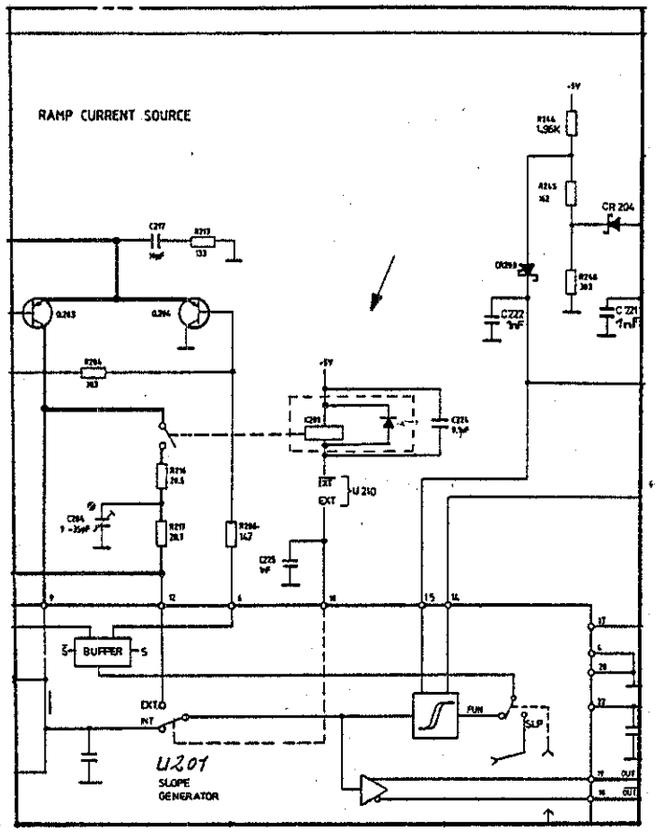


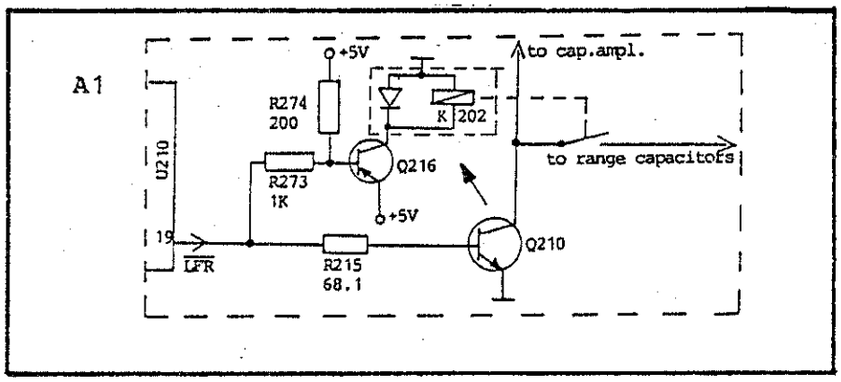


MANUAL CHANGE 16 (Cont.)

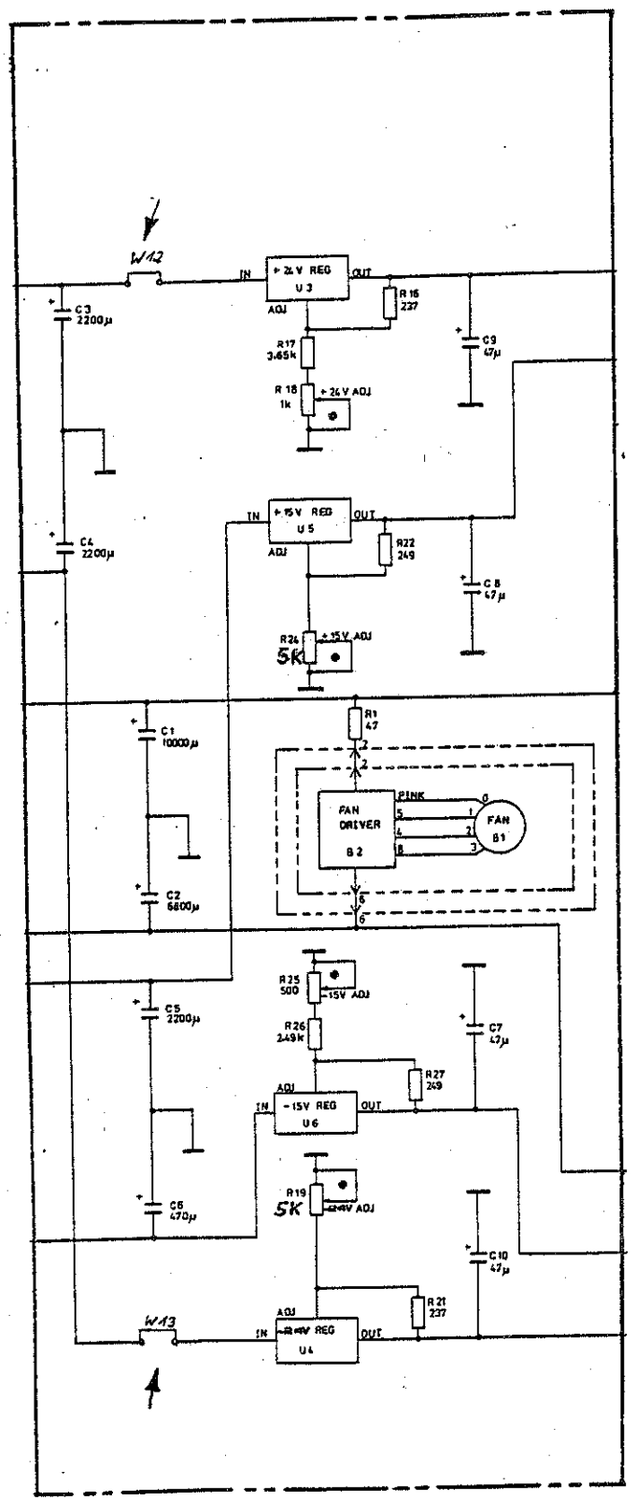


MANUAL CHANGE 16 (Cont.)

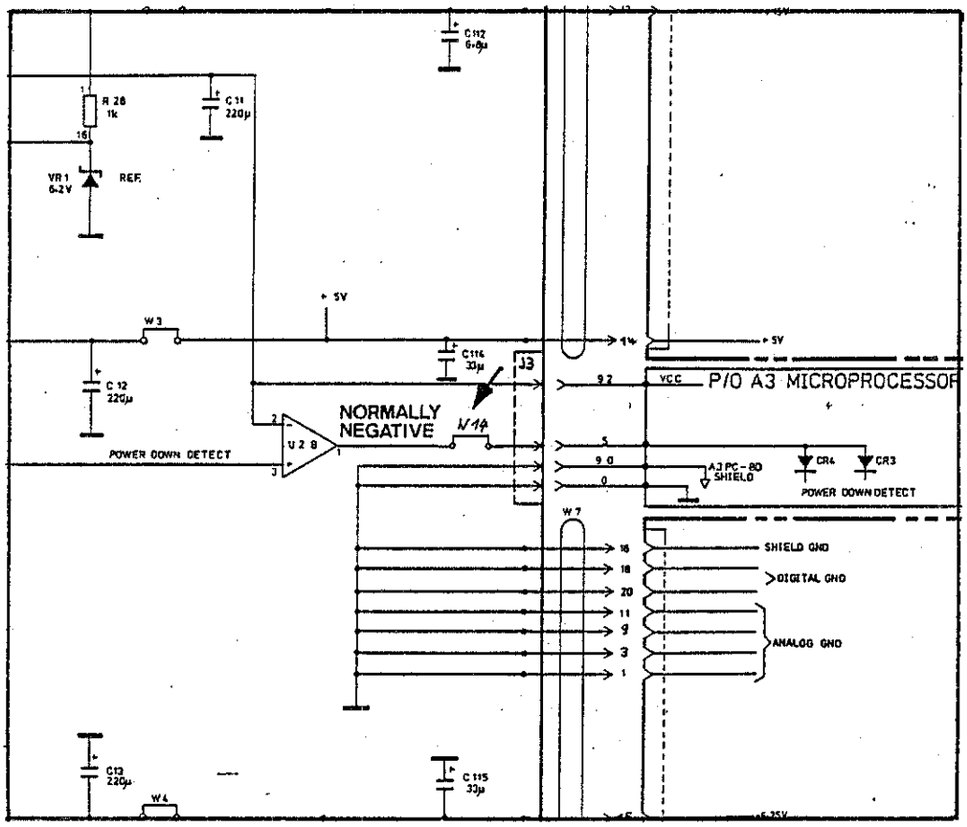




MANUAL CHANGE 16 (Cont.)

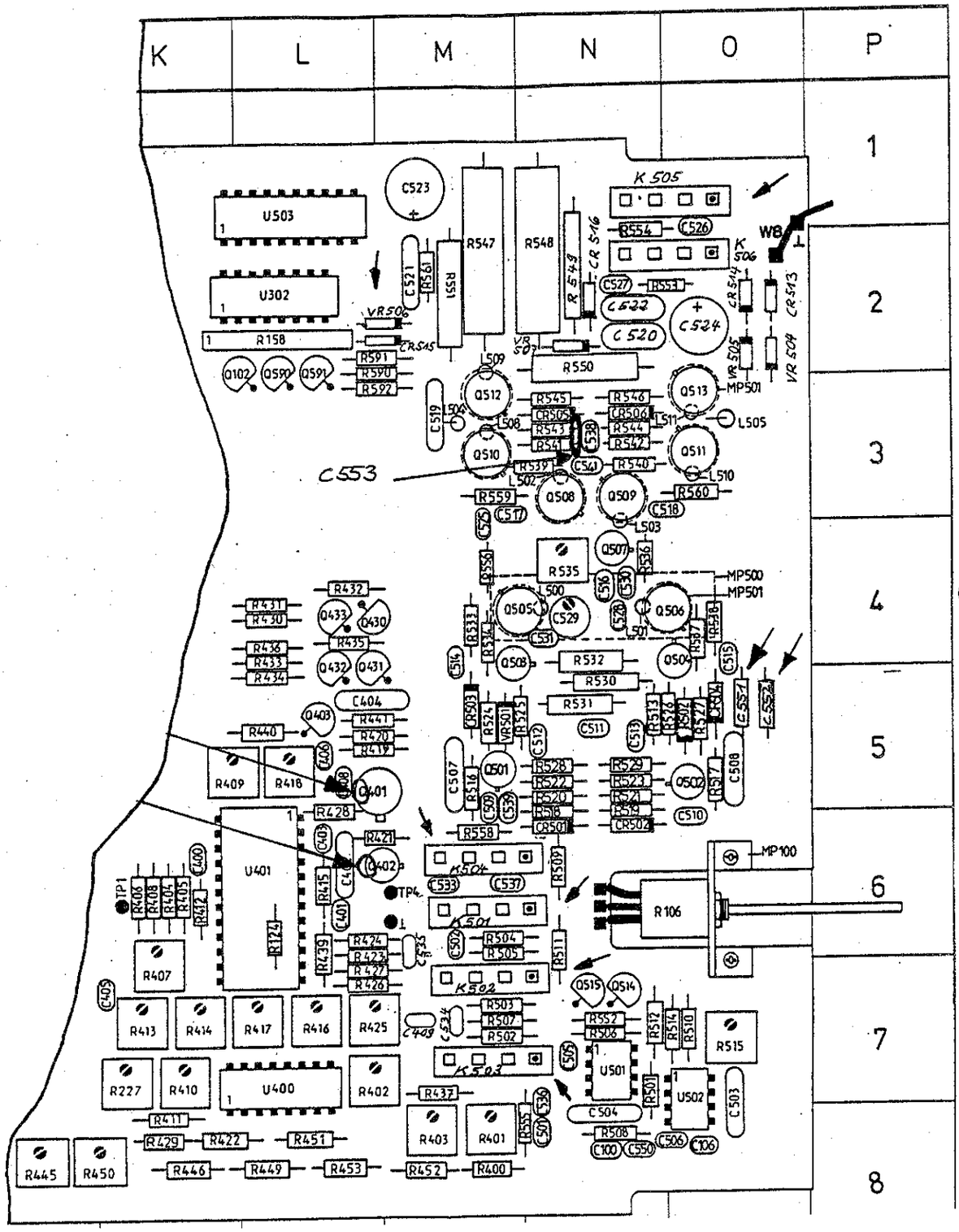


MANUAL CHANGE 16 (Cont.)

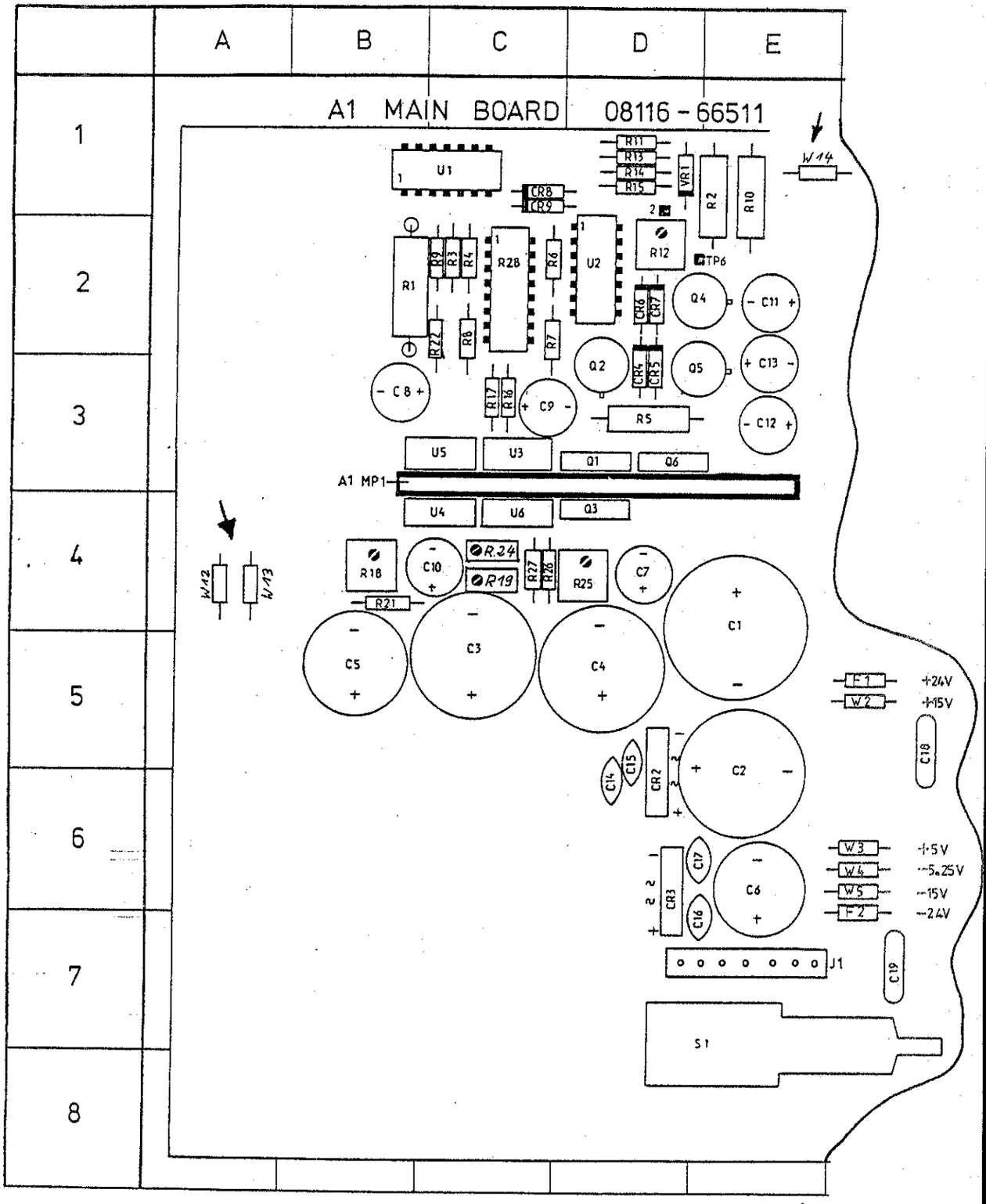


MANUAL CHANGE 16 (Cont.)

On Component Layout, Page 8-18, ADD:



MANUAL CHANGE 16 (Cont.)



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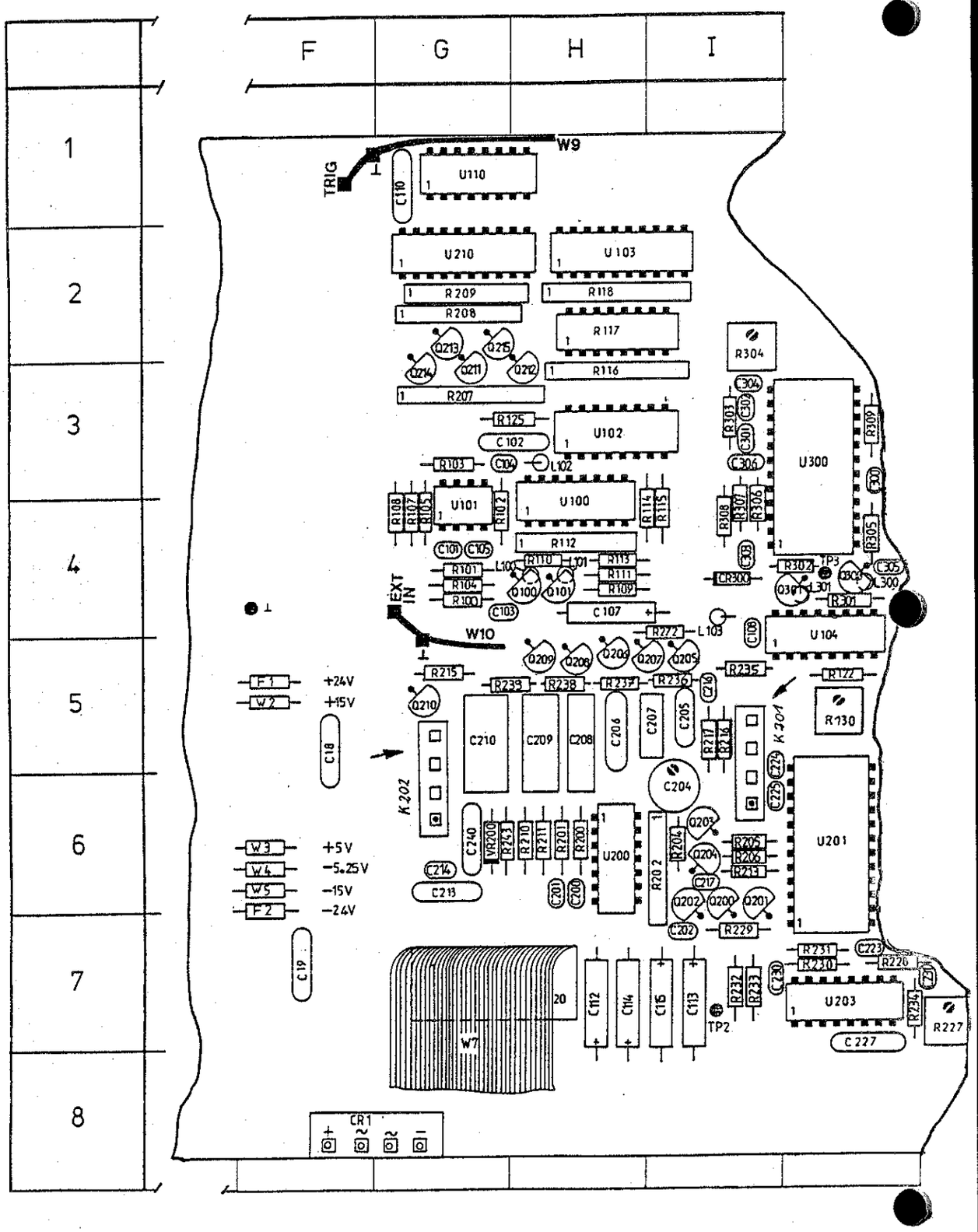


MANUAL CHANGE 16 (Cont.)

On Page 6-7, Replaceable Parts List:

ADD: A1 *C554 0160-5730 C-FXD 100pf

Page 1-3 change: GENERAL INFORMATION

Rise/fall time specification for square pulse under WAVEFORM CHARAKTERISTICS to read: <7ns (10% to 90% of amplitude)

Page 4-9 change: PERFORMANCE TESTS

Transistion time specifications for PULSE CHARACTERISTICS to read: Transition time (10% to 90%):<7ns

change: Procedure step 3 leading edge (risetime) and trailing edge (risetime) to<7ns

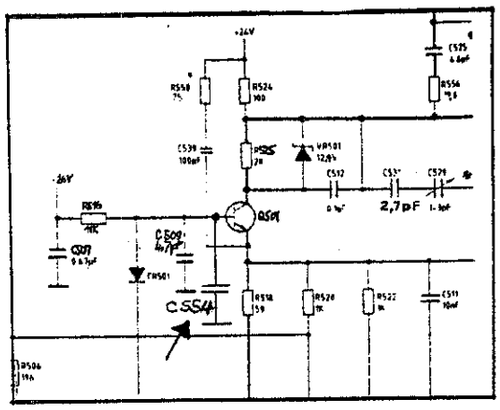
Page 4-22 change:PERFORMANCE TEST RECORD

Para.No 4-15 leading edge and trailing edge max to<7ns

Page 5-4 change: ADJUSTMENT PROCEDURES

Transition in steps 5,6 and 7 of OVERSHOOT/ TRANSITION procedure from< 5,6ns to<6,6ns.

On Schematic, Page 8-18, add:

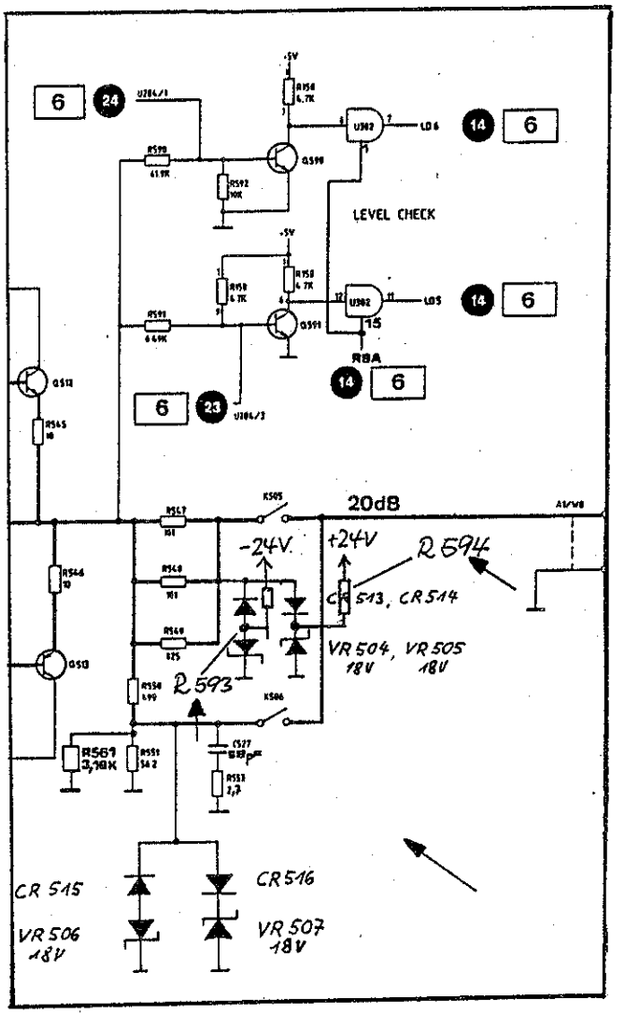


MANUAL CHANGE 16 (Cont.)

On Table 6-3., Replaceable Parts List, change to read:

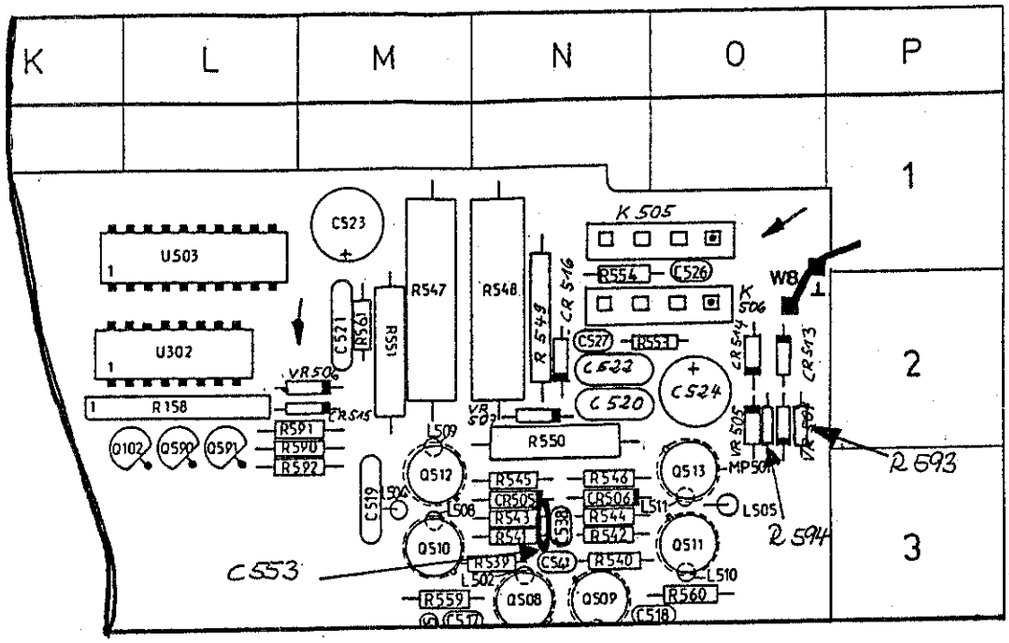
	A1 *C409	0160-5739	C-FXD 15PF
Delete:	A1 *R558		
Add:	A1 R593,594	0757-0280	R-FXD 1K

On Schematic, Page 8-18, add:



MANUAL CHANGE 16 (Cont.)

On Component Layout, Page 8-18, add:



MANUAL CHANGE 17

On Table 6-3., change the Table of Replaceable Parts to read:

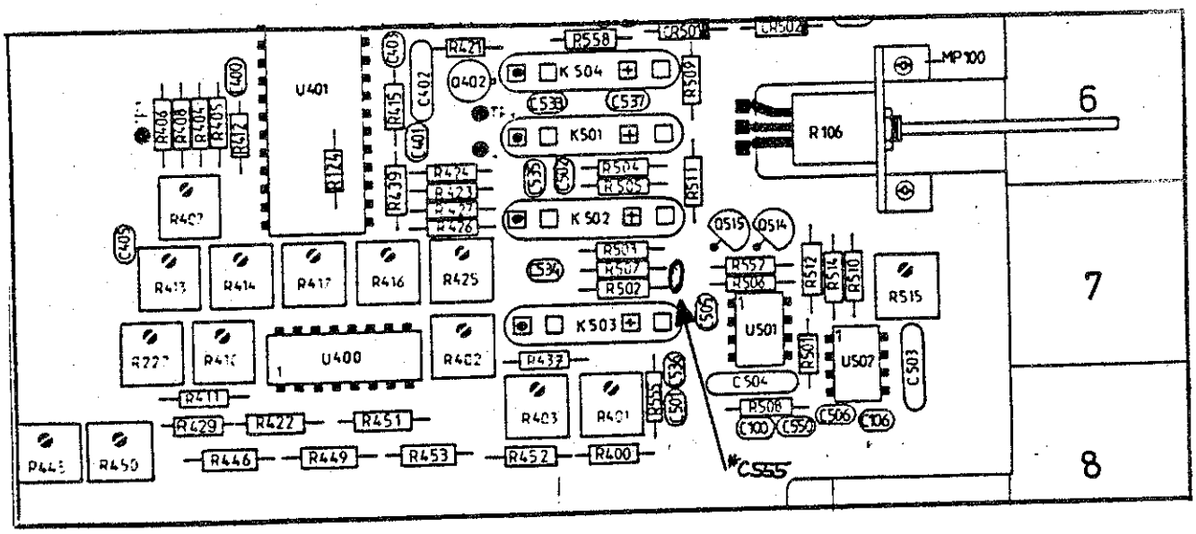
A1	*C409	0160-5736	C-FXD 22PF 5% 100V
A1	C539	0160-5730	C-FXD 100PF 5%
A1	*C502	0160-5730	C-FXD 100PF 5%

Delete: C553

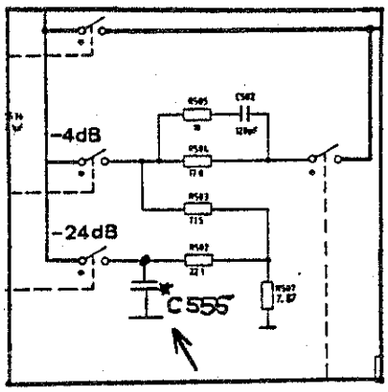
ADD: A1 *C555 0160-5738 C-FXD 6,8PF

MANUAL CHANGE 17 (Cont.)

On Component Layout, Page 8-18, add:



On Schematic, Page 8-18, add:



MANUAL CHANGE 18

On Page 6-7, change the Table of Replaceable Parts to read:

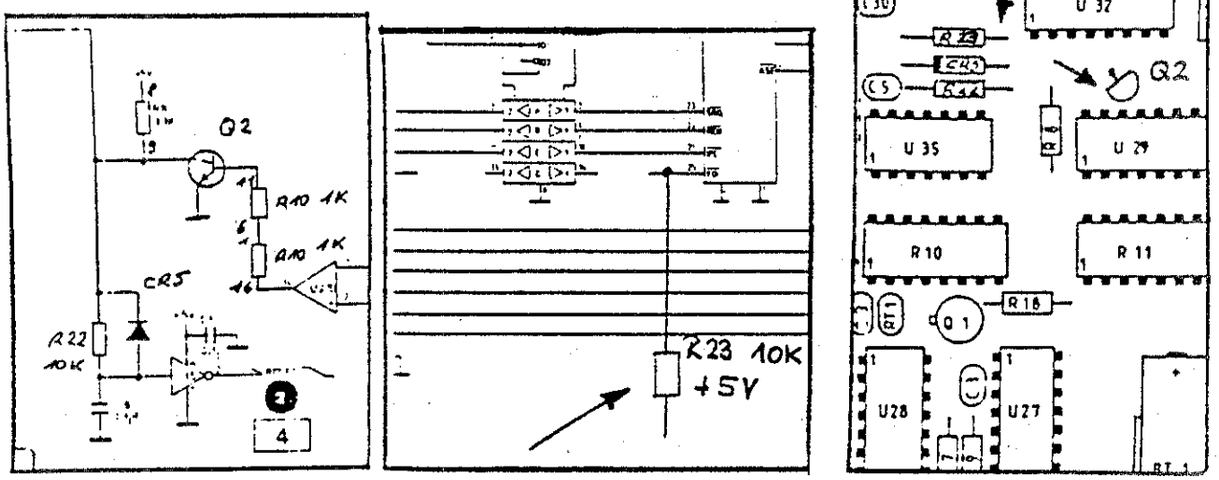
A1	MP 501	1205-0662	HEATSINK

MANUAL CHANGE 18 (Cont.)

On Page 6-11/6-12, Replaceable Parts List:

Add:	A3	CR 5	1901-0535	DIO SCHOTTKY
	A3	Q 2	1854-0215	XSTR NPN 2N3904
	A3	R 22,23	0757-0442	R-FXD 10K 1% .125W

On Schematic and Component Layout, Page 8-9, add:



On Ref Des Table and Grid Loc add:

CR5	H4
Q 2	I4
R22	H4
R23	H4

MANUAL CHANGE 19

On Page 6-7, change the Table of Replaceable Parts to read:

	A1 L260	9100-2255	IDCTR 470 NH 10%
Delete:	L261		

MANUAL CHANGE 20

On Table 6-3, Replaceable Parts List, change to read:

A1 J2	1252-0277	CONN-POST-TP-HDR
A3 J1	1251-8465	CONN-POST- 50 CONT.
A3 J2	1251-8930	CONN-POST-TP-HDR

MANUAL CHANGE 21

On Table 6-3, Replaceable Parts List, change to read:

MP8	5021-5814	FRAME REAR

On Table 6-3, Replaceable Parts List, change to read:

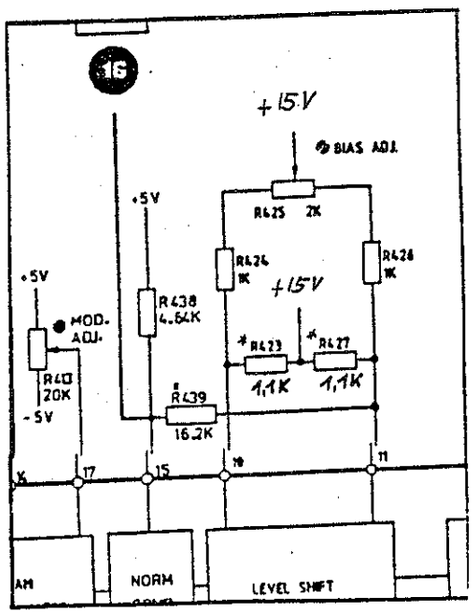
A1 *C300	0160-4385	C-FXD 15PF 200V
A1 *R309	0757-0394	R-FXD 51,1 1%

MANUAL CHANGE 22

On Page 6-9, change the Table of Replaceable Parts to read:

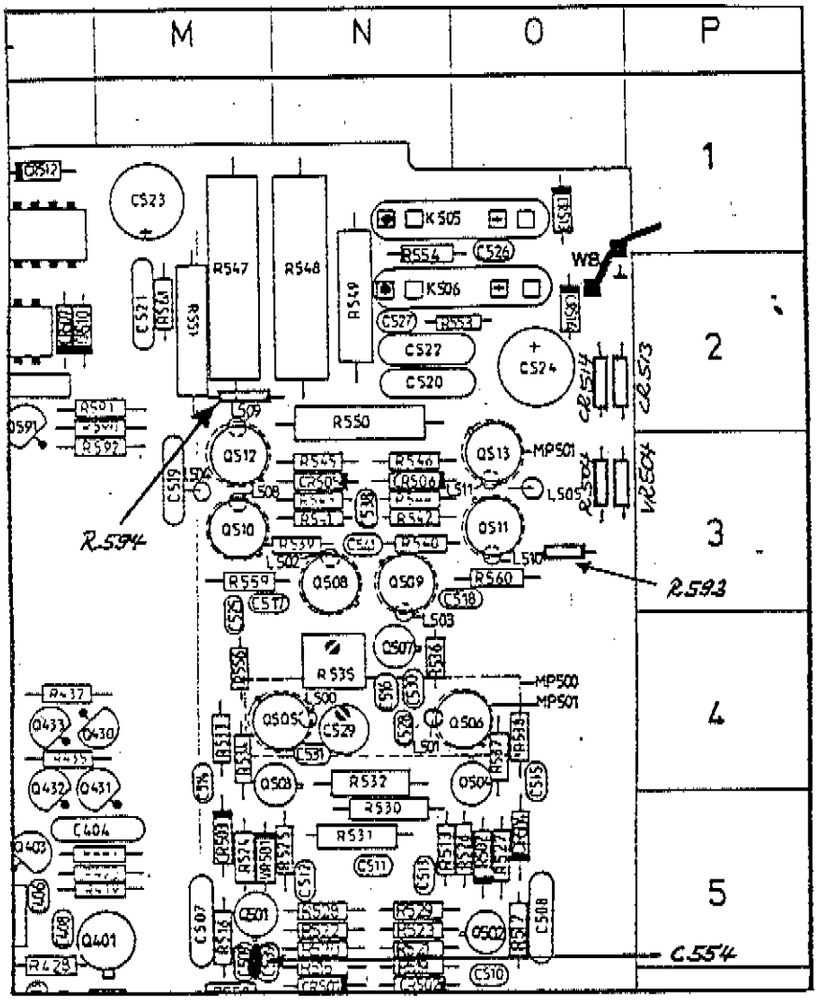
A1 *R423	0757-0424	R-FXD 1,1K 1% .125W
A1 *R427		
A1 R226	0698-4431	R-FXD 2,05K 1%
A1 R436	0698-3226	R-FXD 6,49K 1%

On Schematic, Page 8-18, change:



MANUAL CHANGE 22 (Cont.)

On Component Layout, Page 8-18:



NOTE: IF THE SHAPER IC U401 HAS BEEN REPLACED, CHECK THE DC-VOLTAGE ON U401 PIN 10 AND PIN 11.
IF THE LEVEL IS OUT OF 2,2 V TO 2,6V RANGE, *R423 AND *R427 HAVE TO BE CHANGED TO VALUES BETWEEN 1,05K to 1,15K.

MANUAL CHANGE 23

On Table 6-3, change the Table of Replaceable Parts to read:

A1 *C525	0160-3874	C-FXD 10PF
A1 *R423,427	0698-4467	R-FXD 1,05K

MANUAL CHANGE 24

On Page 6-3, change the Table of Replaceable Parts to read:

MP8	5021-0512	FRAME REAR

LIST OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

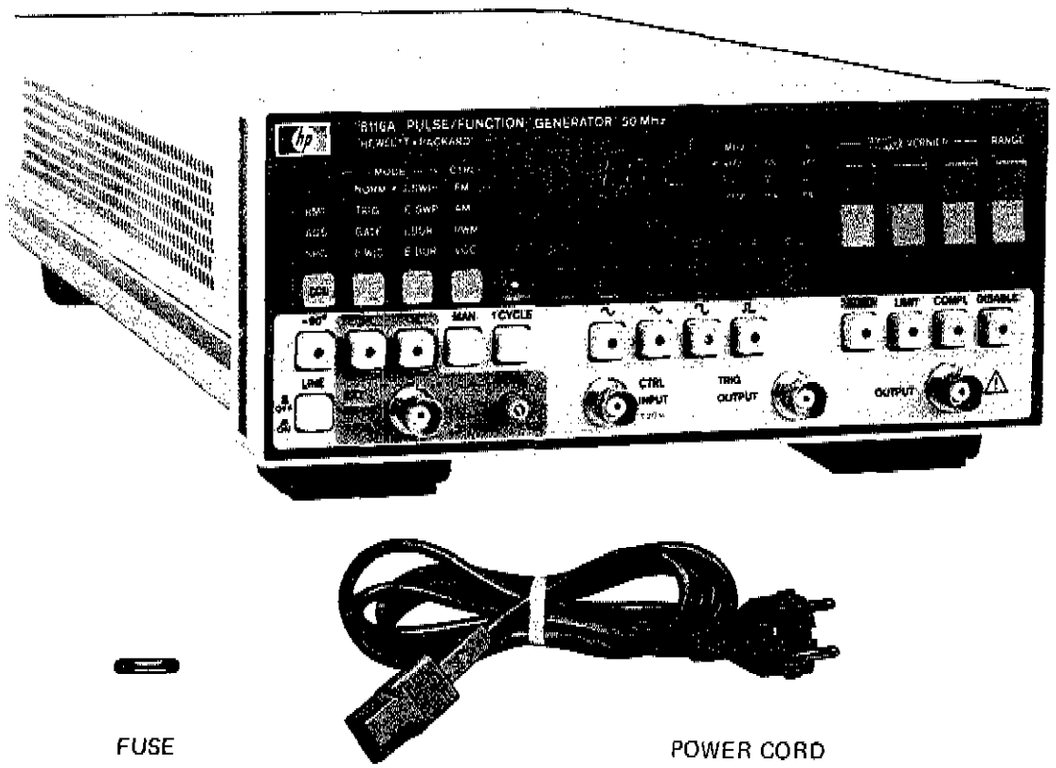


Figure 1–1. 8116A and Supplied Accessories (Instrument shown with Option 001 fitted).

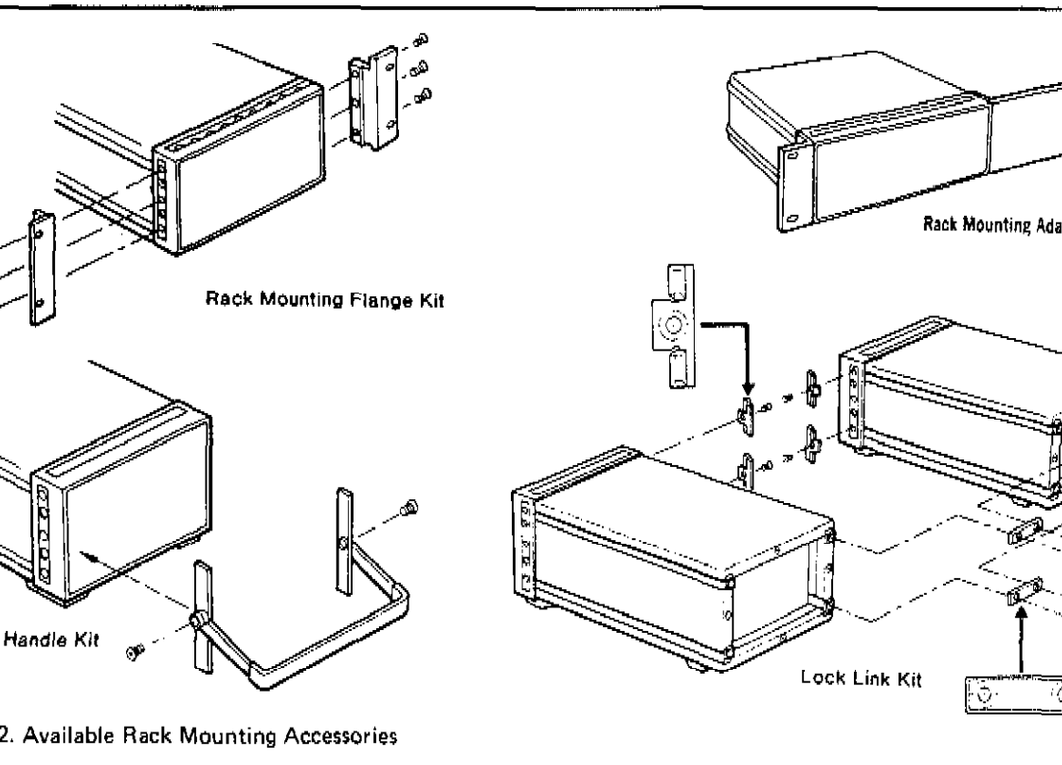


Figure 1–2. Available Rack Mounting Accessories

SECTION I
GENERAL INFORMATION

1–1 INTRODUCTION

1–2 This Operating and Service Manual contains information required to install, operate, test, adjust and service the Hewlett-Packard Model 8116A. Figure 1–1 shows the mainframe and accessories supplied. This section covers instrument identification, description, accessories, specifications, and other basic information.

1–3 A Microfiche version of this manual is available on 4 x 6 inch microfilm transparencies (order number on title page). Each microfilm contains up to 60 photoduplicates of the manual pages. The microfiche package also includes the latest Manual Changes supplement as well as all pertinent Service Notes.

1–4 SPECIFICATIONS

1–5 Instrument specifications are listed in Table 1–2. These specifications are the performance standards or limits against which the instrument is tested.

1–6 SAFETY CONSIDERATIONS

1–7 The 8116A is a Safety Class 1 instrument (it has an exposed metal chassis that is directly connected to earth via the power supply cable). Before operation, the instrument and manual, including the red safety page, should be reviewed for safety markings and instructions. These must then be followed to ensure safe operation and to maintain the instrument in a safe condition.

1–8 INSTRUMENTS COVERED BY MANUAL

1–9 Attached to the rear of this instrument is a serial number plate (Figure 1–3). The first four digits of the serial number only change when there is a significant change to the instrument. The last five digits are assigned to instruments sequentially. The contents of this manual apply directly to the instrument serial number quoted on the title page. For instruments with lower serial numbers, refer to the backdating information in Section VII of this manual. For instruments with higher serial numbers, refer to the Manual Change sheets at the end of this manual. In addition to change information, the Manual Change sheets may contain information for correcting errors in the manual. To keep this manual as up-to-date and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Change supplement. The supplement for this manual is identified with the manual's print date and part number, both of which appear on this manual's title page. Complimentary copies of the supplement are available from Hewlett-Packard.

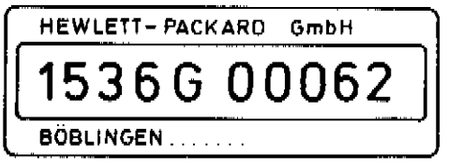


Figure 1–3. Serial Number Plate

1–10 DESCRIPTION

1–11 The HP 8116A Programmable Pulse/Function Generator operates over the frequency range 1 mHz to 50 MHz and up to 32 V peak-to-peak amplitude. Capabilities include:

- Multiwaveform generation (sine, square, triangle, pulse)
- 6 ns transition time for pulse and squarewave
- Variable pulse width down to 10 ns
- AM/FM/PWM modulation modes
- VCO control mode
- Fully HP-IB programmable
- Internal and external logarithmic sweep (Opt. 001)
- Internal and external burst mode for all waveforms (Opt. 001)

1–12 A unique self-prompting operating concept, plus the full HP-IB programmability, provide an easy means to execute single manual operation or complex automatic tasks.

1–13 8116A Options.

1–14 Option 001. The 8116A can provide increased capabilities with the addition of Option 001. Added capabilities include:

- Logarithmic sweep (selectable internal or external triggering)
- Counted burst (selectable internal or external triggering)
- Hold input for sine, triangle and squarewave.

1–15 ACCESSORIES SUPPLIED

1–16 The 8116A is supplied complete with the following items:

ITEM	HP PART NUMBER
750 mA fuse for 220/240 V operation or,	2110–0063
1.5 A fuse for 100/120 V operation	2110–0043
Power cable	See Figure 2–2

1–17 ACCESSORIES AVAILABLE

ITEM	HP PART NUMBER
Carrying handle – Bail Handle Kit	5061–2001
Rack mounting adaptors: Rack mounting flange and filler panel for rack mounting a single 8116A,	5061–0072
Rack mounting flange and lock link kit for rack mounting two 8116A's	5061–0074 5061–0094

1–18 RECOMMENDED TEST EQUIPMENT

1–19 Equipment required to maintain the 8116A is listed in Table 1–1. Alternative equipment can be substituted provided that it meets or exceeds the critical specifications listed in the table.

Table 1–1. Recommended Test Equipment

Instrument	Recommended Model	Required characteristics	Adequate Substitute	Use*
Counter	HP 5335A	50 MHz, Start/Stop, T I, A to B	HP 5345A + HP 5363B	P, A P, A
DVM	HP 3455A	DC .1 V–10 V, .004 % acc.	HP 3456A	P, A
DMM	HP 3465A	AC .1 V–10 V DC .1mA - 10mA	HP 3456A	P, A, T
Function Generator	HP 3325A	20 MHz, THD ≤ .1 %		P, A
Real Time Scope	HP 1740A	100 MHz Bandwidth	HP 1743A	P, A, T
Sampling Scope	TEK 7603 with 7T11/7S11 and S–3A	1 GHz	HP 140A/ 1410A	P, A
Spectrum Analyzer	HP 3580A	5 Hz – 50 kHz	HP 3585A	P, A
Spectrum Analyzer	HP 181T/ 8557A	350 MHz		P
Signature Analyzer	HP 5005A		HP 5004A	T
Logic Probe	HP 545A	TTL		T

* P = Performance Test; A = Adjustments; T = Troubleshooting

Table 1–2. Specifications

The following specifications apply with 50 Ohm load resistance. Output levels double when driving into high impedance (up to 32 Vpp).
Accuracy specifications apply from 15°C to 35°C.
For temperatures below 15°C and above 35°C see "General" information.

WAVEFORMS

Sine, Triangle, Ramp, Square, Pulse, Haversine, Havertriangle, DC

TIMING CHARACTERISTICS

Frequency
Range: 1.00 mHz to 50.0 MHz
Resolution: 3 digits

Accuracy (% of setting)	Pulse mode or 50 % duty cycle	≠ 50 % duty cycle
1.0 mHz to 99.9 kHz	± 3 % ± 0.3 mHz	± 3 % ± 0.6 mHz
100 kHz to 9.99 MHz	± 5 %	± 10 %
10.0 MHz to 50 MHz	± 5 %	------

Repeatability: Factor 4 better than accuracy
Jitter: < 0.1 % + 100 ps (50 % duty cycle and pulse mode)
< 0.2 % + 100 ps (≠ 50 % duty cycle)
Stability: ± 0.2 % (1 hour)
± 0.5 % (24 hours)

Duty Cycle (sine, triangle, square)

Range: 10 % to 90 % (1 mHz to 999 kHz)
20 % to 80 % (1 MHz to 9.99 MHz)
Resolution: 1 %
Accuracy: ± 0.5 digits (100 mHz to 999 kHz)
± 3.0 digits (1 MHz to 9.99 MHz)

Pulse Width (pulse mode)

Range: 10.0 ns to 999 ms
Resolution: 3 digits
Accuracy: ± 5 % of setting ± 2 ns
Repeatability: Factor 4 better than accuracy
Jitter: 0.2 % + 200 ps (width ≤ 10 µs)
0.1 % (width > 10 µs)
Max. Width: Period –10 ns

OUTPUT CHARACTERISTICS

Output Impedance: 50 Ohm ± 5 %
Reflection: < 12 % (ampl. ≥ 100 mVpp)

Amplitude/Offset

Amplitude and offset are independently variable within the following two level windows

Level window	± 800 mV	± 8.00 V
Amplitude range	10.0 mVpp to 99.9 mVpp	100 mVpp to 16.0 Vpp
Ampl. resolution	3 digits	3 digits
Ampl. accuracy*	± 5 % [0.45 dB]	± 5 % [0.45 dB]
Repeatability	Factor 4 better than accuracy	
Offset range	0 to ± 795 mV	0 to ± 7.95 V
Offset resolution	3 digits (best case 100 µV)	3 digits (best case 1 mV)
Offset accuracy	± 1 % of setting ± 1 % of amplitude ± 4 mV	± 0.5 % of setting ± 1 % of amplitude ± 40 mV
Repeatability	Factor 4 better than accuracy	

* The amplitude accuracy for sine and triangle is specified at 1 kHz. For other frequencies see the following flatness specifications.

Amplitude Flatness (50 % duty cycle)	Sine	Triangle
1.00 mHz to 999 kHz	± 3 % (0.26 dB)	± 3 %
1.00 MHz to 9.99 MHz	± 5 % (0.45 dB)	± 5 %
	+ 5 % (0.45 dB)	+ 5 %
10.0 MHz to 50.0 MHz	– 15 % (1.41 dB)	– 25 %

DC Voltage (all waveform selection keys deactivated)

Range: 0 to ± 7.95 V
Resolution: 3 digits (best case 1 mV)
Accuracy: ± 0.5 % of setting ± 20 mV

WAVEFORM CHARACTERISTICS

Sine (Normal Mode, 50 % duty cycle)
Total Harmonic Distortion (THD): < 1 % (–40 dB), (10 Hz to 50 kHz)
Harmonic Signals: More than 34 dB below fundamental (50 kHz to 1 MHz)
More than 23 dB below fundamental (1 MHz to 50 MHz, > 20 mVpp –8 Vpp)
THD may increase by 3 dB below 10°C

Triangle, Ramp

Non-linearity: < ± 3 % (10 % to 90 % of amplitude, 100 mHz to 1 MHz)

Square, Pulse

Rise/Fall time: < 6 ns (10 % to 90 % of amplitude)
Pulse Perturbations: < ± 5 % of amplitude ± 2 mV

OPERATING MODES

Norm: Continuous waveform is generated
Trig*: Each input cycle generates a single output cycle
Gate *: External signal enables oscillator. First output cycle synchronous with active trigger slope. Last cycle always completed.
External Width : (pulse mode only) External signal will be shaped to determine output pulse width and period. Amplitude and offset controls are active.

Sweep: (Opt. 001 only) Logarithmic sweep for all waveforms up to full range (1 mHz to 50 MHz) between selected start and stop frequency. Sweep time per decade selectable in 1-2-5 sequence between 10 ms and 500 s.
Int. Sweep: Continuous sweep cycles.
Ext. Sweep: One sweep cycle generated on receipt of external signal.
(Duty Cycle 50 %)

Burst *: (Opt. 001 only) Preprogrammed number of periods (1 to 1999) is generated. Minimum time between bursts is 100 ns. For bursts with only one period, min time between bursts is 0 ns.
Int. Burst: (pulse mode not available) Internally generated signal starts burst. Repetition time: 20 ns to 999 ms
Ext. Burst: (all waveforms) External signals starts burst.
Freq max = 40 MHz

* Startphase of sine and triangle switchselectable to 0° and −90° for haversine and havertriangle.

AUXILIARY OPERATING MODES

Man: Simulates external input.
1 Cycle: (Opt. 001 only) Provides a single output period in I. BURST and E. BURST mode.
Auto: In NORM mode, all parameters can be automatically incremented or decremented with selectable resolution. Pushing the AUTO button activates the AUTO vernier, which then can be started with the selected vernier key. AUTO vernier stop is accomplished by an external trigger input or pushing AUTO.
Limit: Maximum high and low levels into 50 Ohm can be limited to protect the device under test. Pushing the limit key will set the limits to the actual levels, which then cannot be exceeded as long as the mode is active.
Compl: Switchselectable normal/complement output.
Disable: Relay disconnects all output circuitry.

CONTROL MODES (external voltage modulates output signal)

FM (frequency modulation)
Deviation: ± 5 % max
Sensitivity: 1 V for 1 % deviation
Modulation bandwidth: dc to 20 kHz (carrier frq. < 10MHz)
dc to 3kHz (carrier frq. > 10MHz)

AM (amplitude modulation)
Sensitivity: ± 2.5 V for 100 % modulation depth
+ 2.5 V, −7.5 V for DSBSC
Modulation bandwidth: dc to 1 MHz
Envelope distortion: < 1 % for modulation depth less than 90 % (dc to 50 kHz) NOT COMPL)

PWM (pulse width modulation)
Pulse width ratio: 10:1 max
Sensitivity: ± 6.5V typical for ratio 10:1.
Pulse width ranges: 10 ns to 1 s in eight nonoverlapping decade ranges

VCO (voltage controlled oscillator)
External voltage linearily sweeps 2 full frequency decades.
Modulation range: 1:100 with 0.1 V to 10 V
Modulation bandwidth: dc to 1 kHz

SUPPLEMENTARY PERFORMANCE CHARACTERISTICS

(Supplementary characteristics are intended to provide information useful in applying the instrument by giving non-warranted typical performance parameters).

AUXILIARY INPUTS AND OUTPUTS

Ext. Input: Threshold level: ± 10 V adjustable
Max input voltage: ± 20 V
Sensitivity: 500 mVpp
Min pulse width: 10 ns
Input impedance: 10 kOhm
Trigger slope: pos./neg. and trigger off

Control Input Max input voltage: ± 20 V
Input impedance: 10 kOhm

Trigger Output Output levels: 0/2.4 V into 50 Ohm
0/4.8 V into open
Output impedance: 50 Ohm

X-Output (Opt. 001 only): Increasing X-Output voltage with increasing sweep frequency. 0 V corresponds to start frequency and slope is 1.5 V/frequency decade. The max. output voltage is 10 V.

Marker Output (Opt. 001 only): TTL compatible voltage with positive transition at selected marker frequency.

Hold Input (Opt. 001 only): Main output will hold at the instantaneous voltage level when input signal becomes TTL high. Applicable for sine, triangle and square below 10 Hz.
Droop: 0.01 % of amplitude/s
Max input voltage: ± 20 V

HP-IB CAPABILITY

All modes and parameters can be programmed. The external input threshold level is not programmable.

Programming Times

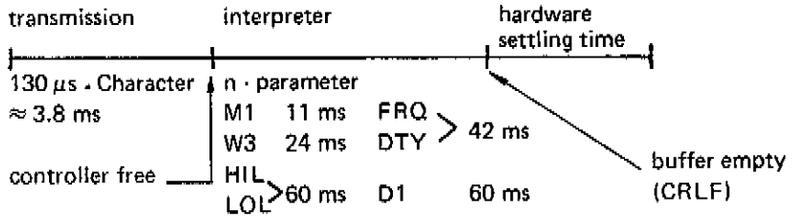
Listen (time for 8116A to receive and verify message)

Data transmission time: 130 µs per ASCII character.
Modes: 11 ms
Waveforms:  24 ms
330 ms

		in one string
DTY	60 ms	42 ms
FRQ	60 ms	
WID	24 ms	38 ms
HIL	110 ms	60 ms
LOL	100 ms	
AMP	150 ms	90 ms
OFS	150 ms	
ENABLE, DISABLE, LIMIT, NORM/COMPL	60 ms	

EXAMPLE:

"M1 W3 FRQ 1 KHz DTY 20 % HIL 3 V LOL 1 V D1"



Talk (time for 8116A to transmit a message)
Learn Mode, Error recognition: 1 ms/character.
Status: < 15 ms.

Settling Times (time to execute message)
Frequency, Duty Cycle, Width, Amplitude: 5 ms
Offset, DC Voltage: 30 ms

GENERAL

Warm-up Time: 15 min to meet all specifications
Environmental:
Storage temperature: –40°C to 70°C
Operating temperature: 0°C to 55°C
Accuracy Specifications apply from 15°C to 35°C.
Accuracy derating factor for temperatures outside this range: 1 + 0.05 x Δ°C.
Δ°C is the temperature deviation below 15°C and above 35°C.

Humidity Range: 95 % R.H., 0°C to 40°C.

Power-off storage: After eight hours of operation, battery maintains all current mode and parameter information up to half a year with instrument switched off.
Power: 100/120/220/240 V rms +5 %, –10 %; 48–440 Hz, 120 VA max.
Weight: Net 5.9 kg (13 lbs), Shipping 8.0 kg (18 lbs).
Dimensions: 89 mm high, 213 mm wide, 450 mm deep (3.5 x 8.4 x 17.7 in)

Options:
001 Burst, Sweep and Hold
910 Additional Operating and Service Manual (Part No.: 08116–90001).

SECTION II
INSTALLATION

2–1 INTRODUCTION

2–2 This section provides installation instructions for the instrument and its accessories. It also includes information about initial inspection and damage claims, preparation for use, and packaging, storage and shipment.

2–3 INITIAL INSPECTION

2–4 Inspect the shipping container for damage. If the container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. The contents of the shipment should be as shown in Figure 1–1 plus any accessories that were ordered with the instrument. Procedures for checking the electrical operation are given in Section 4. If the contents are incomplete, if there is a mechanical damage or defect, or if the instrument does not pass the operator's checks, notify the nearest Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement without waiting for settlement.

2–5 PREPARATION FOR USE

WARNING

To avoid hazardous electrical shock, do not perform electrical tests when there are signs of shipping damage to any portion of the outer enclosure (covers, panels, meters).

2–6 Power Requirements

2–7 The instrument requires a power source of 100/120/220 or 240 Vrms (+5 % – 10 %) at a frequency of 48–440 Hz single phase. The maximum power consumption is 120 VA.

2–8 ⚠ Line Voltage Selection

CAUTION

BEFORE SWITCHING ON THIS INSTRUMENT make sure that the instrument is set to the local line voltage. The line voltage selector switches an be seen through the lefthand side of the instrument cover to the rear. The correct setting for the country of destination will have been made at the factory. The instrument power fuse is located on the rear panel. To access the line selector switches, first DISCONNECT the power cord, then remove instrument top cover by releasing the captive securing screw at rear and sliding cover off.

CAUTION

Do not change the LINE SELECTOR switch settings with the instrument on or with power connected to the rear panel.

2–9 Figure 2–1 provides information for line voltage and fuse selection:

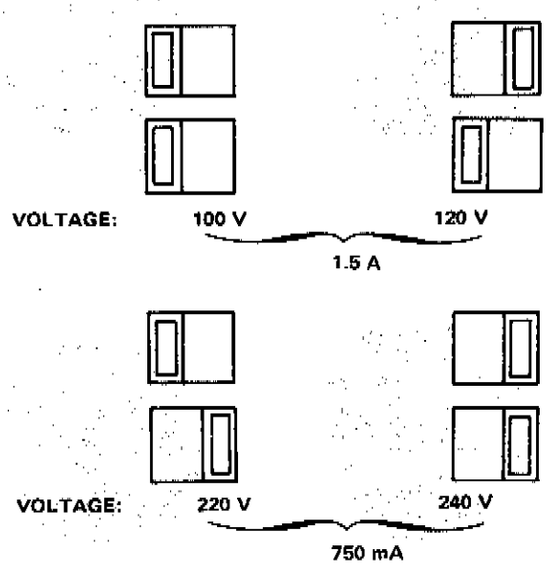


Figure 2–1. Sliding Switches Positions for different Line Voltages

2–10 Power Cable

WARNING

To avoid the possibility of injury or death, the following precautions must be followed before the instrument is switched on:

a. If this instrument is to be energized via an autotransformer for voltage reduction, make sure that the common terminal is connected to the grounded pole of the power source.

b. The power cable plug shall only be inserted into a socket outlet provided with a protective ground contact. The protective action must not be negated by the use of an extension cord without a protective conductor.

c. Before switching on the instrument, the protective ground terminal of the instrument must be connected to a protective conductor of the power cable. This is verified by checking that the resistance between the instrument chassis and the front panel and the ground pin of the power cable plug is zero ohms.

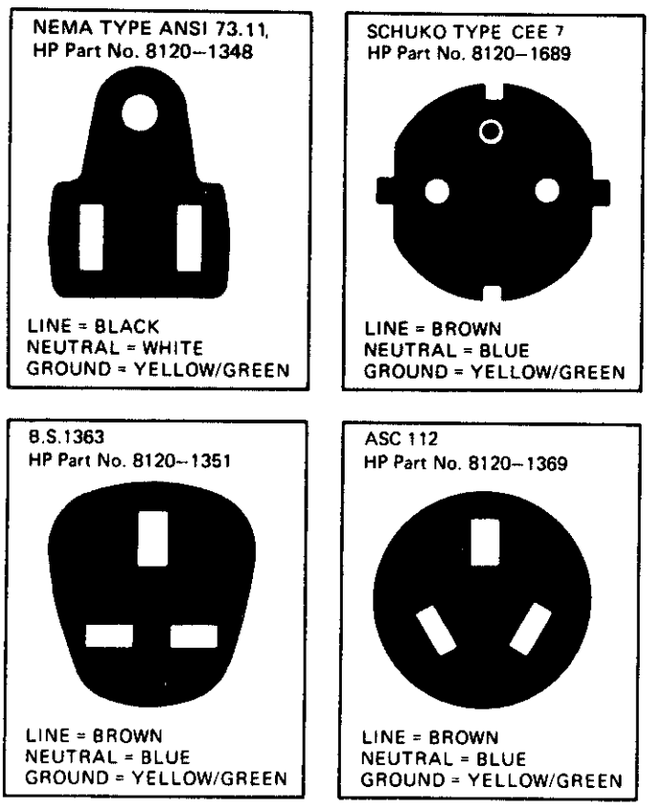


Figure 2–2. Power Cables Available: Plug Identification

2–11 In accordance with international safety standards, this instrument is equipped with a three-wire power cable. When connected to an appropriate ac power receptacle, this cable grounds the instrument cabinet. The type of power cable shipped with each instrument depends on the country of destination. Refer to Figure 2–2 for the part number of the power cords available.

2–12 The following work should be carried out by a qualified electrician and all local electrical codes must be observed. If the plug on the cable supplied does not fit your power outlet, or if the cable is to be attached to a terminal block, then cut the cable at the plug end and re-wire it. The colour coding used in the cable will depend on the cable supplied (see Figure 2–2). If a new plug is to be connected, the plug should meet local safety requirements and include the following features:

adequate load-carrying capacity (see table of specifications in Section 1)

ground connection

cable clamp

2–13 HP-IB Connector

2–14 The rear panel HP-IB connector (Figure 2–3) is compatible with the connectors on Cable Assemblies 10833A, B, C and D. If a cable is to be locally-manufactured, use connector male, HP part number 1251–0293.

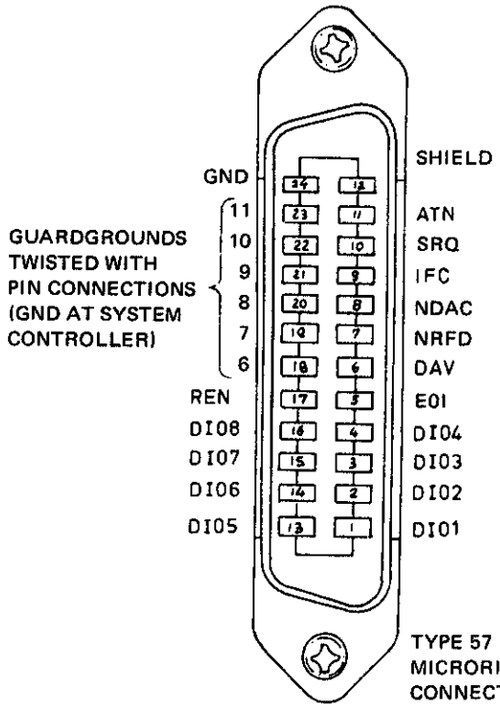


Figure 2–3. HP-IB Connector

2–15 HP-IB Logic Levels

2–16 The 8116A HP-IB lines use standard TTL logic. Logic levels are as follows:

True = low = digital ground or 0V dc to +0.4V dc,
False = high = open or +2.5V dc to +5V dc.

All HP-IB lines have LOW assertion ("1") states. High states are held at +3V dc by pullups within the instrument. When a line functions as an input, approximately 3.2mA of current is required to pull it low through a closure to digital ground. When a line functions as an output, it will sink up to 48mA in the low state and approximately 0.6mA in the high state.

CAUTION

Isolation. The HP-IB line screens are not isolated from outer chassis (frame) ground.

2–17 Operating Environment

The operating temperature limits are 0°C to 55°C. The specifications also apply over this temperature range.

2–18 CLAIMS AND REPACKAGING

2–19 Claims for Damage

2–20 If physical damage is evident or if the instrument does not meet specification when received, notify the carrier and the nearest Hewlett-Packard Sales/Service Office. The Sales/Service Office will arrange for repair or replacement of the unit without waiting for settlement of the claim against the carrier.

2–21 Storage and Shipment

2–22 The instrument can be stored or shipped at temperatures between −40°C and 75°C. The instrument should be protected from temperature extremes which cause condensation within it.

2–23 If the instrument is to be shipped to a Hewlett-Packard Sales/Service Office, attach a tag showing owner, return address, model number and full serial number and the type of service required. The original shipping carton and packaging material may be re-usable but the Hewlett-Packard Sales/Service office will also provide information and recommendations on materials to be used if the original packing is not available or re-usable. General instructions for re-packing are as follows:

1. Wrap instrument in heavy paper or plastic.

2. Use strong shipping container. A double wall carton made of 350-pound test material is adequate.

3. Use enough shock-absorbing material (3 to 4-inch layer) around all sides of instrument to provide firm cushion and prevent movement inside container. Protect control panel with cardboard.

4. Seal shipping container securely.

5. Mark shipping container FRAGILE to encourage careful handling.

6. In any correspondence, refer to instrument by model number and serial number.

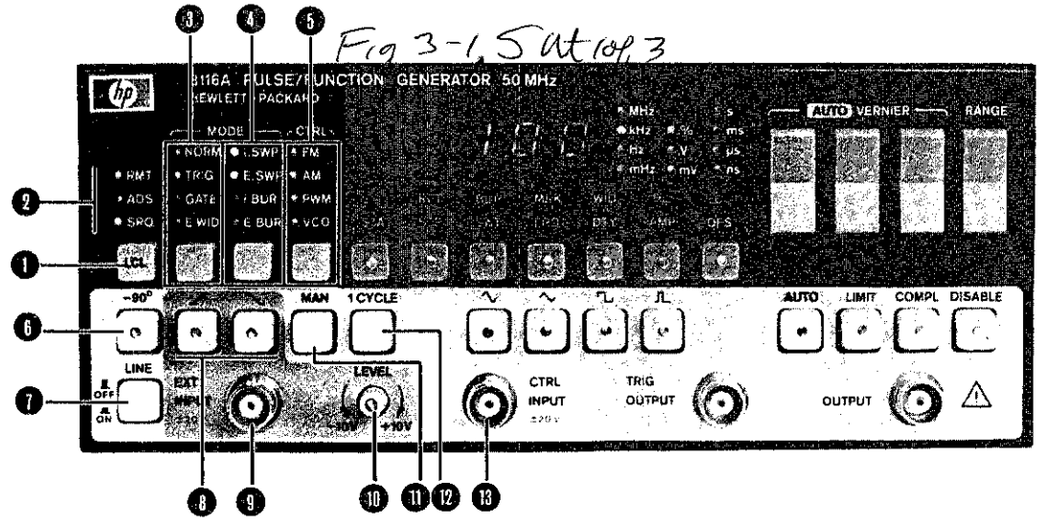


Figure 3–1. Controls and Indicators (Option 001 included)

OPERATING AND CONTROL MODE SELECTION

1 This pushbutton returns the 8116A to local manual operation. (NOTE: Pushbutton disabled when LOCAL LOCKOUT command sent by the controller to the 8116A).
In local mode pressing this pushbutton causes the currently selected HP-IB address to be displayed.

2 Program status LEDs. When illuminated, they indicate the following:

- RMT: Indicates REMOTE control and all frontpanel pushbuttons are disabled (except LCL).
- ADS: Indicates that the 8116A is being ADDRESSED under program control, although frontpanel pushbuttons may be operational depending on wether the RMT LED is lit or unlit.
- SRQ: Indicates that the SERVICE REQUEST has been sent to the controller.

3 Standard mode selection pushbutton and associated LEDs. Repetitive operation of this pushbutton steps through the modes in the sequence indicated by the LED column.
The modes are as follows:

- NORM: NORMAL mode with internal rate generator freerunning.
- TRIG: A TRIGGER signal, either at the EXT INPUT connector or via the MANUAL pushbutton, initiates one output pulse.
- GATE: A GATE signal, either at the EXT INPUT connector or via the MANUAL pushbutton, generates an output for the duration of that signal.
- E.WID: (Pulse waveform only). The EXTERNAL WIDTH mode allows the signal applied to the EXT INPUT to be shaped in order to determine output pulse width and period.

4 Option mode selection pushbutton and associated LEDs. Repetitive operation steps through the modes in the same sequence as the LED column. The modes are as follows:

- I.SWP: INTERNAL SWEEP. Continuous sweep cycles between the selected start and stop frequency. Frequency increment is logarithmic. Sweep direction always upwards.
- E.SWP: EXTERNAL SWEEP. A trigger signal, either at the EXT INPUT connector or via the MANUAL pushbutton, generates a single sweep between the start and stop frequencies. (Further triggering details are given later in this section under External Triggering/MANUAL descriptions).
- I.BUR: (Pulse waveform excluded). INTERNAL BURST. Preselected number of cycles (1 to 1999) generated continuously. Time between bursts set via RPT key.
- E.BUR: (All waveforms). EXTERNAL BURST. A burst trigger, either at the EXT INPUT connector or via the MANUAL pushbutton, generates a preselected number of output cycles (1 to 1999).

5 Control mode select pushbutton and associated LEDs. Repetitive operation steps through the modes in the same sequence as the LED column. The modes are as follows:

- FM: FREQUENCY MODULATION mode. The 8116A's output can be frequency modulated by applying a voltage to the frontpanel CONTROL INPUT connector.
- AM: AMPLITUDE MODULATION mode. The 8116A's output can be amplitude modulated by applying a voltage to the frontpanel CONTROL INPUT connector.
- PWM: PULSE WIDTH MODULATION mode. The 8116A's output can be pulse width modulated by applying a voltage to the frontpanel CONTROL INPUT connector.
- VCO: VOLTAGE CONTROLLED OSCILLATOR mode. In this mode, a signal applied to the CONTROL INPUT connector determines the 8116A output frequency.

6 Phase pushbutton. In TRIG, GATE and optional BURST modes the start phase may be shifted through −90 degrees in sine or triangle generation using this pushbutton. Haversine or havertriangle can thus be generated.

7 LINE switch. Power on/off pushbutton.

8 TRIGGER SLOPE pushbuttons. In external triggering modes, the trigger slope of the signal applied to the EXT INPUT connector is selected using these pushbuttons. The currently selected slope is indicated by an illuminated pushbutton LED.

9 EXTERNAL INPUT connector. BNC connector for external trigger signals.

10 LEVEL adjust. Enables the external input trigger level to be adjusted in the range −10 V to 10 V.

11 MANUAL pushbutton. Used to simulate an external trigger signal. In optional sweep modes, it starts a single sweep cycle and resets from stop frequency to start frequency.

12 1 CYCLE pushbutton. (Opt. 001). Pressing this pushbutton generates a single output period in I.BURST and E.BURST modes.

13 CONTROL INPUT connector. BNC connector for external control signals.

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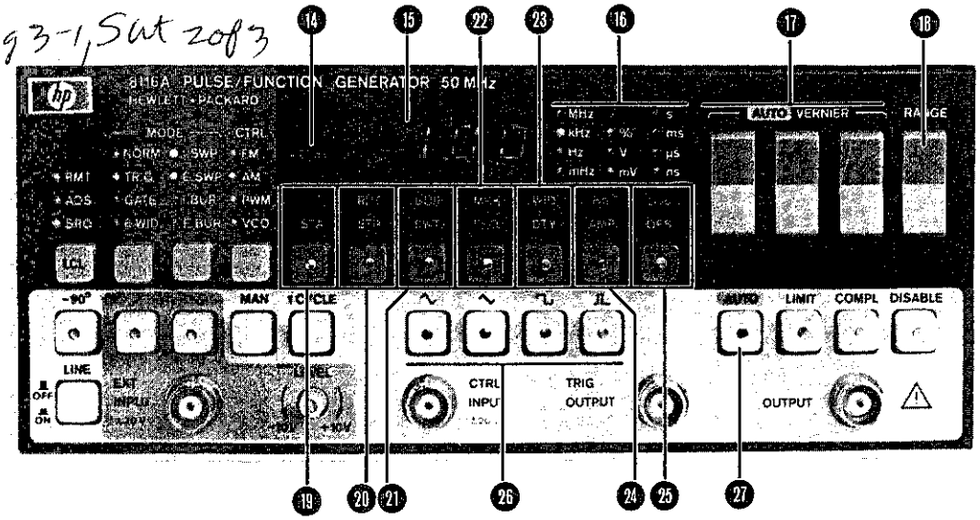
Fig 3-1, Sht 2 of 3



PARAMETER/WAVEFORM SELECTION

14 ERROR LED. Indicates erroneous mode settings and incompatible timing settings.

15 Digital display. Indicates numerical value of currently displayed parameter.

16 Units LEDs. Indicates in which units the currently displayed parameter is measured.

17 VERNIER rocker keys. Used to vary parameter values.

18 RANGE rocker key. Used to change the range of the currently selected parameter.

19 to **25** Parameter selection pushbuttons and their associated mnemonics. On pressing a pushbutton, the built-in LED illuminates and the current value of the selected parameter becomes displayed. For each pushbutton, the selected parameter is indicated by an illuminated mnemonic (automatically controlled by the 8116A). Once selected, the parameter value can be varied via the RANGE/VERNIER keys. Individual details of each pushbutton are given in the following:

19 (Option 001). Only active in sweep modes, and selects sweep start frequency (STA) parameter for display and setting.

20 (Option 001). Selected mode determines mnemonic illumination, hence parameter selection. Mnemonics are:

RPT: REPEAT is illuminated to indicate that the "time between bursts" is currently selectable.
or STP: STOP is illuminated to indicate that "sweep stop frequency" is currently selectable.

21 (Option 001). Selected mode determines mnemonic illumination, hence parameter selection. Mnemonics are:

BUR: BURST. Illuminated to indicate that "burst number" is currently selectable.
or SWT: SWEEP TIME. Illuminated to indicate that SWEEP TIME is currently selectable.

22 Selected mode determines mnemonic illumination, hence parameter selection. Mnemonics are:

MRK: MARKER (Opt. 001). Only illuminated in sweep modes to indicate that "sweep marker frequency" is currently selectable.
or FRQ: FREQUENCY. Illuminated in all modes, except sweep modes, to indicate that "frequency" is currently selectable.

23 Selected waveform determines mnemonic illumination hence parameter selection. Mnemonics are:

WID: WIDTH. Illuminated with pulse waveforms selected to indicate that "width" is currently selectable.
or DTY: DUTY CYCLE. Illuminated when sine, triangle (ramp) or squarewave is selected to indicate that "duty cycle" is currently selectable. (RANGE key and lefthand VERNIER key inactive).

24 Parameter selection is user-dependent. Pressing pushbutton once selects parameter indicated by currently illuminated mnemonic. Pressing the illuminated pushbutton a second time changes parameter selection (mnemonic illumination) e.g. HIGH LEVEL (HIL) to AMPLITUDE (AMP) or vice-versa.

25 Parameter selection is user-dependent. Pressing pushbutton once selects parameter indicated by currently illuminated mnemonic. Pressing the illuminated pushbutton a second time changes parameter selection (mnemonic illumination) e.g. LOW LEVEL (LOL) to OFFSET (OFS) or vice-versa.

26 Waveform pushbuttons. Select the desired waveform to be generated by the 8116A output. The currently selected waveform is indicated by an illuminated pushbutton LED. Pressing the illuminated pushbutton a second time switches waveforms off for d.c. mode.

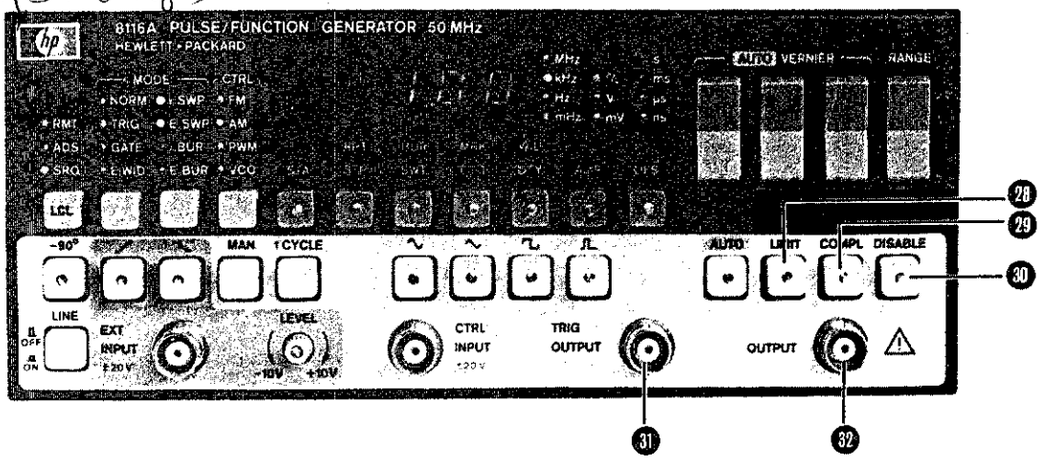
27 AUTO pushbutton. In NORM mode only, all parameters can be automatically incremented or decremented with selectable resolution. Pushing the AUTO pushbutton activates the AUTO VERNIER, which can then be started with the selected VERNIER key. Any of 3 conditions causes an AUTO VERNIER "wait" state i.e. AUTO VERNIER active, but no increment/decrement takes place. The conditions are:

1. Timing error exists.
2. At instrument specification limits e.g. frequency 50 MHz.
3. At output level limits set via the LIMIT key.

AUTO VERNIER switch-off is accomplished by any of the following:

1. External trigger input.
2. Pressing any key other than the VERNIER keys.
3. Pressing the AUTO key.

Fig 3-1, Sht 3 of 3



OUTPUT CONTROLS / CONNECTORS

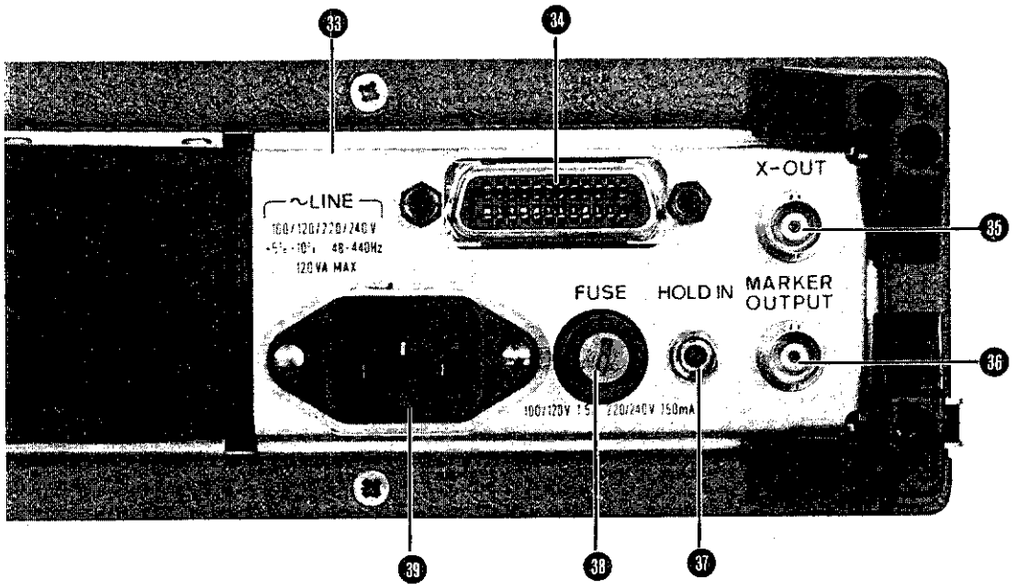
28 LIMIT pushbutton. Maximum high (HIL) and low (LOL) levels into 50 Ohm can be limited to protect the device under test. Pushing the LIMIT key sets the limits to the currently active levels, which cannot be exceeded as long as the LIMIT key is active (pushbutton LED illuminated).

29 COMPLEMENT pushbutton. Provides switch-selectable normal/complement output. When pushbutton LED is illuminated, output is complement.

30 DISABLE pushbutton. Pressing this pushbutton disables the 8116A output. (Disable state indicated by illuminated LED).

31 TRIG OUTPUT connector. BNC connector for providing a trigger output signal.

32 OUTPUT connector. BNC connector for providing the 8116A output signal.



REAR PANEL CONTROLS / CONNECTORS

33 HP-IB device address switch (5 bits A1 to A5).

34 HP-IB connector.

35 X-OUTPUT connector (Opt. 001). Delivers increasing output voltage with logarithmically increasing frequency in sweep mode. 0 V corresponds to start frequency, and slope is 1.5 V/frequency decade. The maximum output voltage is 10 V.

36 MARKER OUTPUT connector (Opt. 001). Provides a TTL compatible voltage with positive-going step at the selected marker frequency in sweep mode.

37 HOLD INPUT connector (Opt. 001). An input signal at this connector causes the 8116A output to hold at that voltage instantaneous to the input signal attaining TTL high. Applicable for sine, triangle and squarewave below 10 Hz.

38 FUSE. Accepts standard fuses to provide instrument protection in case of current overload. A 750 mA slow-blow fuse must be used when operating from a 220/240 V power source. A 1.5 A fuse is used when operating from a 100/120 V power source.

39 LINE. A three pronged receptacle to provide chassis ground through the power cable for operator protection.

SECTION III
OPERATING AND PROGRAMMING

3–1 INTRODUCTION

3–2 The following operating information explains the functions of the controls and indicators of the Model 8116A Pulse/Function Generator. Front and rear panel controls, indicators and connectors are identified and briefly described in Figure 3–1, which should be read before continuing with the following description. Programming information is given at the end of this section.

3–3 SPECIAL OPERATING CONSIDERATIONS ⚠

3–4 Read the following four notes before applying power to the Model 8116A.

1. Read the Safety Summary at the beginning of this manual.

2. Ensure the power selector switches are set properly for the power source being used to avoid instrument damage. This can be done by checking the line selection label on the rear panel.

CAUTION: Do not change the LINE SELECT switch setting with the instrument on or with power connected to the rear panel.

3. Ensure that load cannot be overdriven by the 8116A output (16 Vpp into 50 Ω; 32 Vpp into high impedance).

4. Do not apply an external voltage or electrostatic discharge (ESD) to the output connectors.

3–5 OPERATOR'S CHECKS

3–6 The 8116A performs a 'self check' at power switch-on. During this check, all LED's should be momentarily lit. In the event of a fault, an error code appears in the 8116A frontpanel digital display. The error codes are as follows:

⊏⊐ –	Indicates that a frontpanel key is jammed in the despressed position.
E11–	Indicates a fault by Auto Vernier/ External Sweep Trigger
E21–	Indicates a fault in the internal rep. rate generator
E31–	Indicates a fault in the internal width circuits. The width setting in pulse mode and the 'time between bursts' in I.BUR mode are affected.
E41/42–	Indicates an output amplifier fault.
E51-E62	Error indications for dedicated service tests.

3–7 OPERATING INSTRUCTIONS

3–8 Operating modes and parameters can be set on the frontpanel (local operation) or programmed using the HP-IB. The current operating mode is indicated by an illuminated LED in the MODE column on the frontpanel. Parameter selection for the 8116A digital display is indicated by an illuminated pushbutton LED. Similarly, current output waveform is also indicated by an illuminated pushbutton LED.

3–9 At power switch-on, the 8116A performs a self-test and automatically assumes the operating state prevailing at switch-off with the output disabled (DISABLE key LED lit) to protect externally connected devices. The operator should then select the required mode (NORM, TRIG, GATE, E.WID or an Opt. 001 mode when available) and output waveform. Upon selection, the 8116A automatically displays the parameters (mnemonically e.g. FRQ, DTY, AMP, OFS) which can be set within this mode. Parameter keys other than those which select the displayed parameters are not operational.

3–10 Pressing a parameter key then calls the current value of that parameter into the 8116A digital display, and a new value can be set using the RANGE and VERNIER keys. When all parameters are set to the required values, the DISABLE key should then be pressed to enable the output (key LED no longer illuminated).

3–11 In addition to the operating modes, the 8116A offers 4 control modes for modulating or controlling the output signal i.e. FM, AM, PWM, VCO. Table 3–1 shows which control mode can be combined with which operating mode. In the event of the operator selecting an erroneous combination e.g. E.WID and FM, the 8116A automatically displays ERROR and the E.WID and FM LED's will flash. Similarly, in NORM mode, when the operator makes incompatible timing settings (e.g. width greater than frequency) the 8116A displays ERROR.

Table 3–1. Operating/Control Mode Combinations

Mode / Modulate	NORM	TRIG	GATE	E.WID	I.SWP	E.SWP	I.BUR	E.BUR
FM	•	•	•	–	•	•	•(2)	•
AM	•	•	•	•(1)	•	•	•(2)	•
PWM	•(1)	•(1)	•(1)	–	•(1)	•(1)	–	•(1)
VCO	•	•	•	–	–	–	•	•

• = All waveforms
•(1) = Pulse waveform only
•(2) = All waveforms except pulse
– = Error combination

3–12 PARAMETERS

3–13 Figure 3–2 (Timing) and Figure 3–3 (Output Levels) illustrate the output signal parameters of the standard 8116A. A description of the various parameter-setting controls is given in Figure 3–1.

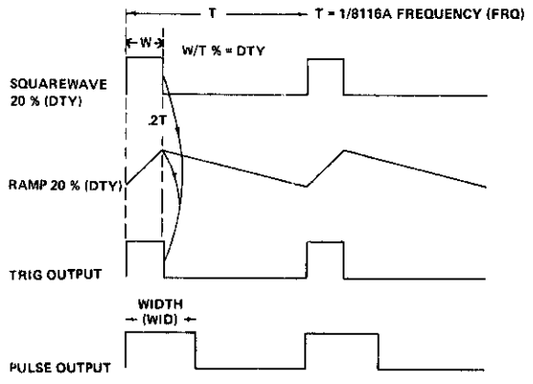


Figure 3–2. Timing Parameters

Figure 3–3. Output Level Parameters

3–14 As described in Figure 3–1, the parameter selection of the amplitude/offset keys is user-dependent. With any change to the HIL or LOL settings, the 8116A automatically calculates and stores the new amplitude and offset values.

3–15 Option 001 mode parameters are explained and illustrated under the respective mode description.

3–16 VERNIER / RANGE OPERATION

3–17 The vernier comprises 3 rocker-switches corresponding to the 3 display digits. Incrementing/decrementing a display digit is accomplished by pressing the upper/lower switch section respectively. (Continuous pressing causes continuous increment/decrement of the related display digit).

3–18 The RANGE key is also a rocker-switch for multiplying/dividing the displayed value by factor 10. For the offset parameter, pressing the key twice provides a quick means of setting 0 V.

3–19 AUTO VERNIER OPERATION

3–20 In NORM mode only, all parameters can be automatically incremented/decremented with selectable resolution. To activate AUTO VERNIER operation, first select the parameter to be incremented/decremented, then press the AUTO key. AUTO VERNIER can now be started by pressing any of the VERNIER keys.

3–21 There are 3 conditions, any of which causes an AUTO VERNIER 'wait' state i.e. AUTO VERNIER active (key LED lit), but no increment/decrement takes place. The conditions are:

1. timing error exists
2. at instrument specification limits e.g. frequency 50 MHz
3. at output level limits set via the LIMIT key.

AUTO VERNIER switch-off is accomplished by any of the following:

1. external signal to the EXT INPUT connector
2. pressing any key other than the vernier keys
3. pressing the AUTO key.

3–22 LIMIT OPERATION

3–23 Maximum high (HIL) and low (LOL) levels into 50 Ohm can be set to protect the device under test. Pushing the LIMIT key sets the currently active high and low levels as the 8116A output limits – which cannot be exceeded as long as LIMIT operation is active (key LED lit).

3–24 EXTERNAL TRIGGERING

3–25 Five pushbuttons, a trigger level adjust and BNC connector (EXT INPUT) facilitate external triggering of the 8116A. The function of the individual pushbuttons in the various external triggering modes is described in the following.

3–26 –90°

3–27 With TRIG, GATE or E.BUR (Opt. 001) mode selected, and output waveform set to sine or triangle, pressing this pushbutton shifts the start phase to –90°. As a result, haversine and havertriangle signals can be generated by the 8116A.

3–28 Trigger Slopes

3–29 Positive or negative slope is selectable for triggering on the signal applied to the EXT INPUT connector. With no slope selected (both key LED's off), the EXT INPUT is switched off.

3–30 Triggering level on the selected slope is set via the LEVEL adjust.

3–31 Note that in E.SWP mode (Opt. 001), two trigger pulses may be required. If the 8116A is not set to the start frequency (STA) i.e. STA key LED not illuminated, the first trigger pulse sets the 8116A to the STA frequency. The second trigger pulse then starts the sweep.

3–32 MANUAL

3–33 In external trigger modes, the 8116A can be triggered manually via the MAN pushbutton:

TRIG Mode. Each operation of the MAN key generates one output cycle, cycle time being determined by the 8116A frequency setting.

GATE Mode. The 8116A outputs continuously for as long as the MAN key is depressed. Frequency is determined by the 8116A frequency setting.

E.SWP Mode (Opt. 001). MAN key operation starts the sweep only if the 8116A is set to the start frequency (STA) i.e. STA key LED illuminated. Otherwise, MAN key must be pressed twice; the first time to reset the 8116A to STA, the second to start the sweep.

E.BUR Mode (Opt. 001). Each operation of the MAN key triggers a burst output.

3–34 1 CYCLE (OPTION 001)

3–35 In E.BUR and I.BUR modes, each operation of this key generates a single cycle at the 8116A output.

3–36 STANDARD PARAMETER SET

3–37 The Standard Parameter Set is available for two reasons. Firstly it serves to overcome RAM corruption, should it occur as a result of battery charge deterioration, by giving an error-free display at switch-on. Secondly, when incompatible mode selection causes an error condition (i.e. E.WID and Sine), the instrument may be switched OFF then ON again to revert to the Standard Parameter Set, thus overcoming any condition previously displayed. The Standard Parameter Set is as follows:

NORM	ON
FRQ (active)	1.00 kHz
DTY	50 %
HIL	+0.5 V
LOL	–0.5 V
	ON

Selecting I.SWP mode gives:

STA	1.00 kHz
STP	100 kHz
SWT	50 ms
MRK	1.00 kHz
DTY	50 %
HIL	+0.5 V
LOL	–0.5 V

Selecting I.BUR mode gives:

RPT . . . . . 100 ms
BUR 1
FRQ . . . . . 1.00 kHz
DTY . . . . . 50 %
HIL . . . . . +0.5 V
LOL . . . . . −0.5 V

Selecting E.BUR withdraws the RPT parameter from the display mnemonics.

Selecting Pulse mode makes WID available (500 µs).

The Standard Parameter Set can be accessed when the 8116A is operating on the HP-IB by sending the command:
CLR 7 (BASIC) CLEAR 7 (HPL)

3–38 CONTROL MODES

3–39 The 8116A output signal can be modulated (AM, FM, PWM) or controlled (VCO) by applying a signal to the CTRL INPUT connector. Table 3–1 indicates the permitted operating mode/control mode combination, a brief description of each control mode being given in the following. For specification details in each mode – see Table 1–2.

3–40 FREQUENCY MODULATION (FM)

3–41 The 8116A's output can be frequency modulated by applying a signal to the CTRL INPUT connector.

3–42 AMPLITUDE MODULATION (AM)

3–43 The 8116A's output can be amplitude modulated by applying a signal to the CTRL INPUT connector. A ground symmetrical modulating signal provides a modulation of 0–100 %. 200 % modulation (DSBSC) can also be obtained. Figure 3–4 illustrates 100 % modulation and DSBSC.

3–44 PULSE WIDTH MODULATION (PWM)

3–45 In pulse mode, the 8116A's output can be pulse width modulated by applying a signal to the CTRL INPUT connector. Pulse width modulation is available in any one of 8 non-overlapping decade ranges, as illustrated in Figure 3–5.

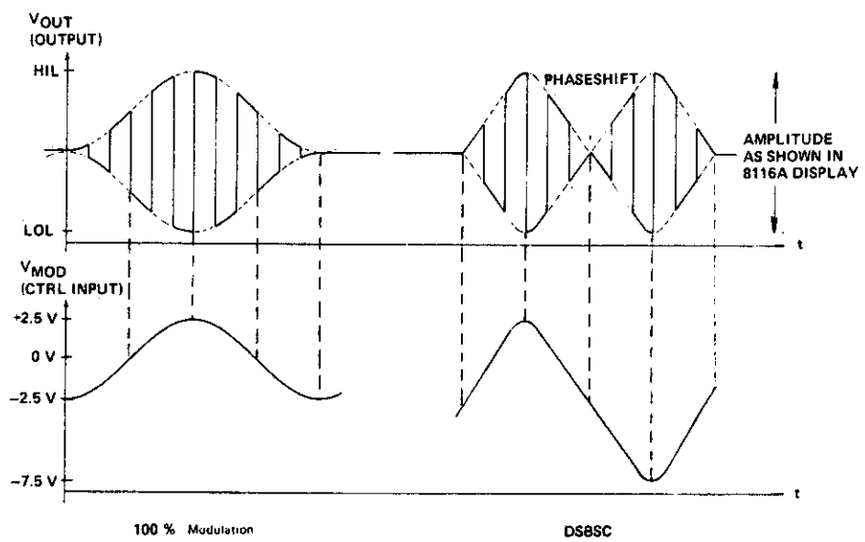


Figure 3–4. Amplitude Modulation

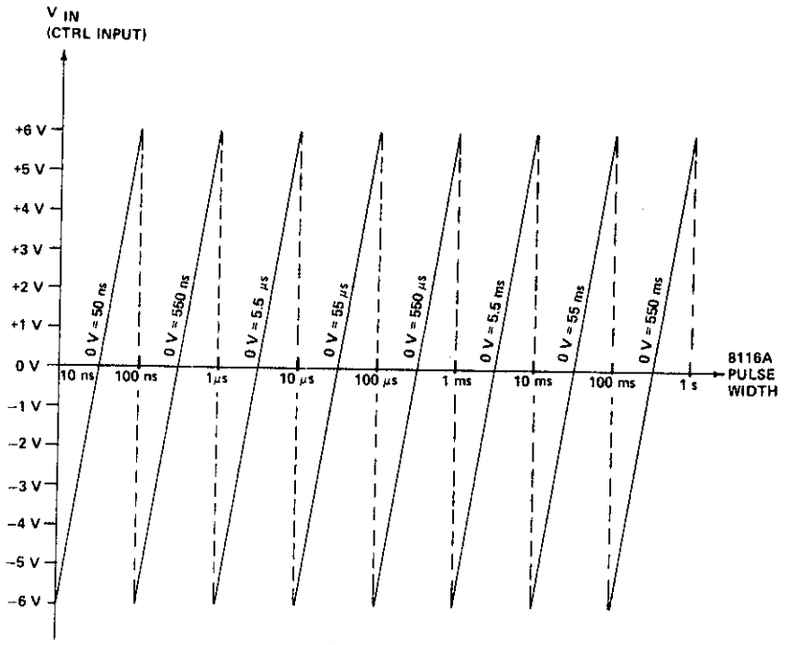


Figure 3–5. PWM Characteristics

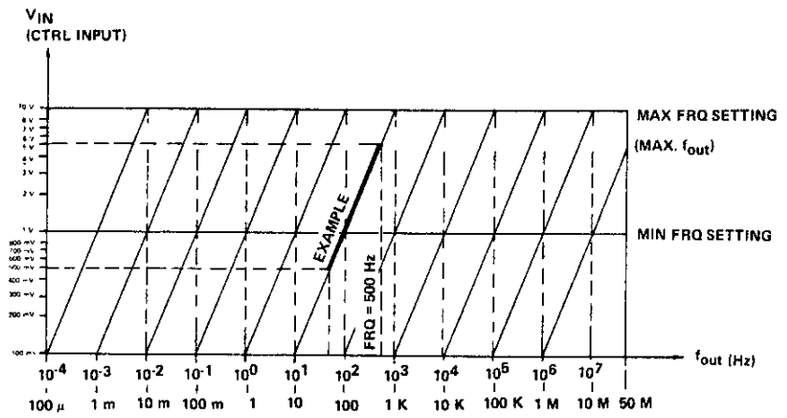


Figure 3–6. VCO Characteristics

3–46 VOLTAGE CONTROLLED OSCILLATOR (VCO)

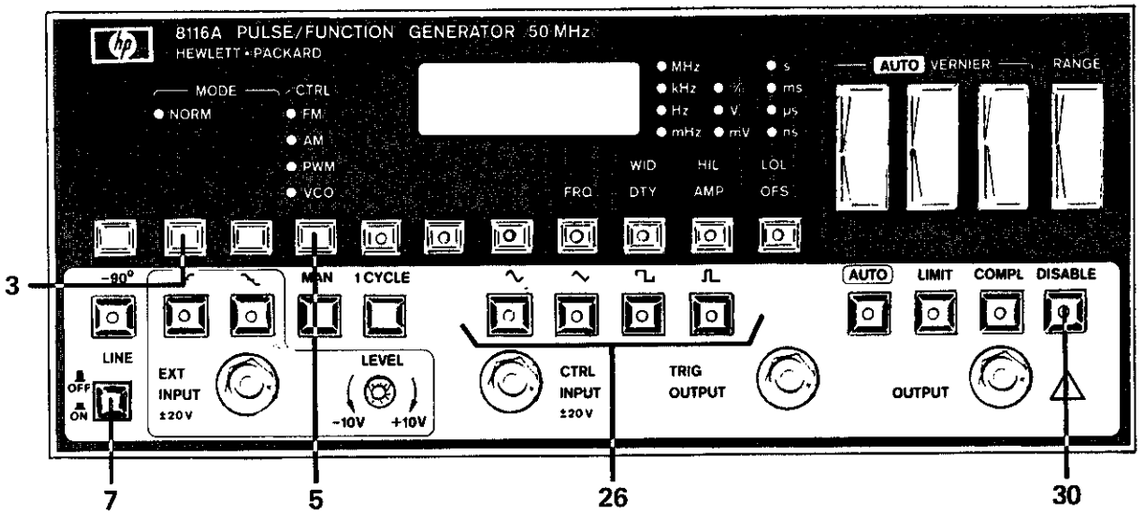
3–47 In this mode, a signal applied to the CTRL INPUT connector determines the output frequency. Output frequency range is a maximum 1:100 as shown in Figure 3–6.

Range selection is automatically determined by the 8116A frequency (FRQ) setting, the selected range being that whose upper decade brackets the FRQ setting. Figure 3–6 gives a range selection example for an FRQ setting of 500 Hz.

3–48 OPERATING MODES

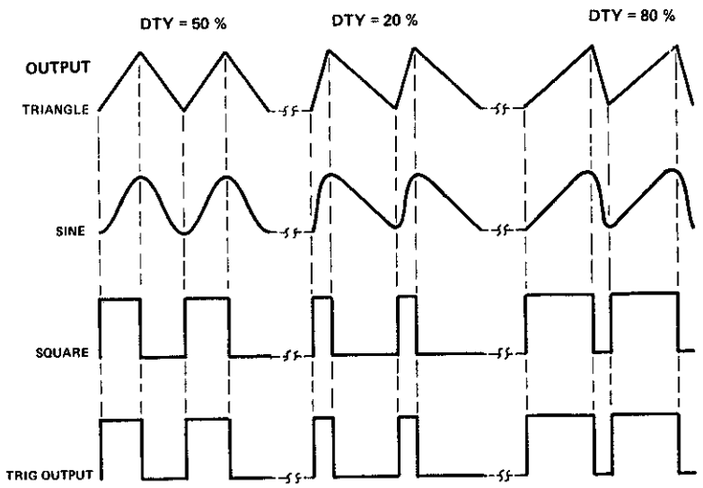
3–49 Each of the 8 operating modes (standard and Opt. 001) is described briefly. For each mode, a short procedure is given to aid quick mode entry together with timing diagrams to illustrate the various outputs in the described mode. Each 8116A operating mode illustration highlights the parameter mnemonics, hence parameter settings for the presented mode.

NORM MODE

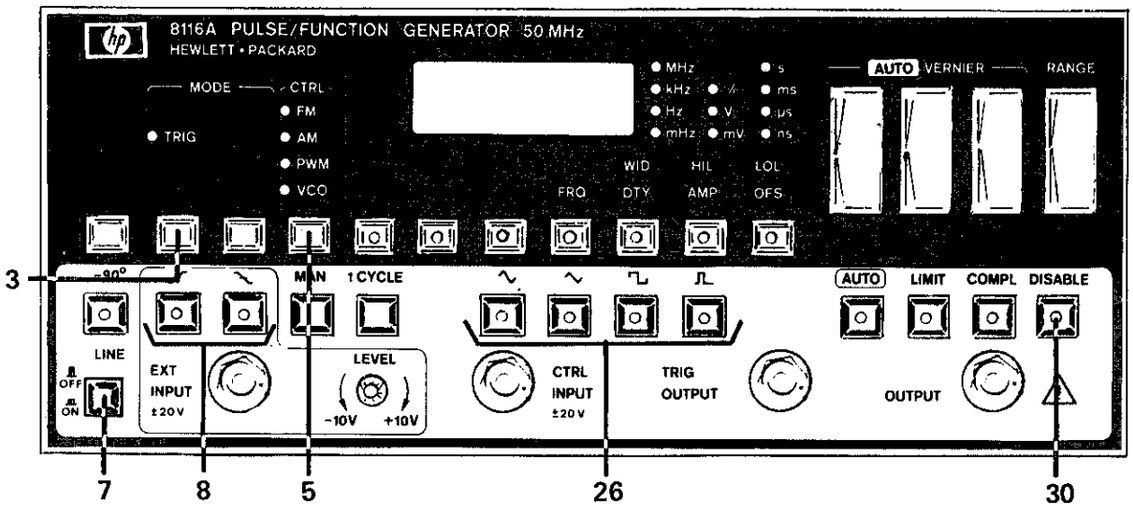


NOTE: For parameter specifications, see Table 1–2.

1. Set the LINE switch (7) to the ON position.
2. Select NORM mode (if necessary) via key (3). Standard modes are stepped-through by repetitive operation of this key.
3. Select the desired waveform at row (26). The parameter menu will automatically be illuminated as shown above (WID only illuminated if pulse waveform selected; also, although HIL, LOL, AMP and OFS can all be selected, only HIL/LOL or AMP/OFS will be illuminated at any one point in time – see Figure 3–1 description).
4. Select each parameter, in turn, via its associated key, and set it to the desired value using the RANGE/VERNIER keys and the digital display.
5. If a modulated output is required, select the desired modulation via key (5), and apply the modulating signal to the CTRL INPUT connector.
6. Press key (30) to enable the 8116A output. Key LED should no longer be illuminated. The following timing diagram illustrates the outputs in NORM mode.



TRIG MODE



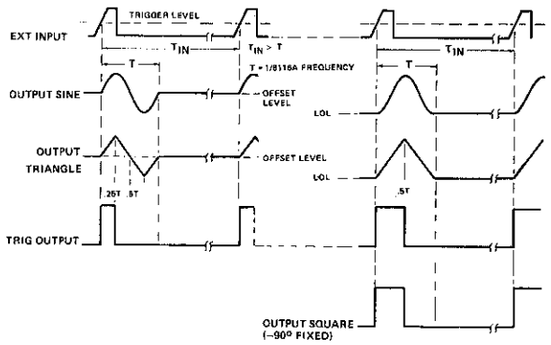
NOTE: For parameter specifications, see Table 1–2.

1. Set the LINE switch (7) to the ON position.
2. Select TRIG mode via key (3). Standard modes are stepped-through by repetitive operation of this key.
3. Select the desired waveform at row (26). The parameter menu will automatically be illuminated, this being a combination of those shown above, e.g. WID only illuminated if pulse waveform selected.
4. Select each parameter, in turn, via its associated key, and set it to the desired value using the RANGE/VERNIER keys and the digital display. Note that the frequency setting should be set less than the frequency of the trigger signal.
5. If triggering is by an external signal, select the trigger slope at (8), and apply the trigger signal to the EXT INPUT connector. Triggering can also be simulated by press the MAN key.
6. If a modulated output is required, select the desired modulation via key (5), and apply the modulating signal to the CTRL INPUT connector.
7. Press key (30) to enable the 8116A output. This key LED should no longer be illuminated. The following timing diagrams illustrate some outputs in TRIG mode.

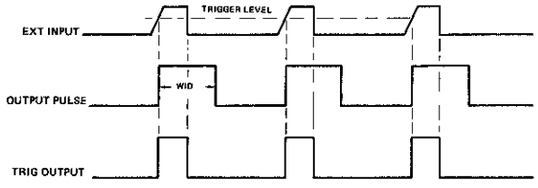
FUNCTIONS

0° START PHASE (DTY = 50 %)

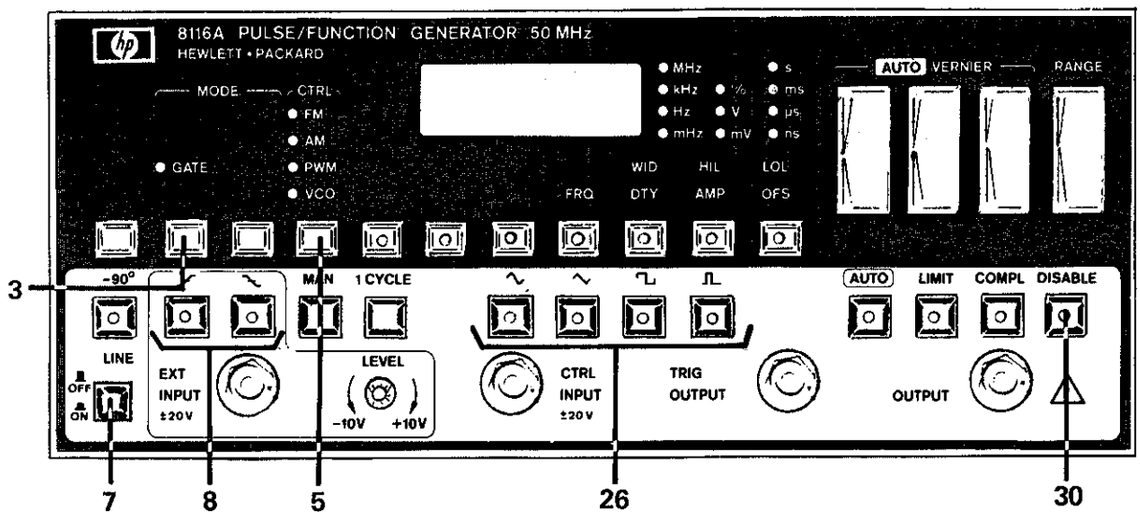
−90° START PHASE (DTY = 50 %)



PULSE



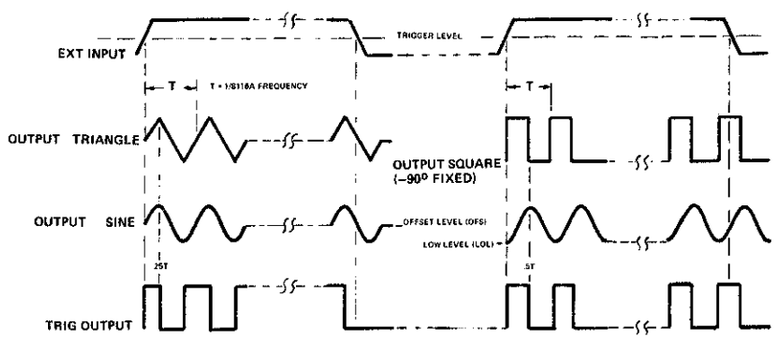
GATE MODE



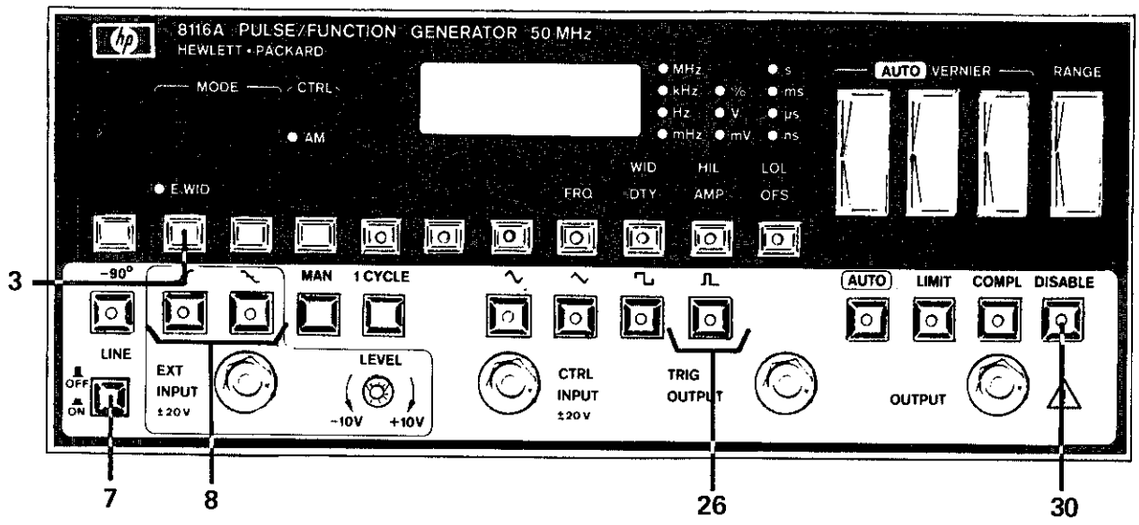
NOTE: For parameter specifications, see Table 1–2.

1. Set the LINE switch (7) to the ON position.
2. Select GATE mode via key (3). Standard modes are stepped — through by repetitive operation of this key.
3. Select the desired waveform at row (26). The parameter menu will automatically be illuminated, this being a combination of those shown above e.g. WID only illuminated if pulse waveform selected.
4. Select each parameter, in turn, and set it to the desired value using the RANGE/VERNIER keys and the digital display.
5. If gating by an external signal, select the trigger slope at (8), and apply the gate signal to the EXT INPUT connector.
6. If a modulated output is required, select the desired modulation via key (5), and apply the modulating signal to the CTRL INPUT connector.
7. Press key (30) to enable the 8116A output. This key LED should no longer be illuminated. The following timing diagrams illustrate some outputs in Gate mode.

0° START PHASE **–90° START PHASE**

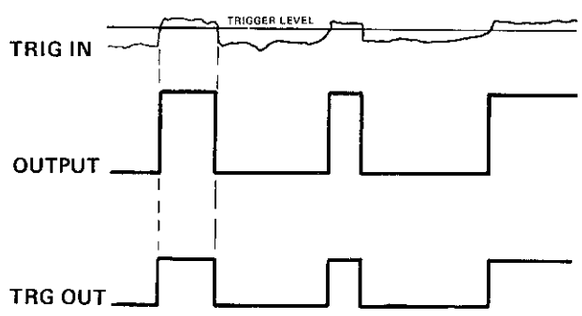


E.WID

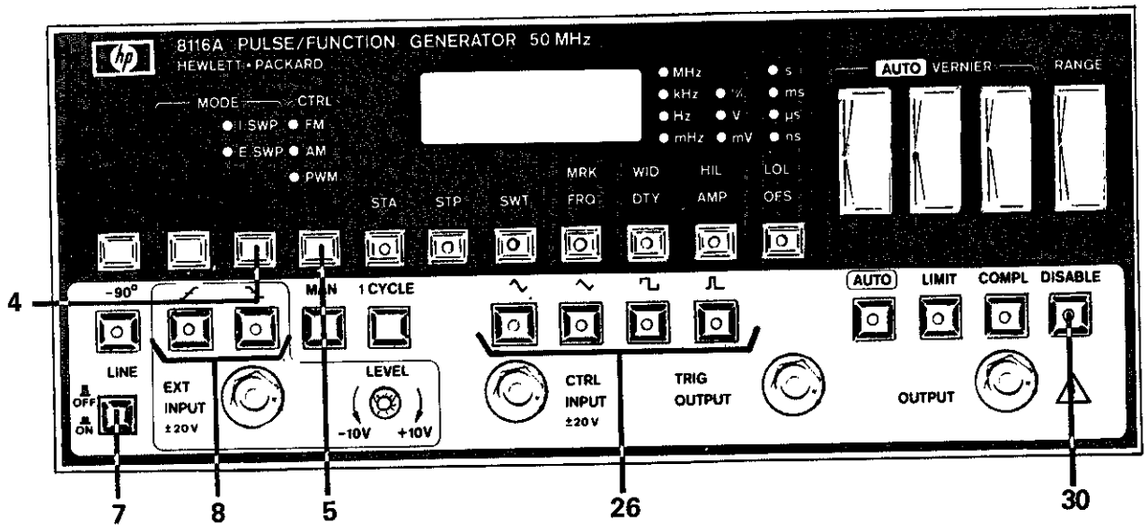


NOTE: For parameter specifications, see Table 1–2.

1. Set the LINE switch (7) to the ON position.
2. Select E.WID mode via key (3). Standard modes are stepped — through by repetitive operation of this key.
3. Select pulse waveform at row (26). The parameter menu will automatically be illuminated, i.e. AMP/OFS or HIL/LOL — see Figure 3–1 description of these parameter keys.
4. Select each parameter in turn, and set it to the desired value using the RANGE/VERNIER keys and the digital display.
5. Apply the external signal to be shaped to the EXT INPUT connector and select the trigger slope at (8).
6. Press key (30) to enable the 8116A output. This key LED should no longer be illuminated. A timing diagram illustrating an output in this mode is given in the following.



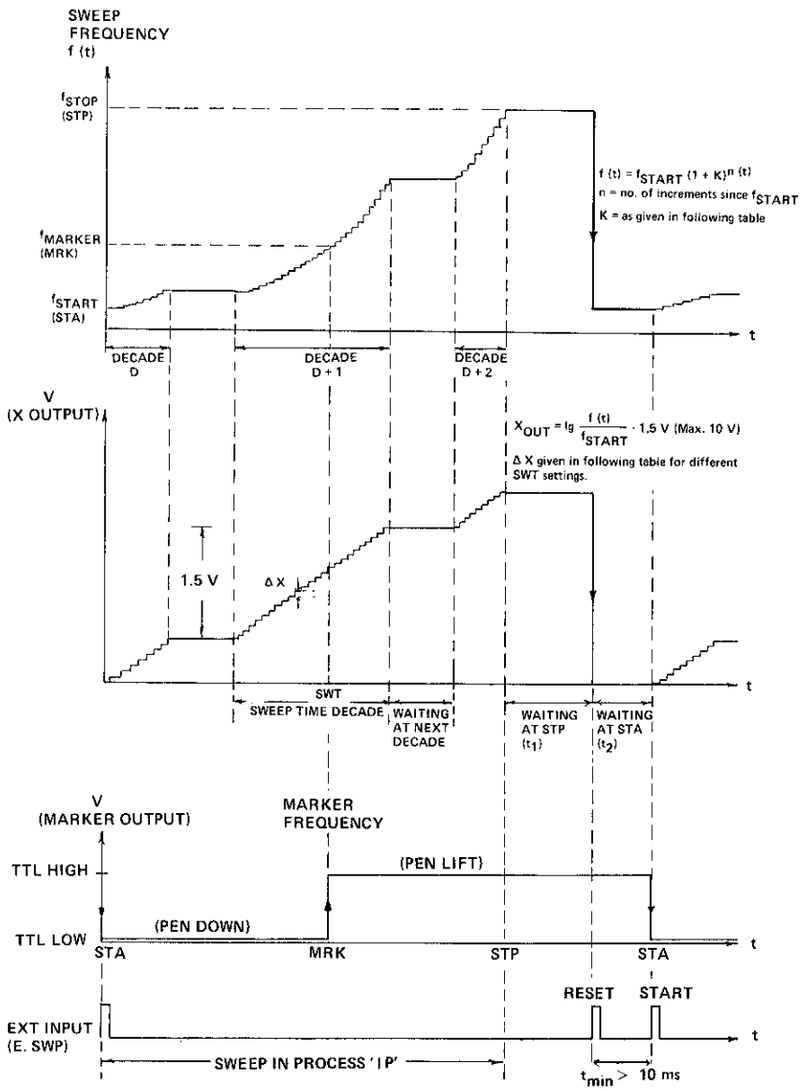
SWEEP MODES



NOTE: For parameter specifications, see Table 1–2.

1. Set the LINE switch (7) to the ON position.
2. Select a sweep mode (Internal or External) via key (4). Repetitive operation of this key steps through the Opt. 001 modes.
3. Select the desired waveform at row (26). The parameter menu will be automatically illuminated in mnemonic form, e.g. AMP for amplitude. The sweep-related parameters (STA, STP, SWT, MRK) are illustrated in the following timing diagrams.
4. Select each parameter, in turn, and set it to the required value using the RANGE/VERNIER keys and the digital display.
5. If triggering via an external signal (E. SWP), select the trigger slope at (8), and apply the trigger signal to the EXT INPUT connector. Triggering can also be simulated by pressing the MAN key. In either case, note the trigger requirements i.e. a 'reset' pulse is required prior to the 'start' pulse if the 8116A is not currently set to the STA frequency.
6. If a modulated output is required, select modulation via key (5) and apply the modulating signal to the CTRL INPUT connector.
7. Press key (30) to enable the 8116A output. The key LED should no longer be illuminated. The following timing diagrams illustrate the 8116A outputs in sweep modes.

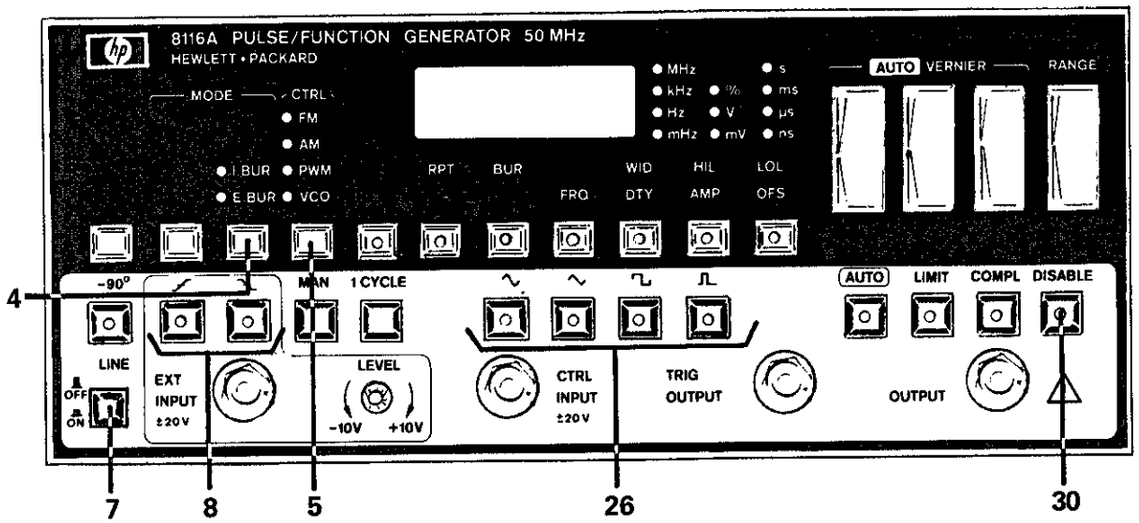
NOTES:
1. When external sweep is in process ('IP' in display), RANGE/VERNIER keys are disabled (also disabled during period 't' in following timing diagrams).
2. Sweep (I. SWP and E. SWP) can be interrupted by pressing any key other than RANGE/VERNIER/MAN/I CYCLE keys.



SWT (Sweeptime/ Decade)	K Factor	η DEC (increments/ decade)	Δ X (X_{OUT} / increment)
10 ms	0.0625	38	40 mV
20 ms	0.03125	75	20 mV
50 ms	0.015625	149	10 mV
100 ms	0.015625	149	10 mV
200 ms	0.015625	149	10 mV
500 ms	0.015625	149	10 mV
1 s	0.015625	149	10 mV
2 s	0.015625	149	10 mV
5 s	0.015625	149	10 mV
10 s	0.015625	149	10 mV
20 s	0.015625	149	10 mV
50 s	0.015625	149	10 mV
100 s	0.015625	149	10 mV
200 s	0.015625	149	10 mV
500 s	0.015625	149	10 mV

SWT is set in multiples of 1, 2 or 5 via the VERNIER keys, or in decades by the RANGE key.

BURST MODES



NOTE: For parameter specifications, see Table 1–2.

1. Set the LINE switch (7) to the ON position.

2. Select a burst mode (Internal or External) via key (4). Repetitive operation of this key steps through the Opt. 001 modes.

3. Select the desired waveform at row (26) (Pulse mode not available with I. BUR). The parameter menu will automatically be displayed in mnemonic form. The burst-related parameters (RPT, BUR) are defined in the following timing diagrams.

4. Select each parameter in turn, and set it to the required value using the RANGE/VERNIER keys and the digital display.

5. If triggering via an external signal (E.BUR), select the trigger slope at (8), and apply the trigger signal to the EXT INPUT connector.

6. If a modulated output is required, select modulation via key (5), and apply the modulating signal to the CTRL INPUT connector. See Table 3–1 for burst/control mode combinations.

7. Press key (30) to enable the 8116A output. The key LED should no longer be illuminated. The following timing diagrams illustrate the 8116A output in burst modes.

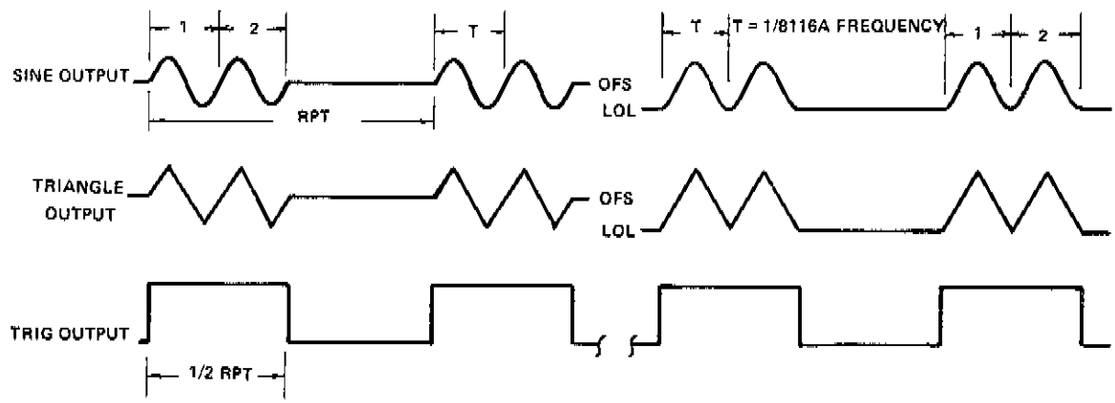
I. BUR

0° START PHASE

(BUR = 2; DTY = 50 %)

–90° START PHASE

(BUR = 2; DTY = 50 %)



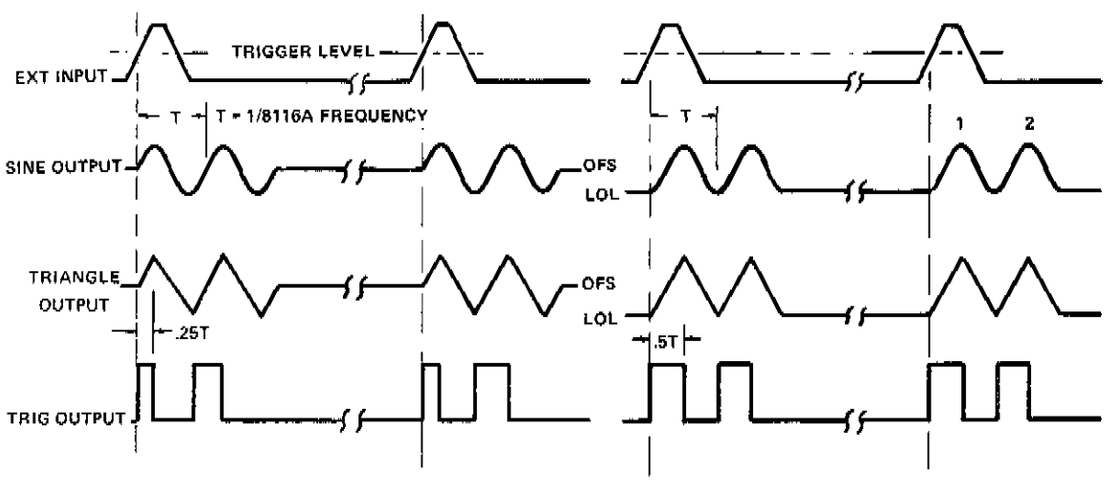
E. BUR

0° START PHASE

(BUR = 2; DTY = 50 %)

–90° START PHASE

(BUR = 2; DTY = 50 %)



3–50 PROGRAMMING

3–51 General

3–52 The 8116A operates on the HP-IB as follows:

Listens: to messages from the HP-IB system controller. In this state, all modes and parameters, except external trigger LEVEL adjust, are programmable. Also provided are special HP-IB only functions to aid the programmer.

Talks: provides error messages and reports operating parameters.

3–53 As shown in Figure 3–13, the bus lines are as follows (all use negative logic):

8-bit data bus (lines DIO 1 to 8)

handshake lines – DAV (data valid), NRFD (not ready for data), NDAC (data not accepted).

control lines – IFC (interface clear), ATN (attention), SRQ (service request), REN (remote enable), EOI (end or identify).

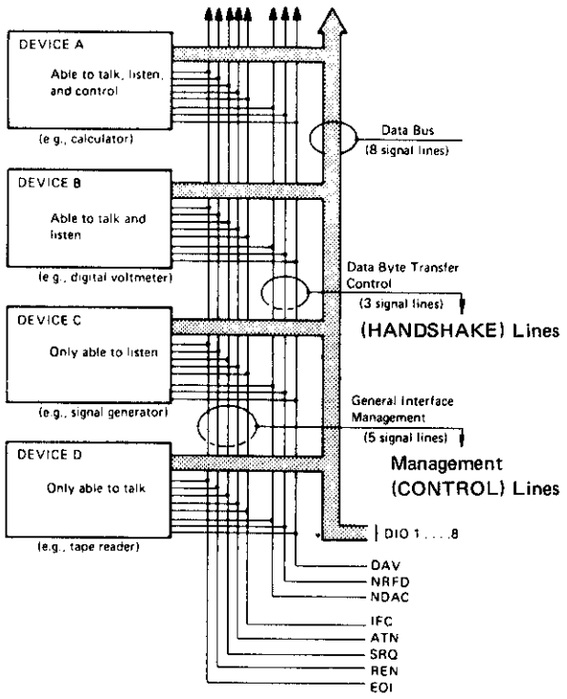


Figure 3–13. Interface Connections + Bus Structure

The 8116A uses all lines on the bus, terminations, logic levels and pinouts being described in Section II. In this manual, bus information will generally be restricted to 8116A specifics. For this reason, handshake lines are not discussed, and control lines are only mentioned in connection with specific 8116A activity. Permissible codes are presented in Table 3–9. For detailed bus information, refer to any of the following publications:

IEEE	Interface Standard 488–1975
ANSI	Interface Standard MC1.1.
HP	Publication 59401–90030
HP	Publication 5952–0058

3–54 Address Assignment

3–55 The 8116A's HP-IB address is determined by an internal storage register. This register is initialised upon power turn-on by reading the address bits A1 through A5 from the HP-IB ADDRESS switch on the rear panel. Note that this switch is factory preset to decimal 16. To change the address, first change the bit settings on the rear panel switch, then press the LCL key to read the new address into the register (alternatively, switch power off and on). Table 3–2 lists all the possible addresses on the bus.

3–56 The current HP-IB address can be checked by pressing the LCL key. The address is then displayed in decimal form.

3–57 Talk and listen addresses are transmitted by the system controller over the data bus with the ATN line true. When an instrument recognizes its address, it will respond accordingly i.e. listen if listen address has been transmitted; talk if talk address has been transmitted. When allocating addresses, make sure no two instruments have the same address. To program an address, set ATN true and arrange that the ASCII character derived from Table 3–2 appears on the bus. For deaddressing, use UNL, UNT commands (or address another device).

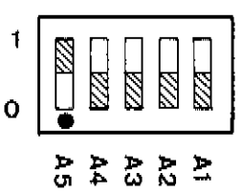
IMPORTANT!

Users of instruments with serial numbers 2124G01235 or lower should perform the following check:

Switch 8116A ON, and select E.WID and sine ~. This combination will give an ERROR condition. Switch the instrument OFF and ON again. Select WID. If the value displayed is 100 μs, it will be necessary to refer to SECTION 7 – Backdating before proceeding with any programming. If the display reads 500 μs, proceed with this section.

Table 3–2. Available Addresses (ATN true)

Data bus (DIO lines)							Address in ASCII		
Fixed			Selectable						
8	7	6	5	4	3	2	1	DEC	Talk	Listen	
0	T	L	0	0	0	0	0	0	@	Space	
0	T	L	0	0	0	0	1	1	A	!	
0	T	L	0	0	0	1	0	2	B	"	
0	T	L	0	0	0	1	1	3	C	#	
0	T	L	0	0	1	0	0	4	D	$	
0	T	L	0	0	1	0	1	5	E	%	
0	T	L	0	0	1	1	0	6	F	&	
0	T	L	0	0	1	1	1	7	G	'	
0	T	L	0	1	0	0	0	8	H	(	
0	T	L	0	1	0	0	1	9	I	)	
0	T	L	0	1	0	1	0	10	J	*	
0	T	L	0	1	0	1	1	11	K	+	
0	T	L	0	1	1	0	0	12	L	,	
0	T	L	0	1	1	0	1	13	M	–	
0	T	L	0	1	1	1	0	14	N	.	
0	T	L	0	1	1	1	1	15	O	/	
0	T	L	1	0	0	0	0	16	P	0	← 8116A set to this address at factory.
0	T	L	1	0	0	0	1	17	Q	1	
0	T	L	1	0	0	1	0	18	R	2	
0	T	L	1	0	0	1	1	19	S	3	
0	T	L	1	0	1	0	0	20	T	4	
0	T	L	1	0	1	0	1	21	U	5	← Usually controller address!
0	T	L	1	0	1	1	0	22	V	6	
0	T	L	1	0	1	1	1	23	W	7	
0	T	L	1	1	0	0	0	24	X	8	
0	T	L	1	1	0	0	1	25	Y	9	
0	T	L	1	1	0	1	0	26	Z	:	
0	T	L	1	1	0	1	1	27	[	;	
0	T	L	1	1	1	0	0	28	\	<	
0	T	L	1	1	1	0	1	29	]	=	
0	T	L	1	1	1	1	0	30	^	>	
0	T	L	1	1	1	1	1	31	_	?	← Forbidden setting! UNT, UNL commands.



Selector on 8116A rear panel (factory setting).

L = 1 for listen address, 0 for talk address
T = 1 for talk address, 0 for listen address

3–58 Remote Operator's Checks

3–59 A quick check of the 8116A's talk/listen functions is provided in Figure 3–14. [Program example assumes the 8116A address is set to the factory value 16].

3–60 Also implemented in the 8116A is a RAM/hardware self-test routine initialized via HP-IB message 'EST' – see Figure 3–15. Tested hardware functions include:

Repetition rate generator
Width generator
Shaper/output amplifier
Auto vernier

3–61 In the event of fault detection, the 8116A sets bits 4 and 7 (System Failure and Service Request) of its HP-IB Status Byte to '1'. More information on this status byte is given later under 'Error Reporting'.

3–62 Mode and Parameter Settings (Listener Function)

3–63 When the 8116A is in remote and has been listen addressed, it accepts messages which change parameter and/or mode settings. Each mode and parameter-setting message comprises either a number of ASCII data bytes transmitted serially over the data lines with ATN false or an HP-IB Universal Command. The coding for the bytes is given in Table 3–3, which summarizes all mode/parameter-setting messages. Note: The HP-IB program code syntax for parameters is identical to the front panel mnemonics e.g. AMP for amplitude. Reference may be made to Table 3–9 to convert each ASCII byte to a bit pattern on the data bus.

Figure 3–14. **TALK/LISTEN FUNCTION CHECK**

Flowchart	HPL Statements (HP 9826 Desktop Computer)	BASIC Statements (HP 85 Desktop Computer)	Visual Indicators
START			
Set REN line true to ensure 8116A is in remote enable state	rem 716	REMOTE 716	RMT LED on
Program 8116A frequency to 1 Hz	wrt 716, "FRQ 1 Hz"	OUTPUT 716; "FRQ 1 Hz"	RMT and ADS LED's on. FRQ key LED on. '1.00 Hz' displayed.
Interrogate 8116A frequency setting	wrt 716, "IFRQ" dim A$ [12] red 716, A$	OUTPUT 716; "IFRQ" ENTER 716; A$	
Print 8116A frequency	prt A$	PRINT A$	Printout "FRQ 1.00 Hz"
END			

Figure 3–15. **RAM / HARDWARE CHECK**

Flowchart	HPL Statement (HP 9826)	BASIC Statement (HP 85)
START		
Set REN line true to ensure 8116A is in remote enable state	rem 716	REMOTE 716
Program 8116A to execute self-test	wrt 716, "EST"	OUTPUT 716; "EST"
Read status of 8116A HP-IB Status Register, and store decimal value of status byte in B	rds (716) → A	A=SPOLL (716)
B # 1 (no / yes)		
CONTINUE		
Print "8116A FAULT"	IF B (BIT 3); PRT "8116A FAULT"	B=BIT (A, 3) IF BIT = 1 THEN PRINT "8116A FAULT"
END		

3–64 When programming, it is possible to put the instrument into an error condition in the same way as when under local (frontpanel) control.
For example:

current settings: HIL 2.5V, LOL 1.5V
FRQ 10kHz, WID 10 μs

program settings: LOL 3.0V, FRQ 1MHz

Both of the new program settings will put the instrument into an error condition. However, if BOTH HIL and LOL and/or FRQ and WID values are re-programmed in the same string, e.g.

HIL 3.5V, LOL 3.0V
FRQ 1MHz, WID 100ns

no error will occur. The above is applicable to HIL, LOL, AMP, OFS, FRQ, WID, DTY, STA and STP. In the event of an error occuring, a "Service Request" will be sent to the controller. More information on parameter programming sequence is given under "Error Reporting".

3–65 The 8116A does not necessarily respond to program codes in the order in which they are sent. The 'Universal' messages such as operating and control modes, waveform and trigger slope selections are processed before parameter data. For some applications, the operator will require a parameter to be changed before, say, an operating mode. To achieve this, the CRLF (") message must be sent immediately after the parameter value, and the operating mode data sent in a seperate string. The following examples illustrate this point.

```
10  OUTPUT 716; "TO, HIL 4.00V, LOL –1.00V, MI"
```

In this case, messages T0 and M1 will be processed before the HIL and LOL data.

```
10  OUTPUT 716; "HIL 4.00V, LOL –1.00V"
20  OUTPUT 716; "T0, M1"
```

In this case, HIL and LOL settings will be processed before T0 and M1. Should the operator require a time interval of, say, 550 ms before line 20 is executed, the input to the controller should look like this:

```
10  OUTPUT 716; "HIL 4.00V, LOL –1.00V"
20  WAIT 550
30  OUTPUT 716; "T0, M1"
40  END
```

The End of String message (EOS) must be the ASCII character sequence CRLF or the bus END command (EOI true and ATN false).

3–66 Mode and Parameter Settings (Talker Function)

3–67 The 8116A can send data messages, concerning its mode/parameter settings, when in remote and addressed to talk. The available output modes are:

Learn String
Interrogate Function
Status

Table 3–4 lists the ASCII commands associated with each of these modes.

3–68 The Learn String message ("CST") consists of an 89 (161 for Opt. 001 instruments) character ASCII string representing the 8116A current settings. The order in which data is presented is always the same, the exception to the rule being whether HIL/LOL or OFS/AMP is currently active on the frontpanel. Below are examples to show what the Learn String messages look like.

```
CST
  M1,CT0,T1,W1,H0,A0,L0,C0,D1,BUR
  001  #, RPT 100 MS, STA 1.00 KHZ
  ,STP 100 KHZ, SWT 50.0 MS, MRK 1.0
  0 KHZ, FRQ 1.00 KHZ, DTY 50 %, WID
  100 US, AMP 1.00 V, OFS 100 MV
                          AMP and OFS active
CST
  M1,CT0,T1,W1,H0,A0,L0,C0,D1,BUR
  0001  #, RPT 100 MS, STA 1.00 KHZ
  ,STP 100 KHZ, SWT 50.0 MS, MRK 1.0
  0 KHZ, FRQ 1.00 KHZ, DTY 50 %, WID
  100 US, HIL 0.30 V, LOL –0.70 V
                          HIL and LOL active
```

3–69 The Status Function sends an 8-bit byte in response to a Serial Poll. Bits 5 and 6 of bits 1 through 8 are allocated for current operating conditions:

Bit 5 set to one (16 dec) indicates "Autovernier in Progress"

Bit 6 set one (32 dec) indicates "Sweep in Progress"

A more detailed description of the Status Byte is given under 'Error Reporting'.

3–70 In all talker modes, the 8116A terminates its data message with the ASCII character sequence CR/LF.

Table 3–3. Mode / Parameter Messages (listen function)

MESSAGE	MNEMONICS ASCII CODE	ASCII CODE DELIMITERS	SAMPLE STATEMENTS
Operating Modes			
select NORM	M1		
select TRIG	M2		
select GATE	M3		
select E.WID	M4		
select I.SWP	M5 (Opt. 001)		
select E.SWP	M6 (Opt. 001)		
select I.BUR	M7 (Opt. 001)		**HPL (HP 9826)** / **BASIC (HP 85)**
select E.BUR	M8 (Opt. 001)		
Control Modes			
off	CT0		
select FM	CT1		
select AM	CT2		wrt 716, "M2, T1, W2" / OUTPUT 716; "M2, T1, W2"
select PWM	CT3		
select VCO	CT4		selects trigger mode with triggering on the positive slope of external signal, and triangle output.
Trigger Slope			
off	T0		
select positive slope	T1		
select negative slope	T2		
Haversine (–90°)			
off	H0		
on	H1		
Waveform			
off (dc)	W0		
select sine	W1		
select triangle	W2		
select square	W3		
select pulse	W4		
Parameters			
set frequency	FRQ	MZ = Millihertz HZ = Hertz KHZ = Kilohertz MHZ = Megahertz	
set duty cycle	DTY	%	
set width	WID	NS = Nanoseconds US = Microseconds MS = Milliseconds	
set amplitude	AMP	MV = Millivolts V = Volts	
set offset	OFS	MV = Millivolts V = Volts	

Table 3–3. Mode / Parameter Messages (cont'd)

MESSAGE	MNEMONICS ASCII CODE		ASCII CODE DELIMITERS	SAMPLE STATEMENTS
set high level	HIL		V = Volts	**HPL** **BASIC**
set low level	LOL		V = Volts	wrt 716, "FRQ 1 KHZ, DTY 50 %, BUR 7 #, RPT 100 MS" OUTPUT 716;"FRQ 1 KHZ, DTY 50 %, BUR 7 #, RPT 100 MS"
				sets frequency to 1 kHz, duty cycle to 50 %, burst number to 7 and time between burst 'starts' to 100ms
set burst number	BUR	Opt. 001	#	
set repetition rate for internal burst	RPT		NS = Nanoseconds US = Microseconds MS = Milliseconds	
set sweep start frequency	STA		MZ = Millihertz HZ = Hertz KHZ = Kilohertz MHZ = Megahertz	
set sweep stop frequency	STP		MZ = Millihertz HZ = Hertz KHZ = Kilohertz MHZ = Megahertz	
set sweep marker frequency	MRK		MZ = Millihertz HZ = Hertz KHZ = Kilohertz MHZ = Megahertz	
set sweep time	SWT		S = Seconds MS = Milliseconds	
Sign				
+	+			
+	–			
Decimal point				
.	.			
Limit				
off	LO			
on	LI			
Complement				
off (normal output)	C0			
on	C1			

Table 3–3. Mode / Parameter Messages (cont'd)

MESSAGE	MNEMONICS ASCII CODE	ASCII CODE DELIMITERS	SAMPLE STATEMENTS
Disable			
off (output enabled)	D0		
on	D1		
Autovernier mode			
off	A0		
on	A1		
Autovernier start			HPL: wrt 716, "OFS 120 MV, A1, LU" / BASIC: OUTPUT 716; "OFS 120 MV, A1, LU" — offset is incremented in 1mV steps with offset start value 120 mV
most significant digit up	MU		
second significant digit up	SU		
least significant digit up	LU		
most significant digit down	MD		
second significant digit down	SD		
least significant digit down	LD		
Execute Self-Test	EST		

HP-IB Universal Commands			HPL	BASIC
Device Clear (DCL)		Loads standard parameter set stored in 8116A ROM's. 8116A does not remain in remote mode e.g. CLEAR 7	clr 7	CLEAR 7
Selected Device Clear (SDC)		Loads standard parameter set stored in 8116A ROM's. 8116A remains in remote mode.	clr 716	CLEAR 716
Group Execute Trigger (GET)		When the 8116A is in trigger, external sweep mode, this message initiates a single cycle, burst or sweep respectively.	trg 716	TRIGGER 716

NOTES:

1. Lower case letters can replace any or all of the ASCII capitals.
2. When programming a parameter for which delimiters are given, the parameter string must be terminated with a delimiter e.g. wrt 716, "BUR 17 #".
   ↑
3. The Autovernier function MUST be enabled BEFORE incrementing/decrementing of any digit can be achieved. Without "A1" appearing in the program string the Autovernier digit commands cannot be executed.

Table 3–4. Mode/Parameter Messages (Talker Function)

Message	ASCII Mnemonics	Sample Statements	
Current Parameter Setting	CST	HPL (HP 9826) dim A$ [89] or [161] wrt 716, "CST" red 716, A$	BASIC (HP 85) DIM A$ [89] or [161] OUTPUT 716; "CST" ENTER 716; A$
Interrogate Parameter	IERR IFRQ IDTY IWID IHIL ILOL IAMP IOFS IBUR IRPT ISTA ISTP IMRK ISWT	dim B$ [12] wrt 716, "IFRQ" red 716, B$	DIM B$ [12] OUTPUT 716; "IFRQ" ENTER 716; B$
Status Byte (Serial Poll Enable/ Serial Poll Disable)		rds (716) → A	A = SPOLL (716)

3–71 Error Reporting

3–72 In general, whenever a program attempts to put the 8116A into an error condition, the 8116A responds by making a Service request i.e. set SRQ line true. Under these circumstances, the system controller will address the 8116A as talker using a serial poll command (SPE), the 8116A then responding by putting an error message on the data bus. This message consists of a single 8-bit byte in which SRQ bit 7 is set true ('1') and bits 1 to 3 comprise an error code. The contents of this byte are shown in Table 3–5.

3–73 As can be seen from Table 3–5, bits 1 to 3 are each allocated to an error type. i.e. TIMING, PROGRAMMING and SYNTAX. In each case the bit is set to '1' for error indication.

3–74 Should a more detailed description of the error be required (e.g. duty cycle error or width error when TIMING ERROR is indicated by the status byte), this can be done via the 'interrogate error' (IERR) command. Table 3–6 and 3–7 list the 8116A responses to the IERR command for TIMING and PROGRAMMING errors respectively.

3–75 Service Request. Bit 7 of the HP-IB Status Byte is usually set in conjunction with any of bits 1–4 (error indicators). However, in the case of the TIMING ERROR indication (bit 1), the 'Service Request' message can be suppressed via the command "SR1"

e.g. (HPL) wrt 716, "SR1"
(BASIC) OUTPUT 716; "SR1"

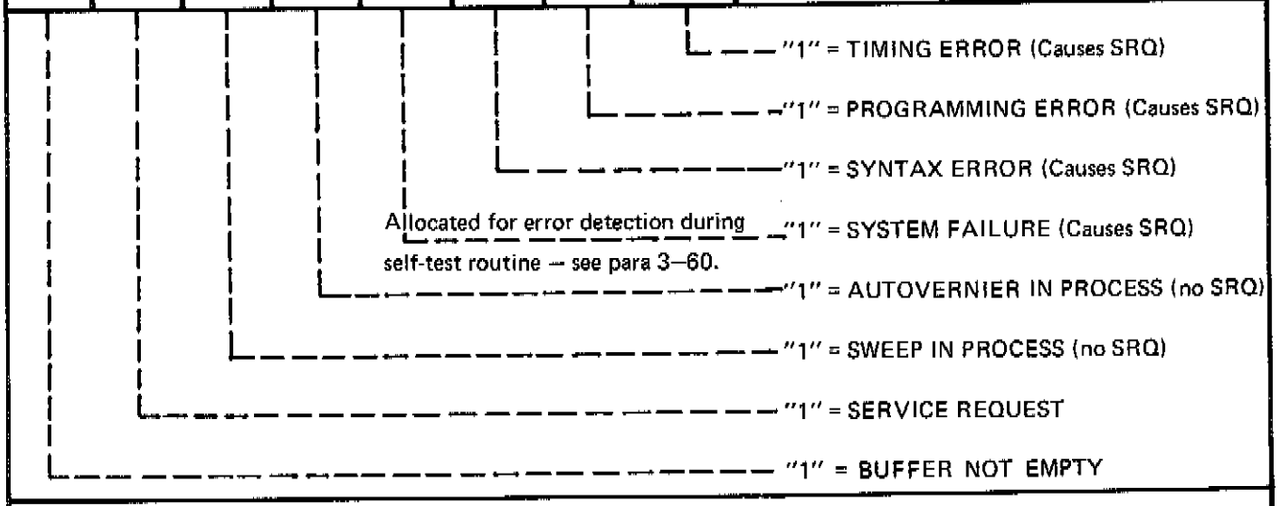
Note: In the permanently stored mode/parameter settings in the 8116A's ROM's, 'SR' is set to '0'. Should these settings be called up as current settings, the service request function can be re-activated for timing errors by programming 'SR' to '0'

e.g. (HPL) wrt 716, "SR0"
(BASIC) OUTPUT 716; "SR0"

3–76 In the event of a FRQ or DTY correction error, SRQ will be displayed until the error has been interrogated by SPOLL. If the current data, for example, includes "FRQ 20 MHZ, W4", and new program data includes "DTY 50 %, W3", SRQ will become active until interrogated, at which time it will be withdrawn. Note that the new DTY value is displayed as 50 % in this case. The reason for this is that at 20 MHz, Duty Cycle selection is not available in Pulse mode. Note also that an "IERR" command will NOT clear SRQ in the event of a DTY or FRQ correction error.

Table 3–5. HP-IB Status Byte

HP-IB Status Byte								Sample Statements	
								HPL (HP 9826)	BASIC (HP 85)
Bit 8 (DIO 8)	Bit 7 (DIO 7)	Bit 6 (DIO 6)	Bit 5 (DIO 5)	Bit 4 (DIO 4)	Bit 3 (DIO 3)	Bit 2 (DIO 2)	Bit 1 (DIO 1)	rds (716) → A	A = SPOLL (716)



e.g. 0 1 0 0 0 1 0 0 (68 decimal) indicates SYNTAX ERROR

Table 3–6. Timing Error Messages (Response to interrogate error statement 'IERR')

ASCII String	Comments
WAVEFORM ERROR (15 characters)	1. This message is sent when any of the following conditions are not observed: a) In PWM control mode, pulse waveform must be selected. b) In E.WID mode, pulse waveform must be selected. c) With E.WID mode and pulse waveform selected, the only permissible control mode is AM. d) In I.BUR mode, pulse waveform is not allowed. Table 3–1 provides a complete overview of permissible mode/waveform combinations. 2. The 8116A output remains unchanged during the error condition, and front panel LED's blink to indicate the erroneous settings. 3. SRQ cannot be suppressed for this error (see 'Service Request' description).
DUTY C. ERROR (14 characters)	1. This message is sent to indicate 'duty cycle error' when either of the following conditions are not observed: a) In frequency range 1 MHz to 9.99 MHz, duty cycle limits are 20 % to 80 %. b) For frequencies ≥ 10 MHz, duty cycle must be set to 50 %. 2. The erroneous duty cycle setting is not stored in the 8116A memory, and the output remains unchanged. 3. SRQ cannot be suppressed for this error – see 'Service Request' description.

Table 3–6. Timing Error Messages (cont'd)

WIDTH ERROR (12 characters)	1. This message is sent when the width and frequency settings are incompatible. 2. 8116A hardware detects this error condition which causes the output to change. 3. SRQ can be suppressed for this error via the HP-IB message "SR1". In this case, the first bit of the HP-IB status byte is still set to '1' during error condition. "SR1" is the 8116A's default value.
TIMING ERROR (13 characters) (OPT 001 ONLY)	1. This message is sent in I.BUR mode to indicate timing error when: BUR x 1/FRQ > RPT where BUR = Burst number FRQ = 8116A frequency setting RPT = Burst repetition time 2. 8116A hardware detects this error condition which causes the output to change. 3. SRQ can be suppressed for this error via the HP-IB message "SR1". In this case, the first bit of the HP-IB status byte is still set to '1' during error condition. "SR1" is the 8116A's default value.
NOTE: The 8116A can output more than one error message in response to a single 'IERR' command, e.g. "WAVEFORM ERROR WIDTH ERROR". When multiple errors are suspected, be sure to dimension enough memory space to accommodate the possible character strings.	

Table 3–7. Programming Error Messages (Response to interrogate error statement 'IERR')

ASCII String	Comments
HANDLING ERROR (15 characters)	1. A handling error occurs when: a) User attempts to select Autovernier operation ("A1") when the 8116A is not in NORM ("M1") mode. b) User attempts to exit NORM mode (e.g. program "M2" for TRIG mode) with Autovernier operation selected. The 8116A output changes to correspond to the new mode. c) User attempts to program a parameter value outside the specification limits. e.g. "FRQ 60 MHZ". The 8116A output and display remain unchanged during this error condition. NOTE: Display overflows are NOT indicated.
LEVEL ERROR (12 characters)	1. This message is sent when either of the following conditions are not observed: a) For amplitudes ≥ 100 mV, the HIL/LOL voltage window is ± 8.00 V. b) For amplitudes ≤ 100 mV, the HIL/LOL voltage window is ± 800 mV. Error detection is determined via the following formula: HIL = OFS + 1/2 AMP LOL = OFS – 1/2 AMP 2. The 8116A output remains unchanged during the error condition. 3. The programmed level is outside the specification limits. e.g. "HIL 20 V".
LIMIT ERROR (12 characters)	1. Conditions are described for 'LEVEL ERROR' except that the HIL/LOL window is determined by the currently active levels when LIMIT operation is selected.
NOTE: The 8116A can output more than one error message in response to a single 'IERR' command e.g. "HANDLING ERROR LEVEL ERROR". When multiple errors are suspected, be sure to dimension enough memory space to accommodate the possible character strings.	

3–77 Universal HP-IB Commands

3–78 The 8116A will respond to the universal commands listed in Table 3–8, which are sent in the command modes (ATN true).

Table 3–8. HP-IB Universal Commands

Mnemonic	Command	ASCII Code
DCL	Device Clear	DC4
LLO	Local Lockout	DC1
MLA	My Listen Address	(selectable)
MTA	My Talk Address	(selectable)
SPD	Serial Poll Disable	EM
SPE	Serial Poll Enable	CAN
UNL	Unlisten	?
UNT	Untalk	–
GET	Group Execute Trigger	BS
GTL	Go to Local	SOH
SDC	Selected Device Clear	EOT

3–79 Local, Remote and Local Lockout

3–80 Local Capability. In local mode, the 8116A can communicate on the bus by sending a Status Byte indicating 'autovernier in process' or 'sweep in process'., as well as responding to the Remote Message.

3–81 **Remote Capability.** In remote mode, the 8116A's front panel controls are disabled except the LINE switch, LCL key and LEVEL adjust. When addressed to listen, the 8116A will respond to the following bus messages: Data, Trigger, Clear, Remote, Local, Local Lockout, Clear Lockout/Set Local and Abort. When addressed to talk, the 8116A will send one of the following messages: Data, Require Service, or Status Byte.

3–82 The RMT LED is on when the 8116A is in remote mode. The ADS LED is on when the 8116A is currently addressed to talk or listen. The 8116A front panel digital display shows the value of the last programmed parameter.

3–83 Local-to-Remote Change. The 8116A switches to remote upon receipt of the two part Remote Message. The two parts are:

Remote Enable (REN)
Addressed to Listen or Talk (MLS or MTA)

The 8116A's output signal and all control settings remain unchanged with the local-to-remote transition.

3–84 Remote-to-Local Change. The 8116A returns to local control upon receipt of the Local or Clear Lockout/Set Local message. It can also be set to local by pressing the front panel LCL key (assuming that local lockout is not in effect). The output signal and all control settings remain unchanged with the remote-to-local transition.

3–84 Local Lockout. When a data transmission is interrupted, which can happen by returning the 8116A to local with the front panel LCL key, the data could be lost. This would leave the 8116A in an unknown state. To prevent this, a local lockout is recommended to disable the LCL key. Local lockout remains in effect until the 8116A is returned to the local state by either turning the LINE switch off/on or by programming the Local Message.

Table 3–9. Code Assignments (ASCII) for the 8116A

APPLIES ONLY IN COMMAND MODE (ATN TRUE)

THESE CHARACTERS CAUSE SRQ

THESE CHARACTERS ARE IGNORED

DATA MODE (ATN FALSE)

SAME INTERPRETATION

SAME INTERPRETATION

HP IB DATA LINES 7 6 5 / 4 3 2 1 0	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0 0 0 0 0	NUL		DLE		SP	0	@	P		p
0 0 0 1 1	SOH GTL		DC1	LLO	!	1	A	Q	a	q
0 0 1 0 2	STX		DC2		"	2	B	R	b	r
0 0 1 1 3	ETX		DC3		#	3	C	S	c	s
0 1 0 0 4	EOT SDC		DC4	DCL	$	4	D	T	d	t
0 1 0 1 5	ENQ		NAK		%	5	E	U	e	u
0 1 1 0 6	ACK		SYN		&	6	F	V	f	v
0 1 1 1 7	BEL		ETB		'	7	G	W	g	w
1 0 0 0 8	BS GET		CAN	SPE	(	8	H	X	h	x
1 0 0 1 9	HT		EM	SPD	)	9	I	Y	i	y
1 0 1 0 10	LF		SUB		*	:	J	Z	j	z
1 0 1 1 11	VT		ESC		+	;	K	[	k	{
1 1 0 0 12	FF		FS		,	<	L	\	l	|
1 1 0 1 13	CR		GS		-	=	M	]	m	}
1 1 1 0 14	SO		RS		.	>	N	^	n	~
1 1 1 1 15	SI		US		/	?	O	_	oo	DEL

ASSIGNED LISTEN ADDRESS

ASSIGN LISTEN ADDRESS

UNL

ASSIGNED TALK ADDRESS

ASSIGNED TALK ADDRESS

UNT

SECTION IV
PERFORMANCE TESTS

4–1 INTRODUCTION

4–2 The procedures in this section test the electrical performance of the instrument using the specifications of Table 1–2 as performance standards. All tests can be performed without access to the interior of the instrument.

4–3 EQUIPMENT REQUIRED

4–4 Equipment required for the performance tests is listed in Table 1–1, Recommended Test Equipment. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended model(s).

4–5 TEST RECORD

4–6 Results of the performance tests may be tabulated on the Test Record at the end of the test procedures. The Test Record lists all of the tested specifications and their acceptable limits. Test results recorded at incoming inspection can be used for comparison in periodic maintenance, troubleshooting, and after repairs or adjustments.

4–7 PERFORMANCE TESTS

4–8 The performance tests given in this section are suitable for incoming inspection, troubleshooting, or preventive maintenance. During any performance test, all shields and connecting hardware must be in place. The tests are designed to verify the published instrument specifications, perform the tests in the order given and record the data on the Test Record at the end of the test procedures.

4–9 Each test is arranged so that the specification is written as it appears in Table 1–2. Next, when necessary, a description of the test and any special instructions or problem areas are included. Each test that requires test equipment has a setup drawing and a list of the required equipment. The initial steps of each procedure give control settings required for that particular test.

PERFORMANCE TESTS

4–10 FREQUENCY

SPECIFICATION

1.00 mHz to 50 MHz

(1 mHz to 999 kHz for 10 % and 90 % duty cycle)

(1 mHz to 9,99 MHz for 20 % and 80 % duty cycle)

Accuracy in Norm input mode:

% of setting	Pulse mode or 50 % duty cycle	≠ 50 % duty cycle
1 mHz to 99,9 kHz	± 3 %	± 3 %
100 kHz to 9,99 MHz	± 5 %	± 10 %
10 MHz to 50 MHz	± 5 %	—

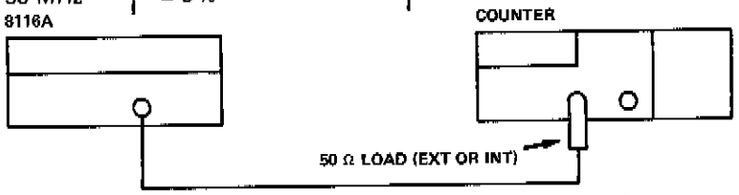


Figure 4–1. Test Setup for Frequency, Burst and Sweep

EQUIPMENT

Counter
Cable Assembly BNC (61 cm)
Feedthrough Termination 50 Ω (if necessary)

PROCEDURE

1. Connect equipment as shown in Figure 4–1.

2. Set 8116A as follows:

INPUT MODE	NORM
FUNCTION	SQUARE
DUTY CYCLE	50 %
CTRL	OFF
AMPL	1 V
OFFSET	0 V
OUTPUT MODE	NORM

3. Set counter to frequency measurement.

4. Set 8116A frequency and verify counter frequency reading as follows:

8116A setting	Counter reading
50,0 MHz	50,0000 MHz ± 2500 kHz
10,0 MHz	10,0000 MHz ± 500 kHz
10,0 kHz	10,0000 kHz ± 300 Hz
1,0 kHz	1,00000 kHz ± 30 Hz

5. Set 8116A frequency and verify counter period reading as follows:

8116A setting	Counter reading
1,00 Hz	1,00000 s ± 33,3 ms
100 mHz	10,00000 s ± 333 ms

PERFORMANCE TESTS

4–11 PULSE WIDTH (pulse mode)

SPECIFICATION

10 ns to 999 ms
Accuracy ± 5 % of setting ± 2 ns

EQUIPMENT

Counter
Cable Assembly BNC
Sampling oscilloscope
Feedthrough Termination (if necessary)

PROCEDURE

1. Connect equipment as shown in Figure 4–1.

2. Set 8116A as follows:

INPUT MODE	NORM
FUNCTION	PULSE
CTRL	OFF
FRQ	1 MHz
AMP	1 V
OFS	0 V

3. Set counter to TI, COMA, CH A +, CH B –, Trig level 0 V.

4. Set 8116A width /frequency as shown and verify counter width reading.

FREQUENCY	WIDTH	COUNTER READING
1 MHz	100 ns	93 ns – 107 ns
100 KHz	1 µs	948 ns – 1052 ns
1 KHz	100 µs	95 µs – 105 µs
10 Hz	1 ms	950 µs – 1050 µs
1 Hz	500 ms	475 ms – 525 ms

5. Connect the equipment as shown in Figure 4–6.

6. Set 8116A as follows:

FRQ	10.0 MHz
WID	8.0 ns

7. Set sampling scope such that one cycle fills the display. Verify that width is between 7.5 and 10 ns.

PERFORMANCE TESTS

4–12 BURST (Option 001 only)

SPECIFICATION

A pre-programmed number of output cycles is generated on receipt of an input trigger signal or manual command, min time between bursts: 100 ns. Burst length: 1 to 1999 cycles. Frequency up to 40 MHz.

EQUIPMENT

Counter
Cable Assembly BNC (61 cm)
Feedthrough Termination 50 Ω (if necessary).

PROCEDURE

1. Load Burst number 816 into 8116A.

2. Set 8116A as follows:

INPUT MODE	EXT BURST
FUNCTION	SQUARE
DUTY CYCLE	50 %
CTRL	OFF
FRQ	10 kHz
AMPL	1 V
OFFSET	0 V
BURST	816
OUTPUT MODE	NORM

3. Use Figure 4–1 test setup and set counter to START.

4. Press 8116A's MAN button and verify that counter now displays the set number (816) of output cycles. (5345A reading will be 815, since first pulse arms the counter).

PERFORMANCE TESTS

4–13 AMPLITUDE AND OFFSET

SPECIFICATION

Amplitude and offset are independently variable within the two following level windows.

Level window	± 800 mV	± 8.00 V
Amplitude range	10.0 mVpp to 99.9 mVpp	100 mVpp to 16.0 Vpp
Ampl. resolution	3 digits	3 digits
Ampl. accuracy*	± 5 % (0.45 dB)	± 5 % (0.45 dB)
Repeatability	Factor 4 better than accuracy	
Offset range	0 to ± 795 mV	0 to ± 7.95 V
Offset resolution	3 digits (best case 100 μV)	3 digits (best case 1 mV)
Offset accuracy	± 1 % of setting ± 1 % of amplitude ± 4 mV	± 0.5 % of setting ± 1 % of amplitude ± 40 mV
Repeatability	Factor 4 better than accuracy	

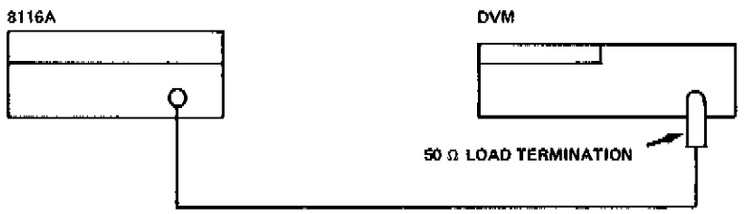


Figure 4–2. Test Setup for Amplitude and Offset

EQUIPMENT

Digital Voltmeter (RMS)
Cable Assembly BNC (1 x 61 cm)
Feedthrough Termination 50 Ω

If total error is > ± .5 % of nominal, note deviation and take into account during measurement.

PROCEDURE

1. Connect the equipment as shown in Figure 4–2.

2. Set 8116A as follows:

INPUT MODE	NORM
FUNCTION	SINE
DUTY CYCLE	50 %
CTRL	OFF
FRQ	1,0 kHz
OFFSET	0 V
OUTPUT MODE	NORM

PERFORMANCE TESTS

AMPL	FUNCTION	DVM Reading *
8.00 V	Sine W1	2,69 – 2,97 V
	triangle W2	2,19 – 2,43 V
	square W3	3,8 – 4,2 V
3.00 V	Sine	1,008 – 1,114 V
	triangle	0,823 – .909 V
	square	1,425 – 1,575 V
1.00 V	Sine	0,336 – 0,372 V
	triangle	0,275 – 0,303 V
	square	0,475 – 0,525 V
100 mV	Sine	33,6 – 37,1 mV
	triangle	27,4 – 30,3 mV
	square	47,5 – 52,5 mV

3. Set 8116A to NORM mode, Amplitude 100 mV.

4. Using best DVM resolution, measure the dc voltages for the following 8116A settings:

OFFSET	DVM Reading *
7.5 V	7,421 – 7,578 V
5.00 V	4,934 – 5,066 V
3.00 V	2,944 – 3,056 V
1.00 V	0,954 – 1,046 V
100 mV	58 mV– 142 mV

5. Set 8116A to amplitude 10 mV and measure the DC voltages for the following 8116A settings:

OFFSET	DVM Reading *
795 mV	783 - 807 mV
500 mV	491 - 509 mV
100 mV	95 - 105 mV

* last digit rounded

PERFORMANCE TESTS

4–14 SINE CHARACTERISTICS

SPECIFICATION

Total Harmonic Distortion (THD): < 1 % (–40 dB),
(10 Hz to 50 kHz)
Harmonic Signals: More than 34 dB below fundamental (50 kHz to 1 MHz).
More than 23 dB below fundamental (1 MHz to 50 MHz, > 20 mVpp to 8 Vpp.)

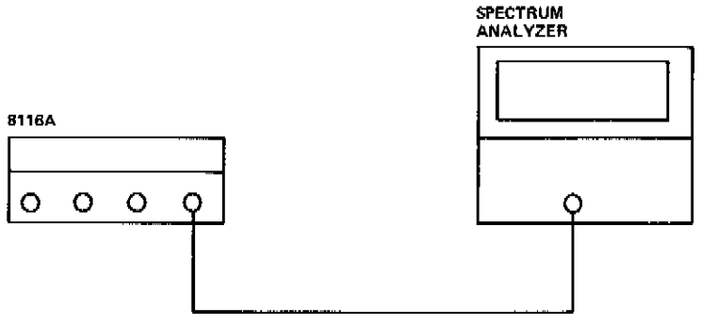


Figure 4–3. Test Setup for Sine Characteristics

EQUIPMENT

Spectrum analyzer
Cable assembly BNC (1 x 61 cm)

PROCEDURE

1. Connect the equipment as shown in Figure 4–3.

2. Set 8116A as follows:

INPUT MODE	NORM
FUNCTION	SINE
DUTY CYCLE	50 %
CTRL	OFF
FRQ	1 kHz
AMPL	8 V
OFFSET	0 V
OUTPUT MODE	NORM

3. Tune spectrum analyzer for minimum display amplitude. Adjust gain so that fundamental corresponds to 0 dB.

PERFORMANCE TESTS

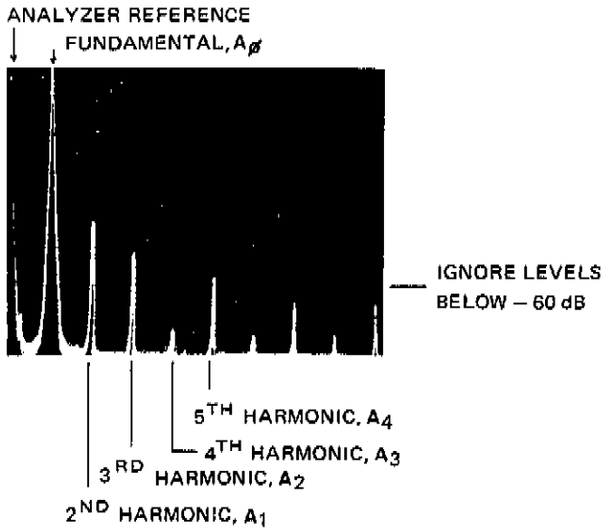


Figure 4–4. Typical Spectrum Analyzer Display at 1 KHz

The value of harmonics may differ between instruments.

4. Verify that THD $<$ 1 %

$$THD = \frac{\sqrt{E_1^2 + E_2^2 + E_3^2 + \ldots\ldots\ldots}}{E_0} \cdot 100\ \%$$

where E_0 = fundamental voltage amplitude and E_1, E_2 etc are the 2nd, 3rd etc harmonic amplitudes.

When the harmonics are expressed in dB the formula becomes:

$$THD = \sqrt{10^{\frac{A_1}{10}} + 10^{\frac{A_2}{10}} + 10^{\frac{A_3}{10}} + \ldots\ldots\ldots} \cdot 100\ \%$$

where A_1 = first harmonic in dB etc.

5. Set 8116A FRQ to 50 MHz.

6. Tune spectrum analyzer for minimum display amplitude. Adjust gain so that fundamental corresponds to 0 dB. Verify that no harmonics exceed the –23 dB level.

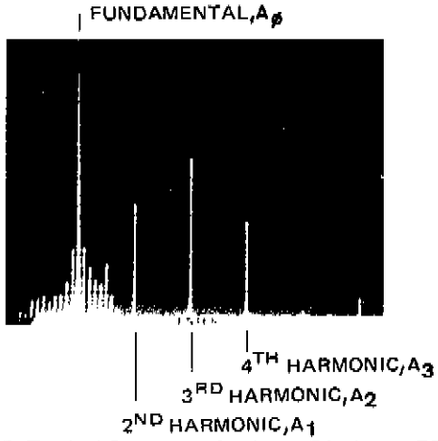


Figure 4–5. Typical Spectrum Analyzer Display at 50 MHz, NORM

The value of harmonics may differ between instruments.

PERFORMANCE TESTS

4–15 PULSE CHARACTERISTICS

SPECIFICATION

Transition times (10 % to 90 %): < 6 ns

Preshoot/Overshoot/Ringing: ± 5 %

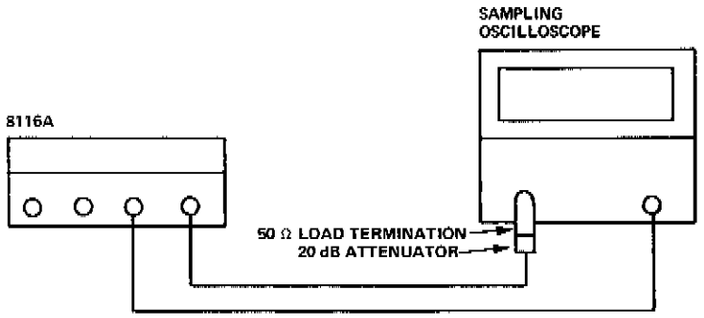


Figure 4–6. Test Setup for Pulse Characteristics

EQUIPMENT

Sampling oscilloscope
Cable assembly BNC (2 x 61 cm)
Feedthrough termination 50 Ω
Power attenuator 20 dB, 20 W

PROCEDURE

1. Connect the equipment as shown in Figure 4–6.

2. Set the 8116A as follows:

INPUT MODE	NORM
FUNCTION	SQUARE
DUTY CYCLE	50 %
CTRL	OFF
FRQ	1 MHz
AMPL	8 V
OFFSET	0 V
OUTPUT MODE	NORM

3. Set scope so that one cycle fills the display and measure:

leading edge (risetime)	⩽ 6 ns
trailing edge (risetime)	⩽ 6 ns
preshoot	⩽ ± 5 % of amplitude *
overshoot and ringing	⩽ ± 5 % of amplitude *

* note possible sampling error

PERFORMANCE TESTS

4–16 TRIGGER, GATE and E.WIDTH PERFORMANCE

SPECIFICATION

Trig: pos. ext input pulse ≥ 10 ns wide generates one output cycle.
Sensitivity: 500 mVpp
Gate: Ext. signal enables oscillator. First output cycle synchronous with active trigger slope.
Last cycle always completed.
E.Width: External signal will be shaped to determine output pulse width and period. (Pulse mode only).
Max. input: ± 20 V
Input impedance: 10 kΩ typical

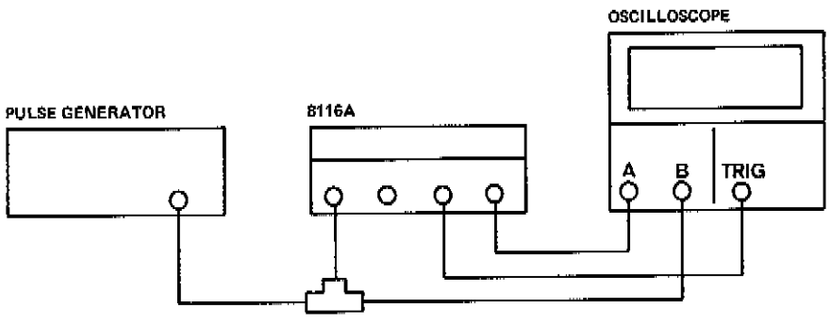


Figure 4–7. Test Setup for Burst Gate and Trigger Performance

EQUIPMENT

Pulse generator
Oscilloscope
Cable assembly (3 x 61 cm, 2 x 30 cm)
BNC Tee,
Feedthrough termination 50 Ω

PROCEDURE

1. Connect the equipment as shown in Figure 4–7.

2. Set the 8116A as follows:

INPUT MODE	TRIG
FUNCTION	SINE
DUTY CYCLE	50 %
CTRL	OFF
FRQ	60 KHz
AMPL	1 V
OFFSET	0 V
OUTPUT MODE	NORM
EXT INPUT	⏚

PERFORMANCE TESTS

3. Set ext. function generator for output pulse approx 50 μs wide, rep. rate 10 kHz, baseline zero or more negative, pulse top + 1 V. Adjust 8116A trigger input level for correct trigger. Verify that each trigger pulse generator one complete output cycle (Figure 4–8).

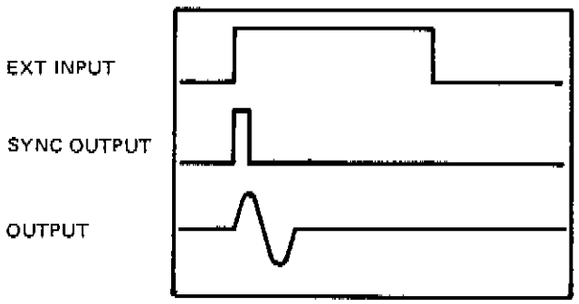


Figure 4–8. Example of correct trigger operation

4. Set 8116A to GATE mode. Verify that each positive gate releases a burst of output cycles and that each cycle is complete (Figure 4–9).

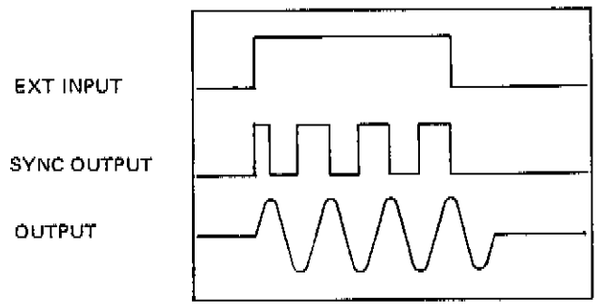


Figure 4–9. Example of correct gate operation

5. Set 8116A waveform to PULSE and mode to E.WIDTH. Verify that each external pulse releases a pulse of same width.

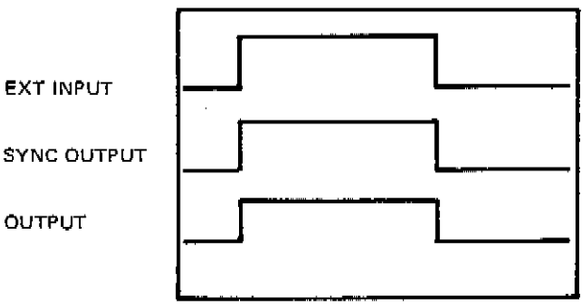


Figure 4–10. Example of correct E.Width operation

PERFORMANCE TESTS

4–17 FM

SPECIFICATION

Output is frequency modulated by an external voltage applied to the CTRL Input,1 V modulates 1 % deviation.

Deviation: ± 5 % max

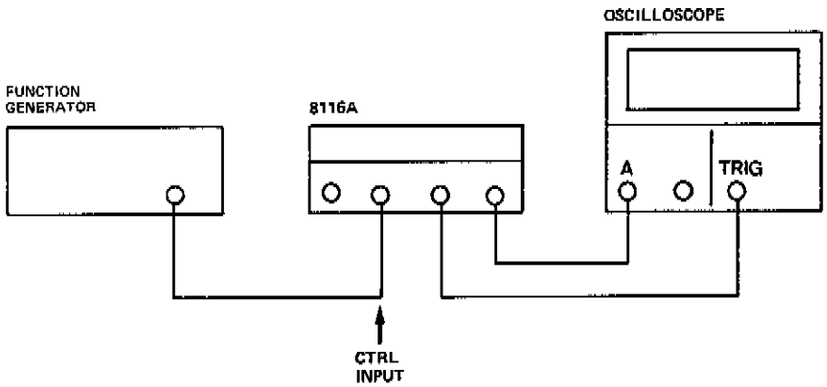


Figure 4–11. Test Setup for FM

EQUIPMENT

Oscillator
Oscilloscope
Cable assembly BNC (3 x 61 cm)

PROCEDURE

1. Connect the equipment as shown in Figure 4–11.

2. Set oscillator to 10 kHz, 2 Vpp

3. Set oscilloscope to 0,1 µs/div timebase, Magnification X10

4. Set the 8116A as follows:

INPUT MODE	NORM
FUNCTION	SQUARE
DUTY CYCLE	50 %
CTRL	FM
FRQ	1 MHz
AMPL	1 V
OFFSET	0 V
OUTPUT MODE	NORM

5. Check the delayed sweep for a typical jitter of 2 div ± 10 %.

PERFORMANCE TESTS

4–18 AMPLITUDE MODULATOR

SPECIFICATION

Modulating Frequency: dc to 1 MHz (–3 dB).
Input impedance: 10 kΩ typical.
Envelope Distortion: (dc to 50 kHz mod. freq. in Normal mode only.)

Carrier	Modulation		Distortion
≤ 1 MHz	0 to 90 %		< 1 %
> 1 MHz	0 to 30 %	<	< 3 %

Carrier Frequency Deviation: < 0.01 %, 0 to 30 % modulation.

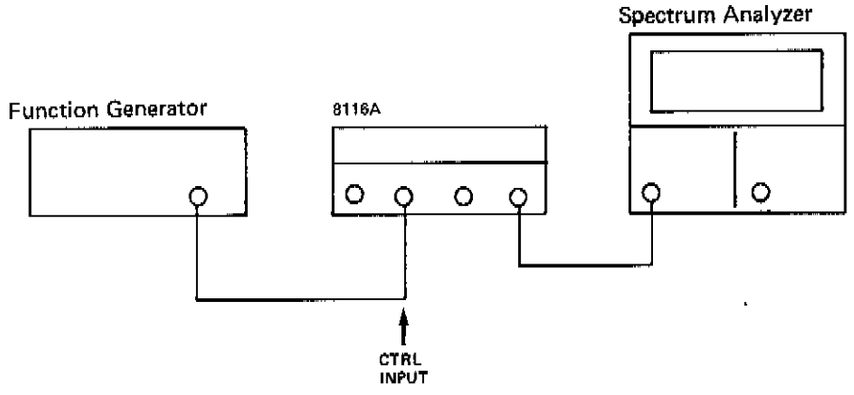


Figure 4–12. Test setup for AM

EQUIPMENT

Function Generator
spectrum analyzer

PROCEDURE

1. Connect the equipment as shown in Figure 4–12.

2. Set the 8116A as follows:

INPUT MODE	NORM
FUNCTION	SINE
DUTY CYCLE	50 %
CTRL	AM
FRQ	10 kHz
AMPL	1 V
OFFSET	0 V
OUTPUT MODE	NORM

3. Set Function Generator to 2 kHz and 4.5 Vpp amplitude, with 0.25 V offset.

4. Adjust the spectrum analyzer to display the 10 kHz carrier and the lower sideband frequency down to the 2 kHz modulating frequency. All harmonics should be at least 42 dB lower than the modulation sidebands.

PERFORMANCE TESTS

4–19 PULSE WIDTH MODULATION

SPECIFICATION

Pulse Width ratio: 10:1 max.
Sensitivity: ± 6,5V typically for ratio 1:10
Pulse Width ranges: 10 ns to 1 s in eight non-overlapping decade ranges.

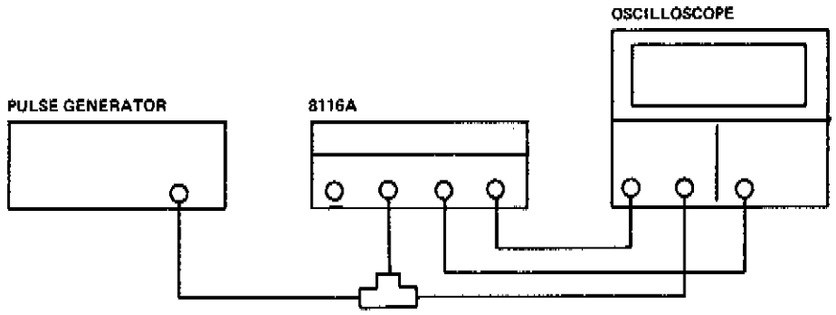


Figure 4–13. Test setup for PWM

EQUIPMENT

Realtime scope
Pulse Generator
Cable Assembly BNC (4x61 cm)
BNC Tee

PROCEDURE

1. Connect equipment as shown in Figure 4–13.

2. Set 8116A as follows:

INPUT MODE	NORM
FUNCTION	PULSE
CTRL	PWM
HIL	1.0 V
LOL	0.0 V
OUTPUT MODE	NORM

3. Set the Pulse Generator as follows:

FUNCTION	SINE
FREQUENCY	1 Hz
AMPLITUDE	13.0 Vpp
OFFSET	0.0 V

4. Select the settings shown for each test in the following Table. Verify that the 8116A Pulse Width varies with the amplitude of the signal applied to the CTRL INPUT within the given limits.

NOTE: When a width value is selected, the 8116A displays the value corresponding to a 0 V CTRL input WITHIN THE DECADE RANGE OF THE SELECTED WIDTH VALUE.
e.g. Decade = 100 ns to 1.0 us, display reads 550 ns

8116A WIDTH			SCOPE	
FREQUENCY	DECADE RANGE	DISPLAY	MIN. WID	MAX. WID
1 MHz	10 ns – 100 ns	55 ns	10 ns	100 ns
100KHz	100 ns – 1.0 µs	550 ns	100 ns	1.0 µs
100 Hz	100 µs – 1.0ms	550 µs	100 µs	1.0ms

PERFORMANCE TESTS

4–20 DUTY CYCLE (sine, triangle, square)

SPECIFICATION

Range: 10 % to 90 % (1 mHz to 999 kHz)
20 % to 80 % (1 MHz to 9.99 MHz)
Accuracy: ± 0.5 digits (1 mHz to 999 kHz)
± 3.0 digits (1 MHz to 9.99 MHz)

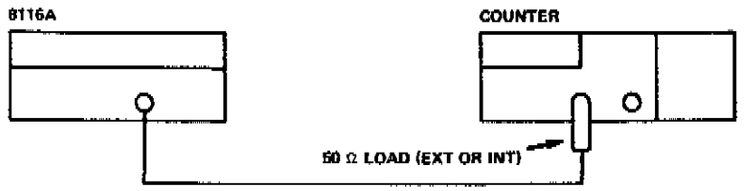


Figure 4–14. Test setup for Duty Cycle

EQUIPMENT

Counter
Cable Assembly BNC (1 x 61 cm)

PROCEDURE

1. Connect the equipment as shown in Figure 4–14.

2. Set 8116A as follows:

INPUT MODE	NORM
FUNCTION	SQUARE
CTRL	OFF
AMP	1.0 V
OFS	0.0 V
OUTPUT MODE	NORM

3. Set the counter to DTY CY A. Set 8116A duty cycle / frequency as shown and verify counter duty cycle readings.

FREQUENCY	DUTY CYCLE	COUNTER READING
1 Hz	10 %	9.5 % to 10.5 %
	50 %	49.5 % to 50.5 %
	90 %	89.5 % to 90.5 %
1 kHz	10 %	9.5 % to 10.5 %
	50 %	49.5 % to 50.5 %
	90 %	89.5 % to 90.5 %
9.99 MHz	20 %	17.0 % to 23.0 %
	50 %	47.0 % to 53.0 %
	80 %	77.0 % to 83.0 %

PERFORMANCE TESTS

4–21 SWEEP (Opt. 001 only)

SPECIFICATION

Logarithmic sweep for all waveforms up to full range (1 mHz to 50 MHz) between selected start and stop frequency. Sweep time per decade selectable in 1–2–5 sequence between 10 ms and 500 s.

EQUIPMENT

Realtime scope
Pulse Generator
Cable Assembly BNC (3 x 61 cm)

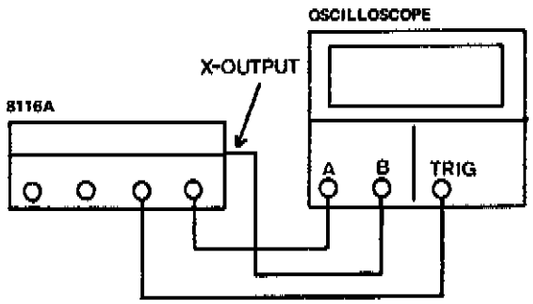


Figure 4–15. Test setup for SWEEP

PROCEDURE

1. Connect equipment as shown in Figure 4–15.

2. Set the 8116A as follows:

INPUT MODE	E.SWP
FUNCTION	SINE
CTRL	OFF
STA	10 kHz
STP	10 MHz
SWT	2 s/decade
MRK	1.0 MHz
AMPLITUDE	1.0 V
OFFSET	0.0 V
OUTPUT MODE	NORM

3. Set the channel B vertical scale to 1.0 V/division and the scope timebase to 50 us/division. Verify that the frequency of the displayed sinewave on Channel A is 10 kHz.

4. Press the MAN pushbutton on the 8116A frontpanel and confirm that
   a) the 8116A displays IP
   b) the frequency of the displayed signal increases
   c) the level of the X-OUTPUT gradually rises from 0 V to 4.5 V during the sweep time (6 seconds).

5. Adjust the scope timebase to 50 ns/division and verify that the frequency of the displayed sinewave on channel A is 10 MHz.

6. Disconnect the X-OUTPUT of the 8116A from the scope and connect the MARKER OUTPUT in its place. Press MAN to return to the start frequency.
   Press MAN again to begin the sweep, and note that the MARKER OUTPUT switches instantaneously when the marker frequency (1 MHz) has been reached (4 seconds after the sweep was initiated).

7. Select I.SWP at the 8116A frontpanel. Verify that the internal sweep is running, and that the start, stop and marker frequencies, sweep time/decade and X-OUTPUT are identical to the previously set values.

PERFORMANCE TESTS

4–22 DC VOLTAGE (all waveform keys deactivated)

SPECIFICATION

Range: 0 V to ± 7.95 V
Resolution: 3 digits (best case 1 mV)
Accuracy: ± 0.5 % of setting ± 20 mV

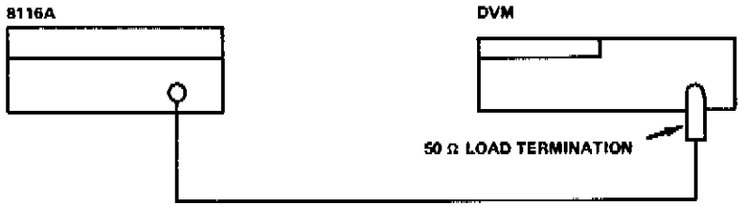


Figure 4–16. Test setup for DC Voltage

EQUIPMENT

Digital Voltmeter
Cable Assembly BNC (1 x 61 cm)

PROCEDURE

1. Connect the equipment as shown in Figure 4–16.

2. Set 8116A as follows:

INPUT MODE	NORM
FUNCTION	OFF
CTRL	OFF
OUTPUT MODE	NORM

3. Set 8116A AMP and OFS values as shown and verify DVM reading.

AMP	OFS	DVM READING
+100 mV	+7.95 V	+7.890 V – +8.010 V
+100 mV	+5.00 V	+4.955 V – +5.045 V
+100 mV	+2.00 V	+1.970 V – +2.030 V
+100 mV	0.00 V	–0.020 V – +0.020 V
+100 mV	–2.00 V	–2.030 V – –1.970 V
+100 mV	–5.00 V	–5.045 V – –4.955 V
+100 mV	–7.95 V	–8.010 V – –7.890 V

PERFORMANCE TESTS

4–23 MAN, 1 CYCLE, LIMIT, COMPLEMENT and DISABLE OPERATION

FUNCTION AND CAPABILITY

MAN: Simulates external input.

1 CYCLE: (Opt. 001 only). Provides a single output period in EXT BURST mode.

AUTO: In NORM mode, all parameters can be automatically incremented or decremented with selectable resolution. Pushing the AUTO button activates the AUTO vernier, which can then be started with the selected vernier key. AUTO vernier stop is accomplished by an external trigger input or pushing AUTO.

LIMIT: Maximum high and low levels into 50 Ohm can be limited to protect the device under test. Pushing the LIMIT key will set the limits to the actual levels, which then cannot be exceeded as long as the mode is active.

COMPL: Switch-selectable normal/complement output.

DISABLE: Relay disconnects all output circuitry.

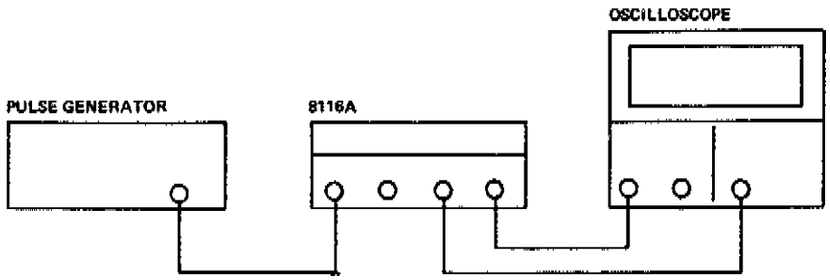


Figure 4–17. Test setup

EQUIPMENT

Realtime scope
Counter
Pulse Generator
Cable Assembly BNC (3 x 61 cm)

PROCEDURE

1. Connect equipment as shown in Figure 4–17.

2. Set 8116A as follows:

INPUT MODE	NORM
FUNCTION	SQUARE
CTRL	OFF
FREQUENCY	1 kHz
HIL	1.0 V
LOL	0.0 V
OUTPUT MODE	NORM
DUTY CYCLE	10 %
TRIG SLOPE	NOT SELECTED

NOTE: The Autovernier acts upon the LAST selected parameter.

PERFORMANCE TESTS

3. Adjust the scope timebase to 0.2 ms/div and select AUTO at the 8116A frontpanel. Press the upper section of the right hand VERNIER key and verify that the duty cycle of the 8116A output is incremented to 90 %. Press the lower section of the left-hand VERNIER key and verify that the duty cycle decremented to 10 %. Deselect the AUTO pushbutton. Ensure that no Ext. Input Slope is selected.

4. Press the COMPL pushbutton and verify that the 8116A output becomes inverted. Deselect the COMPL pushbutton.

5. Select DISABLE at the 8116A frontpanel and confirm that the output is withdrawn.

6. Make the following adjustments to the 8116A frontpanel settings:
OPT. 001

INPUT MODE	EXT BURST
FUNCTION	PULSE
CTRL	OFF
BUR	123
FREQUENCY	100 Hz
WIDTH	5 us
AMP	4.0 V
OFS	0.0 V
OUTPUT MODE	LIMIT

7. Disconnect the scope and connect the counter in its place. Set the Counter to TOT A. Reset the counter and enable the GATE. Press MAN. Verify that the counter reads 123. Note that 5345A counter will read 122, since the first pulse arms the counter.

8. OPT. 001 ONLY — Deselect the EXT INPUT trigger and reset the counter. Press the 1 CYCLE key on the 8116A frontpanel. Confirm that the counter reading is 124. Reset the counter and press the MAN key on the 8116A frontpanel. Verify that the new counter reading is 123.

9. Select the AMP parameter on the 8116A frontpanel. Verify that pressing the VERNIER keys will not increase the amplitude of +4.0 V set previously. Similarly, when OFS is selected, verify that the previously set level of 0.0 V cannot be made more negative by action of the VERNIER keys.

PERFORMANCE TESTS

4–24 HP-IB CAPABILITY

EQUIPMENT

System Controller
Realtime scope
HP-IB Cable Assembly
Cable Assembly BNC (1 x 61 cm)

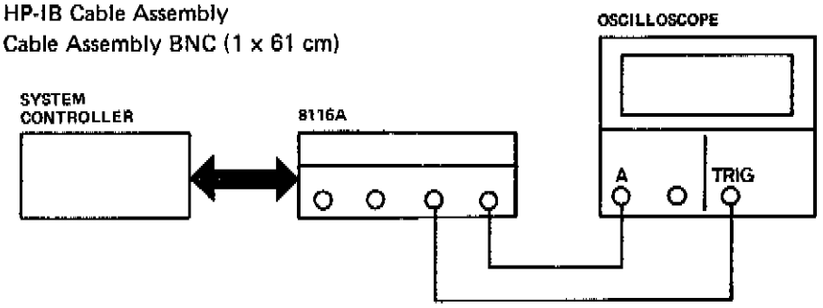


Figure 4–18. Test setup for HP-IB capability

PROCEDURE

1. Connect equipment as shown in Figure 4–18.

2. Type the following instructions to the 8116A via the system controller:

```
REMOTE 716
CLEAR 716
DIM A$ [161]
OUTPUT 716; "CST"
ENTER 716; A$
PRINT A$
```

3. Verify that the controller output is as follows:

```
M1,CT0,T1,W1,H0,A0,L0,C0,D1,BUR
0001 #,RPT 100 MS,STA 1.00 KHZ,
STP 100 KHZ,SWT 50.0 MS,MRK 1.00 KHZ,
FRQ 1.00 KHZ, DTY 50 %, WID 500 US,
HIL +0.50 V, LOL –0.5 V
```

4. Type the following instruction to the 8116A via the controller:

```
OUTPUT 716; "FRQ 10 KHZ, DTY 10 %,
            W3, HIL 1.5 V"D0"
DIM B$ [161]
OUTPUT 716; "CST"
ENTER 716; B$
PRINT B$
```

5. Verify that the controller printer output data matches the data previously output in step 3, except for the following changes:

```
FRQ 10.0 KHZ
DTY 10 %
HIL 1.50 V
W3
D0
```

5. Check the scope display to confirm that the 8116A output waveform has the following parameters:

SQUARE, Frequency 10 kHz, Duty Cycle 10 %,
High Level 1.50 V, Low Level –0.50 V.

PERFORMANCE TESTS

Table 4–1. Performance Test Record

Hewlett-Packard Company
Model 8116A/8116A Option 001
Programmable Signal Source
Serial No. _____

Tested By _____

Date _____

Para. No.	Test Description		Results Min	Actual	Max
4–10	Frequency				
		50.0 MHz	47,5 MHz	_____	52,5 MHz
		10.0 MHz	9,5 MHz	_____	10,5 MHz
		10.0 kHz	9,7 kHz	_____	10,3 kHz
		1.00 kHz	0,97 kHz	_____	1,03 kHz
		1.00 Hz	0,967 ms	_____	1,033 ms
		100 mHz	9,66 ms	_____	10,33 ms
4–11	Pulse Width				
		100 ns	93 ns	_____	107 ns
		1 µs	948 ns	_____	1052 ns
		100 µs	95 µs	_____	105 µs
		1 ms	950 µs	_____	1050 µs
		500 ms	475 ms	_____	525 ms
		8 ns	7.5 ns	_____	10 ns
4–12	Burst (Option 001) only Number of actual output cycles same as set burst length ?			yes/no	
4–13	Amplitude and Offset				
	AMPL	FUNCTION			
	8.00 V	sine *	2.69 V	_____	2.97 V
		triangle *	2.19 V	_____	2.43 V
		square *	3.8 V	_____	4.2 V
	3.00 V	sine *	1.008 V	_____	1.114 V
		triangle *	0.823 V	_____	0.909 V
		square *	1.425 V	_____	1.575 V
	1.00 V	sine *	0.336 V	_____	0.372 V
		triangle *	0.275 V	_____	0.303 V
		square *	0.475 V	_____	0.525 V
	100 mV	sine *	33.6 mV	_____	37.1 mV
		triangle *	27.4 mV	_____	30.3 mV
		square *	47.5 mV	_____	52.5 mV

PERFORMANCE TESTS

Para No.	Test Description	Results		
		Min	Actual	Max
4–13	OFFSET			
	7.5 V	7,421 V	_____	7,578 V
	5.00 V	4,934 V	_____	5,066 V
	3.00 V	2,944 V	_____	3,056 V
	1.00 V	0,954 V	_____	1,046 V
	100 mV	58 mV	_____	142 mV
4–14	Sine Characteristics (Harmonic level)			
	FRQ = 1 kHz (2^{nd} harmonic)		_____	–42 dB
	FRQ = 1 kHz (3^{rd} harmonic)		_____	–47 dB
	FRQ = 1 MHZ (THD)		_____	1 %
	FRQ = 50 MHz (worst harmonic)		_____	–23 dB
4–15	Pulse Characteristics			
	Leading edge		_____	≤ 6 ns
	Trailing edge		_____	≤ 6 ns
	Preshoot	≤ –5 %	_____	≤ +5 %
	Overshoot and ringing	≤ –5 %	_____	≤ +5 %
4–16	Trigger, Gate, E.Width			
	Positive trigger releases one complete output cycle ?		yes/no	
	Positive gate releases a burst of output cycles, fast cycle complete ?		yes/no	
	Positive pulse releases a pulse of same width ?		yes/no	
4–17	FM Mode Jitter, FM on		_____	
4–18	Amplitude Modulator (worst harmonic)		_____	–42 dB
4–19	Pulse Width Modulator			
	10 ns → 100 ns		yes/no	
	100 μs → 1.0 ms		yes/no	
	100 ms → 1.0 s		yes/no	

PERFORMANCE TESTS

Para. No.	Test Description	Results		
		Min	Actual	Max
4–20	DUTY CYCLE			
	FRQ DTY CY			
	10 %	9.5 %	_____	10.5 %
	1 Hz 50 %	49.5 %	_____	50.5 %
	90 %	89.5 %	_____	90.5 %
	10 %	9.5 %	_____	10.5 %
	1 KHz 50 %	49.5 %	_____	50.5 %
	90 %	89.5 %	_____	90.5 %
	20 %	17.0 %	_____	23.0 %
	9.99 MHz 50 %	47.0 %	_____	53.0 %
	80 %	77.0 %	_____	83.0 %
4–21	SWEEP (Opt. 001 only)			
	frequency 10 kHz		yes/no	
	'IP' displayed		yes/no	
	frequency increases		yes/no	
	X-OUTPUT 0 V → 4.5 V in 6 seconds		yes/no	
	10 MHz		yes/no	
	Verify 3, 4 and 5		yes/no	
	MARKER OUTPUT functional ?		yes/no	
	Internal sweep running ?		yes/no	
	STA, STP, SWT, MRK and X-OUTPUT functional ?		yes/no	
4–22	D.C. VOLTAGE			
		+7.890 V	_____	+8.010 V
		+4.955 V	_____	+5.045 V
		+1.970 V	_____	+2.030 V
		–0.020 V	_____	+0.020 V
		–2.030 V	_____	–1.970 V
		–5.045 V	_____	–4.955 V
		–8.010 V	_____	–7.890 V
4–23	MAN, 1 CYCLE, LIMIT, COMPL and DISABLE			
	AUTOVERNIER functional ?		yes/no	
	COMPL functional ?		yes/no	
	DISABLE functional ?		yes/no	
	MAN Reading 123 ?*		yes/no	
	1 CYCLE Reading 124 ?*		yes/no	
	LIMIT functional ?		yes/no	
4–24	HP-IB functional ?		yes/no	

* (5345A reading will be 122/123, since the first pulse arms the counter)

Related Paragraph	Component	Range of values	Description
Overshoot/ Transition Times	A1 C530	jumper or 1 pF	jumper increases overshoot
	A1 C525	1.5 pF – 6.8 pF	decreasing C 525 value increases transition times
Voltage Controlled Oscillator	A1 R220/R223	1.5 k – 4.02 k	increasing R220/223 values increases amplitude flatness
	A1 R242	1.0 k – 1.3 k	Baseline accuracy in TRIG Mode and startphase 0'
Width	A1 R309	1 Ohm – 100 Ohm	increasing R309 value decreases min. Width (< 10 ns)
	A1 R310	1 k, 2K or open	change, if min. and max. Widths are not adjustable
	A1 R157	4.5 k – 5.56 k	increasing R157 value decreases Width in PWM Mode
Shaper	A1 R439	7.5 k – open	increasing R439 value increases offset in normal Mode and decreases offset in complement Mode
	A1 R428	10 k – open	decreases 2nd harmonic at 1.00 V amplitude (increasing R428 decreases negative offset)

Table 5–1. * Values

NOTE: All resistors are 0.125 W, ± 1 %

SECTION V
ADJUSTMENT PROCEDURE

5–1 INTRODUCTION

This section describes the adjustments which will return the instrument to peak operating condition after repairs are completed. An adjustment location diagram is given on a fold-out page at the end of this section.

5–2 SAFETY CONSIDERATIONS

Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition (see Sections II and III).

WARNING

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnection of the protective earth terminal is likely to make the instrument dangerous. Intentional interruption is prohibited.

Any adjustment, maintenance, or repair of the opened instrument with voltage applied should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

5–3 EQUIPMENT REQUIRED

The test equipment required for the adjustment procedure is listed in Table 1–1, Recommended Test Equipment. The critical specifications of substitute test instruments must meet or exceed the standards listed in the table if the instrument is to meet the standards set forth in Table 1–2, Specifications.

5–4 ADJUSTMENT PROCEDURE

The adjustment procedure is divided into the following sections:

5–6 Power Supplies
5–7 Pre-adjustments
5–8 Overshoot/Transition Times
5–9 Voltage Controlled Oscillator
5–10 Width
5–11 Shaper
5–12 Offset
5–13 Amplitude Modulator

When repairs have been made, paragraph 5–6 Power Supplies should always be checked. If readjustment is necessary, the whole adjustment procedure should be carried out.

Of the remaining paragraphs, only those which the repairs could affect need to be completed. Execute a paragraph completely and in the order in which it is presented. Only the significant instrument settings are given.

Allow 1 hour warm-up time before starting the adjustments.

5–5 ADJUSTMENTS

Set 8116A into service position as shown in Figure 5–1. At beginning of the procedure load the 8116A with its standard setting which is done by setting the 8116A to

MODE . . . . . E.WID
OUTPUT . . . . . sine

then turning the instrument off and on again.

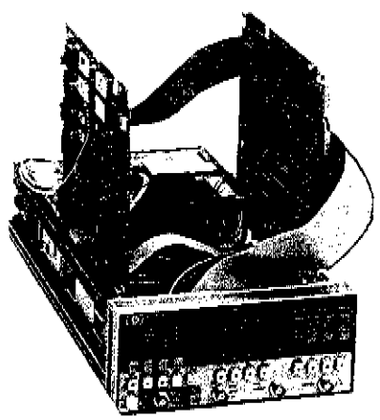


Figure 5–1. 8116A service position

If the 8116A is completely disarranged, it is recommended to turn A1R413 fully CW and A1R418 fully CCW, all other adjustment pots into their mid position.

5–6 POWER SUPPLIES

EQUIPMENT
Digital Voltmeter

PROCEDURE

1. Connect DVM low terminal to ground testpoint on A1 and measure the power supply output voltages.
2. Adjust supply voltages as follows:

TP	Adjust	Result
A1 +15 V	A1R24	+15.00 V ± 15 mV
A1 –5.2 V	A1R12	– 5.25 V ± 10 mV
A3 +5.0 V	check	+ 5.15 V ± 50 mV
A1 +5.0 V	check	+ 5.05 V ± 50 mV
A1 +24 V	A1R18	+24.00 V ± 50 mV
A1 -24 V	A1R19	–24.00 V ± 50 mV
A1 –15 V	A1R25	–15.00 V ± 15 mV

5–7 PRE-ADJUSTMENTS

EQUIPMENT
Real Time Scope

PROCEDURE
Square High Amplitude/Offset

1. Set 8116A:

MODE . . . . . NORM
FRQ . . . . . 100 kHz
DTY . . . . . 50 %
AMP . . . . . 16.0 V
OFS . . . . . 0.00 mV
OUTPUT . . . . . square, enabled

Connect 8116A output via 50 Ohm (2 W) feedthrough to Real Time Scope (2 V/Div.)

Adjust A1R410/R425 for a symmetrical 8 Div. signal.

Triangle high Amplitude/Offset

2. Set 8116A:

OUTPUT . . . . . triangle, enabled

Adjust A1R227/R401 for a symmetrical 8 Div. signal.

Sine high Amplitude/Offset

3. Set 8116A:

OUTPUT . . . . . sine, enabled

Adjust A1R418/R402 for a symmetrical 8 Div. signal.
Adjust A1R409 for optimal sinewave signal.

Square low Amplitude/Offset

4. Set 8116A:

AMP . . . . . 1.00 V
OFS . . . . . 0.00 mV
OUTPUT . . . . . square, enabled

Set Real Time Scope to 200 mV/Div.
Turn A1 R450 fully CCW then adjust A1 R450/R416 for a symmetrical 5 Div. signal.

Sine low Amplitude

5. Set 8116A:

OUTPUT . . . . . sine, enabled

Turn A1R445 fully CCW then adjust A1R445 for a 5 Div. signal.

Low Frequency Pulse Performance

6. Set 8116A:

FRQ . . . . . 1 kHz
OUTPUT . . . . . square, enabled

Adjust A1R515 for optimal squarewave signal.

5–8 OVERSHOOT/TRANSITION TIMES

EQUIPMENT
Sampling scope

PROCEDURE

1. Set 8116A:

MODE	NORM
FRQ	10.0 MHz
DTY	50 %
AMP	1.60 V
OFS	0.00 mV
OUTPUT	triangle, enabled

Connect 8116A output to Sampling Scope.
Preadjust A1R535 for linear triangular waveform.

2. Set 8116A;

AMP	16.0 V
OUTPUT	square, normal/complement as required enabled

Connect 8116A output via 20 dB attenuator to Sampling Scope. Adjust A1C529 for overshoot < 4 % in both normal and complement modes.

3. Set 8116A:

AMP	1.00 V

Connect 8116A output without 20 dB attenuator to Sampling Scope. Adjust A1R535 for overshoot < 4 % in both normal and complement modes.

4. Set 8116A:

AMP	16.0 V

Connect 8116A output via 20 dB attenuator to Sampling Scope. Check that overshoot < 4 %. If necessary, readjust A1R535.

5. Set 8116A:

AMP	1.00 V

Connect 8116A output without 20 dB attenuator to sampling scope. Check that transition times < 5.6 ns for both normal and complement modes.

6. Set 8116A:

AMP	999 mV

Check that transition times < 5.6 ns for both normal and complement modes.

7. Set 8116A:

AMP	1.00 V
OFS	+7.50 V

Connect 8116A output via 20 dB attenuator to Sampling Scope. Check that transition times < 5.6 ns for both normal and complement modes.

Note: Transition times can be increased by increasing the overshoot. If Overshoot/Transition Times Adjustment cannot be achieved within specifications change * values A1C525, A1C530 (see table 5–1).

5–9 VOLTAGE CONTROLLED OSCILLATOR

EQUIPMENT
Counter, Sampling Scope, HF Spectrum Analyzer

PROCEDURE

Frequency/Duty Cycle (100 Hz – 999 kHz)

1. Set 8116A:

MODE	NORM
FRQ	1.00 kHz
DTY	50 %
AMP	999 mV
OFS	0.00 mV
OUTPUT	triangle, enabled

Set Counter: Time Interval A⟶ B
Slope A ⌐
Slope B ¬
COM A
Trigger level 1.2 V

Connect 8116A trigger output via 50 Ohm feedthrough (or internal 50 Ohm termination) to counter.

Adjust A1 R22 for 500 us ± 0.5 us

2. Set 8116A:

FRQ . . . . . 9.99 kHz

Adjust A2R24 for 50.05 us ± 0.05 us.

3. Repeat steps 1. and 2. until values remain within the given limits.

4. Set 8116A:

FRQ . . . . . 1.00 kHz

Set Counter: Slope A ↘
Slope B ↗

Adjust A2R25 for 500 us ± 0.5 us.

5. Set 8116A:

FRQ . . . . . 9.99 kHz

Adjust A2R27 for 50.05 us ± 0.05 us

6. Repeat steps 4. and 5. until values remain within the given limits.

High Frequency (1 .... 9.99 MHz Range)

7. Set 8116A:

FRQ . . . . . 9.99 MHz

Set Counter: Frequency A

Adjust A1C204 for 9.99 MHz ± 0.1 MHz

Flatness

8. Set 8116A:

FRQ . . . . . 1.00 MHz
AMP . . . . . 999 mV
OUTPUT . . . . . triangle, enabled

Connect 8116A output without 20 dB attenautor to Sampling Scope. Adjust Sampling Scope for 100 % display. Step 8116A up to 9.99 MHz. Observe amplitude flatness. The amplitude must decrease by 2 % to 4 %. Otherwise change* values A1R220/223 (see table 5–1).

High Frequency (10 ..... 50 MHz Range)

9. Set 8116A;

FRQ . . . . . 10.0 MHz

Connect 8116A trigger output via 50 Ohm feedthrough (or internal 50 Ohm termination) to Counter.

Adjust A1R17 for 10.00 MHz ± 0.03 MHz.

10. Set 8116A:

FRQ . . . . . 2.00 MHz
DTY . . . . . 50 %
AMP . . . . . 999 mV
OFS . . . . . 0.00 mV
OUTPUT . . . . . triangle, enabled

Connect 8116A output without 20 dB attenuator to Sampling Scope. Adjust Sampling Scope for 100 % display.

11. Set 8116A:

FRQ . . . . . 50 MHz

Adjust A1R221/R224 for 51.0 MHz ± 0.5 MHz on counter and symmetrical output on Sampling Scope as shown in Figure 5–2.

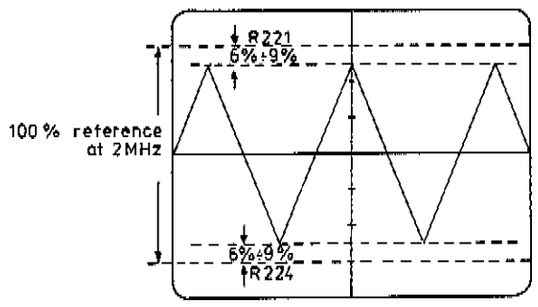


Figure 5–2. HF symmetry adjust

12. Connect 8116A output to HF Spectrum Analyzer (50 Ohm Termination). Readjust A1R221 for min. 2nd harmonic distortion with respect to best compromise between normal and complement mode. Readjust A1 R224 for 51.0 MHz ± 0.5 MHz on counter.

13. Connect 8116A output to Sampling Scope. Check that the amplitude flatness is −10 % to −18 % corresponding to the 2 MHz reference.

    The signal may not necessarily be symmetrical.

14. Set 8116A:

    FRQ . . . . . 42.0 MHz

    Check that frequency < 43.5 MHz.

15. Check that amplitude flatness from 40 MHz to 50 MHz > −20 % (100 % reference at 2 MHz).

16. Set 8116A:

    FRQ . . . . . 10.0 MHz
    OUTPUT . . . . . square, enabled

    Adjust A1R130 for 50 % ±10% Duty Cycle.

Low Frequency (1 mHz – 99.9 Hz)

17. Set 8116A:

    FRQ . . . . . 99.9 Hz
    DTY . . . . . 50 %
    AMP . . . . . 1.00 V
    OFS . . . . . 0.00 mV
    OUTPUT . . . . . square, enabled

    Adjust A2R18 for 99.9 Hz ± 0.1 Hz on Counter.

18. Set 8116A:

    FRQ . . . . . 9.99 Hz

19. Adjust A2R2 for 9.99 Hz ± 0.025 Hz.

20. Adjust A2R4 for Duty Cycle 50.00 % ± 0.2 %.

    Note: If counter has no Duty Cycle Mode, use Time Interval Measurement from leading to trailing edge and from trailing to leading edge. The difference between both must be < 0.4 ms.

21. Repeat steps 19. and 20. until values remain within the given limits.

5–10 WIDTH

EQUIPMENT
Counter, Sampling Scope

PROCEDURE

1. Set 8116A:

    MODE . . . . . NORM
    FRQ . . . . . 900 Hz
    WID . . . . . 100 us
    AMP . . . . . 1.00 V
    OFS . . . . . 0.00 mV
    OUTPUT . . . . . pulse, normal, enabled

    Set Counter: Time Interval A –> B
    Slope A ⌐
    Slope B ⌙
    COM A
    Trigger level 0 V

    Connect 8116A output via 50 Ohm feedthrough (or 50 Ohm termination of Counter) to Counter.

    Adjust A2R32 for 98.0 us + 2 us/−1 us.

2. Set 8116A:

    WID . . . . . 999 us

    Adjust A1R304 for 980 us + 20 us / − 10 us.

3. Repeat steps 1. and 2. until values remain within the given limits.

4. Set 8116A:

    WID 400µs

    Check that width > 386 µs.
    If not, repeat steps 1. and 2.

5. Set 8116A:

    FRQ . . . . . 100 kHz
    WID . . . . . 99.9 ns

    Adjust A2R31 for 99.9 ns ± 1 ns.

6. Set 8116A:

WID . . . . . 100 ns

Check width for 100 ns ± 5 ns.

7. Set 8116A:

FRQ . . . . . 10.0 MHz
WID . . . . . 8.0 ns

Connect 8116A output to Sampling Scope.
Check that 7.5 ns < Width < 10 ns.

8. Set 8116A:

MODE . . . . . NORM
CRTL . . . . . PWM
FRQ . . . . . 1.00 kHz
WID . . . . . 550 us
AMP . . . . . 1.00 V
OFS . . . . . 0.00 mV
OUTPUT . . . . . pulse, normal, enabled

Connect 8116A output via 50 Ohm feedthrough to Counter. (Or use internal 50 Ohm termination of the counter).

Check that width equals 550 us ± 20 us.
If not, change * value A1R157 (see table 5–1).

5–11 SHAPER

EQUIPMENT

Digital Voltmeter (RMS), LF Spectrum Analyser, Low Pass Filter as shown in figure 5–3.

PROCEDURE

1. Turn A1R413 fully CW
   Turn A1R418 fully CCW

Square Amplitude

2. Set 8116A:

MODE . . . . . NORM
FRQ . . . . . 1.00 kHz
DTY . . . . . 50 %
AMP . . . . . 9.99 V
OFS . . . . . 0.00 mV
OUTPUT. . . . . square, normal enabled

Set DVM: AC, 10 V Range

Connect 8116A output via 50 Ohm feedthrough to DVM. Adjust A1R410 for 5.055 V ± 25 mV RMS.

3. Set 8116A:

AMP . . . . . 16.0 V

Check amplitude > 8.080V (typ. 8.082 V).

4. Set 8116A:

AMP . . . . . 1.00 V

Adjust A1R450 for 0.506 V ± 2 mV RMS.

Square Normal/Complement Balance

5. Set 8116A:

AMP . . . . . 16.0 V
OFS . . . . . 0.00 mV
OUTPUT . . . . . square, normal/complement required, enabled

Set DVM: DC, 10 V Range.
Use DVM built in filter function, otherwise use set up as shown in figure 5–3.

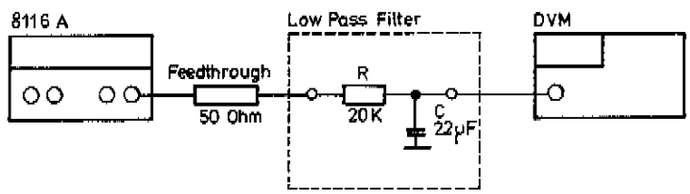


Figure 5–3. Low-pass filter test setup

Change 8116A output mode from normal to complement and back. Adjust A1R403 for minimum difference (<5 mV) between normal and complement output mode.

Triangle Amplitude

6. Set 8116A:

AMP . . . . . 9.99 V
OUTPUT . . . . . triangle, normal, enabled

Set DVM: AC, 10 V Range

Adjust A1R227 for 2.918 V ± 15 mV RMS

7. Set 8116A:

AMP . . . . . 16.0 V

Check that amplitude > 4.660 V.

2nd Harmonic Distortion

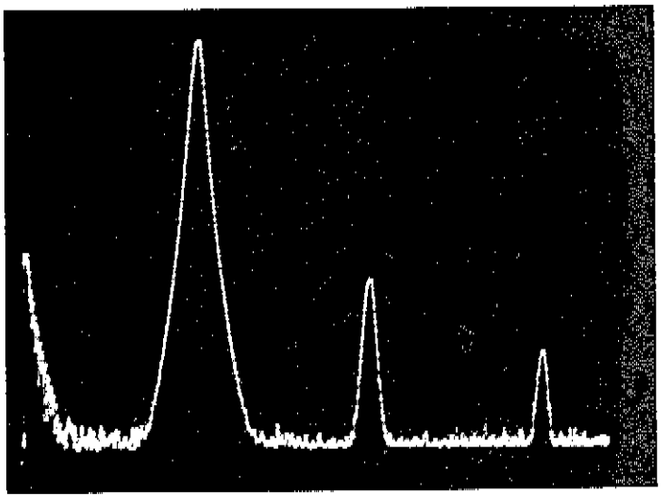
8. Set 8116A:

FRQ . . . . . 3.00 kHz
AMP . . . . . 16.0 V
OUTPUT . . . . . sine, normal/complement as required enabled

Connect 8116A output via 50 Ohm (2 W) feedthrough to LF Spectrum Analyzer adjusting the input amplifier so that the fundamental equals 0 dB on display.

Preadjust A1R409 for minimum 3rd harmonic in normal mode. Adjust A1R417 for minimum 2nd harmonic in normal mode. Change 8116A from normal to complement mode and back. Adjust A1R407 for minimum difference between the 2nd harmonics in normal and complement mode.

Note: 2nd harmonic should be < −48 dB for both normal and complement modes.
The difference between normal and complement mode must not exceed 5 dB. To achieve this, alternating adjustment of A1R417 and A1R407 may be necessary.



3kHz

Figure 5-4. 2nd harmonic distortion adjust.

Sine Normal/Complement balance

9. Set 8116A:

FRQ . . . . . 1.00 kHz
AMP . . . . . 16.00 V
OFS . . . . . 0.00 mV
OUTPUT . . . . . sine, normal/complement as required enabled

Set DVM: DC, 10 V Range

Connect 8116A output via 50 Ohm feedthrough to DVM. Use DVM built in filter function, otherwise use set-up as shown in figure 5−3.

Change 8116A output mode from normal to complement and back. Adjust A1R402 for minimum difference (< 5 mV) between normal and complement output mode

If the adjustment is not possible, change * value A1R439 (see table 5−1) and repeat the procedure from step 5.

Sine Amplitude/THD

10. Set 8116A:

FRQ . . . . . 1.00 kHz
AMP . . . . . 9.99 V

Set DVM: AC, 10 V Range

Connect 8116A via 50 Ohm feedthrough to DVM.
Adjust A1R418 for 3.532 V ± 10 mV RMS.

11. Set 8116A:

AMP . . . . . 1.00 V

Adjust A1R445 for 0.354 V ± 1 mV RMS.

12. Set 8116A:

FRQ . . . . . 3.00 kHz
AMP . . . . . 9.99 V
OUTPUT . . . . . normal

Connect 8116A output via 50 Ohm feedthrough to LF Spectrum Analyzer adjusting its input amplifier so that the fundamental equals 0 dB on display.
Adjust A1R409 for minimum 3rd harmonic.
It should be < −50 dB

13. Repeat steps 10 through 12 until values are within the given limits.

14. Set 8116A:

FRQ . . . . . 1.00 kHz
AMP . . . . . 16.0 V

Connect 8116A output via 50 Ohm feedthrough to DVM. Readjust A1R448 for 5.655 to 5.741 V RMS.

Triangle Normal/Complement Balance

15. Set 8116A:

FRQ . . . . . 1.00 kHz
AMP . . . . . 16.0 V
OFS . . . . . 0.00 mV
OUTPUT . . . . . triangle, normal/complement as required enabled

Set DVM: DC, 10 V Range

Connect 8116A output via 50 Ohm feedthrough to DVM, use built-in filter function, otherwise use set-up as shown in figure 5–3.

Change 8116A output mode from normal to complement and back. Adjust A1R401 for minimum difference (<5 mV) between normal and complement output mode.
If adjustment is not possible, change * value A1R439 (see table 5–1) and repeat the procedure from step 5.

Sine Offset

16. Set 8116A:

AMP . . . . . 16.0 V
OFS . . . . . 0.00 mV
OUTPUT . . . . . sine, normal, enabled

Adjust A1R425 for 0.00 V ± 10 mV.

17. Set 8116A:

AMP . . . . . 1.00 V

Adjust A1R416 for 0.00 V ± 5 mV.

Square low Amplitude

18. Set 8116A:

AMP . . . . . 1.00 V
OFS . . . . . 0.00 mV
OUTPUT . . . . . square, normal, enabled

Set DVM: AC, 10 V Range

Connect 8116A output via 50 Ohm feedthrough to DVM
Readjust A1R450 for 0.506 V ± 2 mV RMS.

THD Check

19. Set 8116A:

FRQ . . . . . 3.00 kHz
AMP . . . . . 1.00 V
OUTPUT . . . . . sine, normal / complement as required.

Connect 8116A output via 50 Ohm feedthrough to LF Spectrum Analyzer and adjusting the input amplifier so that the fundamental equals 0 dB on display.

Check that 2nd harmonic < –45 dB in both normal and complement modes.

20. Set 8116A;

FRQ . . . . . 50 MHz
AMP . . . . . 100 mV

Connect 8116A output to HF Spectrum Analyzer (50 Ohm feedthrough or termination) and adjust its input amplifier so that fundamental equals 0 dB on display.

Check that 2nd and 3rd harmonic < –27 dB in both normal and complement.

5–12 OFFSET

EQUIPMENT
Digital Voltmeter

PROCEDURE

1. Set 8116A:

MODE . . . . . NORM
FRQ . . . . . 1.00 kHz
DTY . . . . . 50 %
AMP . . . . . 100 mV
OFS . . . . . +7.95 V
OUTPUT . . . . . sine, normal, enabled

Set DVM: DC, 10 V Range

Connect 8116A output via 50 Ohm feedthrough to DVM. Use DVM built in filter function, otherwise use set-up shown in figure 5–3.
Adjust A2 R43 for +7.97 V ±30 mV.

2. Set 8116A:

OFS . . . . . –7.95 V

Check that offset equals –7.97 V ± 30 mV.

5–13 AMPLITUDE MODULATOR

EQUIPMENT
Signal Generator (THD < 0.1 %), Real Time Scope, LF Spectrum Analyzer

PROCEDURE

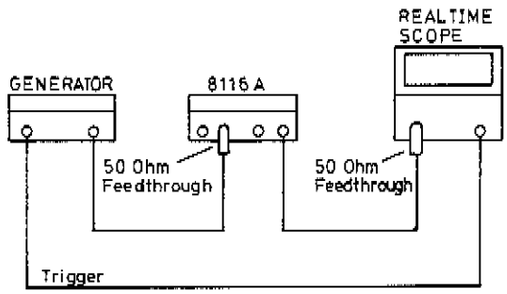


Figure 5–5. AM offset test setup

1. Set 8116A:

MODE . . . . . NORM
CRTL . . . . . AM
FRQ . . . . . 100 kHz
DTY . . . . . 50 %
AMP . . . . . 16.0 V
OFS . . . . . 0.00 mV
OUTPUT . . . . . sine, normal/complement as required enabled

Set Signal Generator:

FREQUENCY . . . . . 5.0 kHz
AMPLITUDE . . . . . ca. 5 V as required
OFFSET . . . . . 0 V
WAVEFORM . . . . . sine

Use set-up as shown in figure 5–5.

Adjust amplitude of signal generator so that the maximum amplitude of the 8116A modulated output signal equals 16 V on Real Time Scope display.

2. Change 8116A output mode from normal to complement and back. Adjust A1R414 for minimum offset difference at the 8116A modulated output signal's minimum amplitude between normal and complement mode:

3. Adjust A1R413 for the mean (medium) modulation between the actual modulation and 100 % modulation.

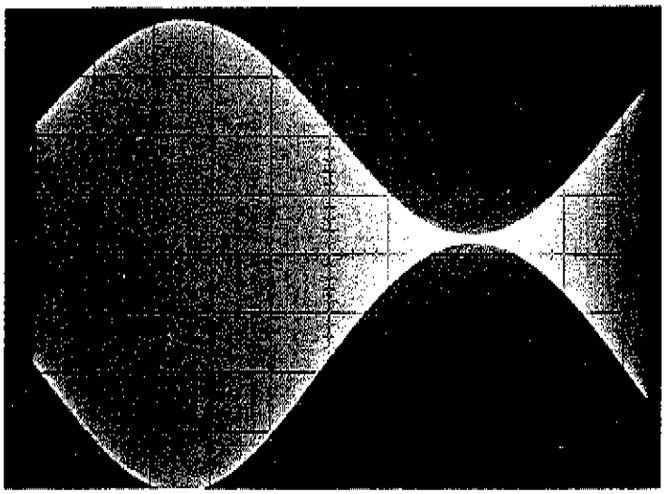


Figure 5–6 (a). Incorrect AM offset

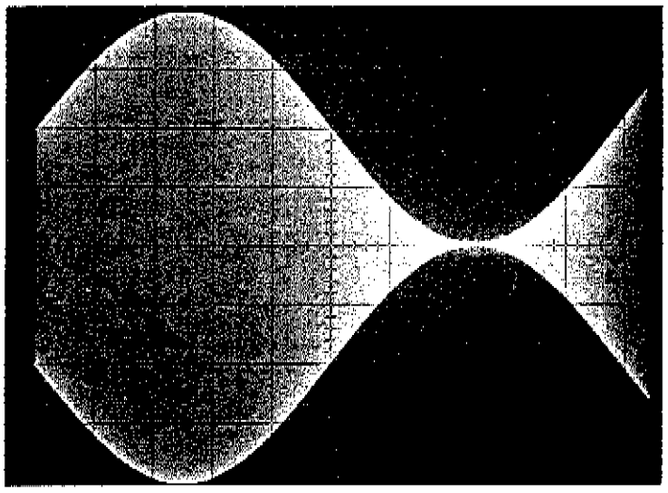


Figure 5–6 (b). Correct AM offset

4. Repeat steps 2. and 3. until 100 % modulation with minimum offset difference between normal and complement mode is reached.

5. Set 8116A:

FRQ . . . . . 15.0 kHz
OUTPUT . . . . . sine, normal, enabled

Set Signal Generator:

FREQUENCY . . . . . 2.0 kHz
AMPLITUDE . . . . . 4.5 V
OFFSET . . . . . 0.25 V
WAVEFORM . . . . . sine

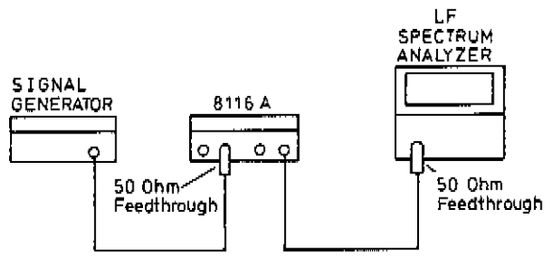


Figure 5–7. AM envelope test setup

Use set-up as shown in figure 5–7.

Adjust the Spectrum Analyzer to display the 15 kHz carrier and the lower sideband frequencies down to the 2 kHz modulating frequency. Adjust input amplifier of the Spectrum Analyzer so that the carrier equals 0 dB on display.

6. Adjust A1R414 for minimum 2 kHz modulating frequency.

7. Verify that envelope distortion < 40 dB. All harmonics of the sideband should be at least 42 dB lower than the modulation sidebands.

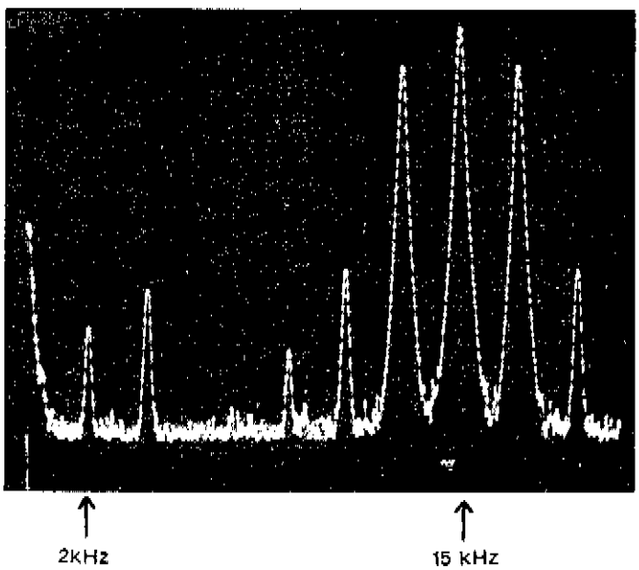


Figure 5–8. AM Envelope Distortion

8. Recheck and if necessary readjust steps 9., 11., 15. and 18. of paragraph 5–11 Shaper.

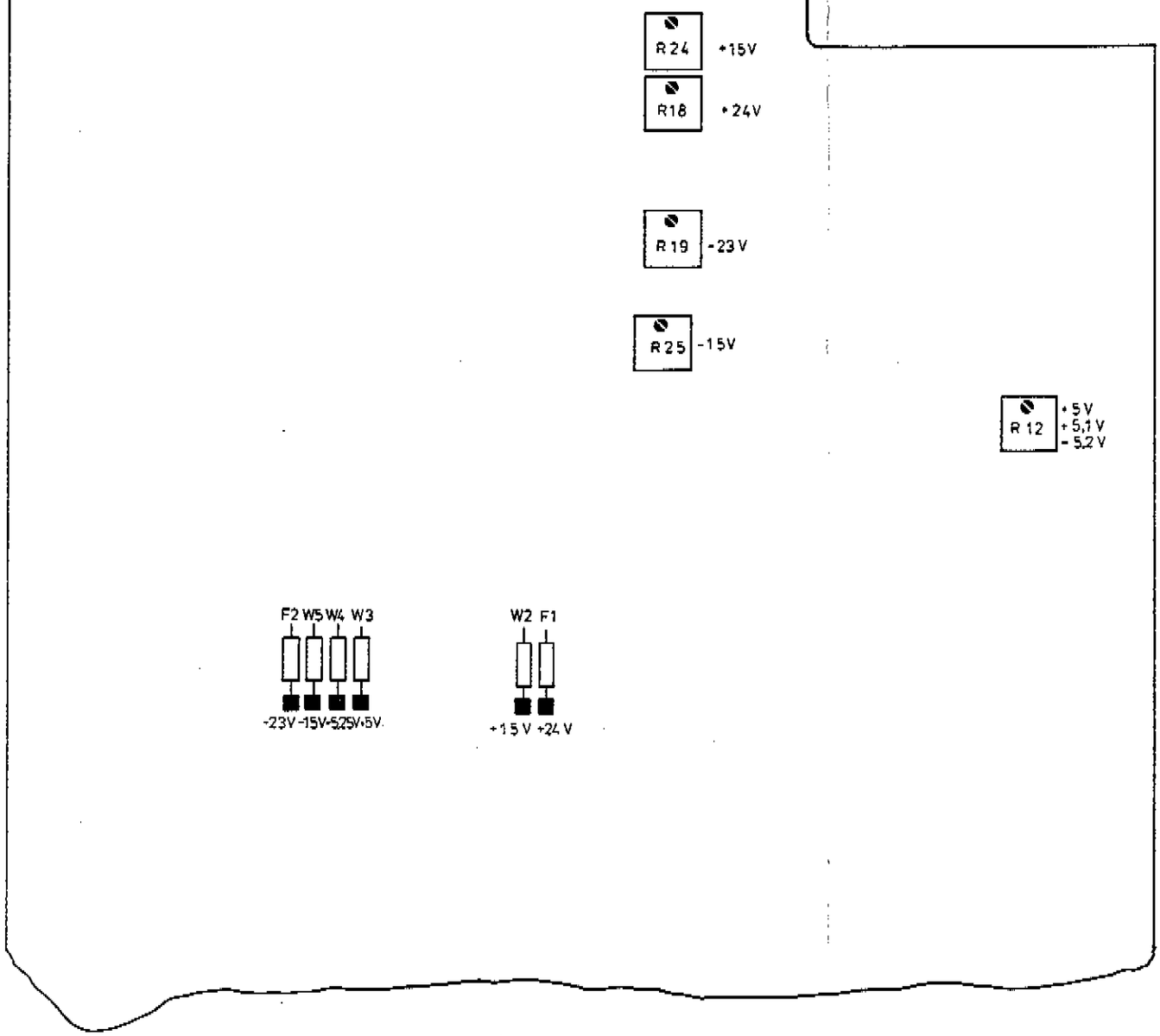
9. Verify again step 7.

BD ASSY
Sht 1 of 3

8	7	6	5	4	3	2	1

PART OF A1 BD ASSY
08116 - 66511

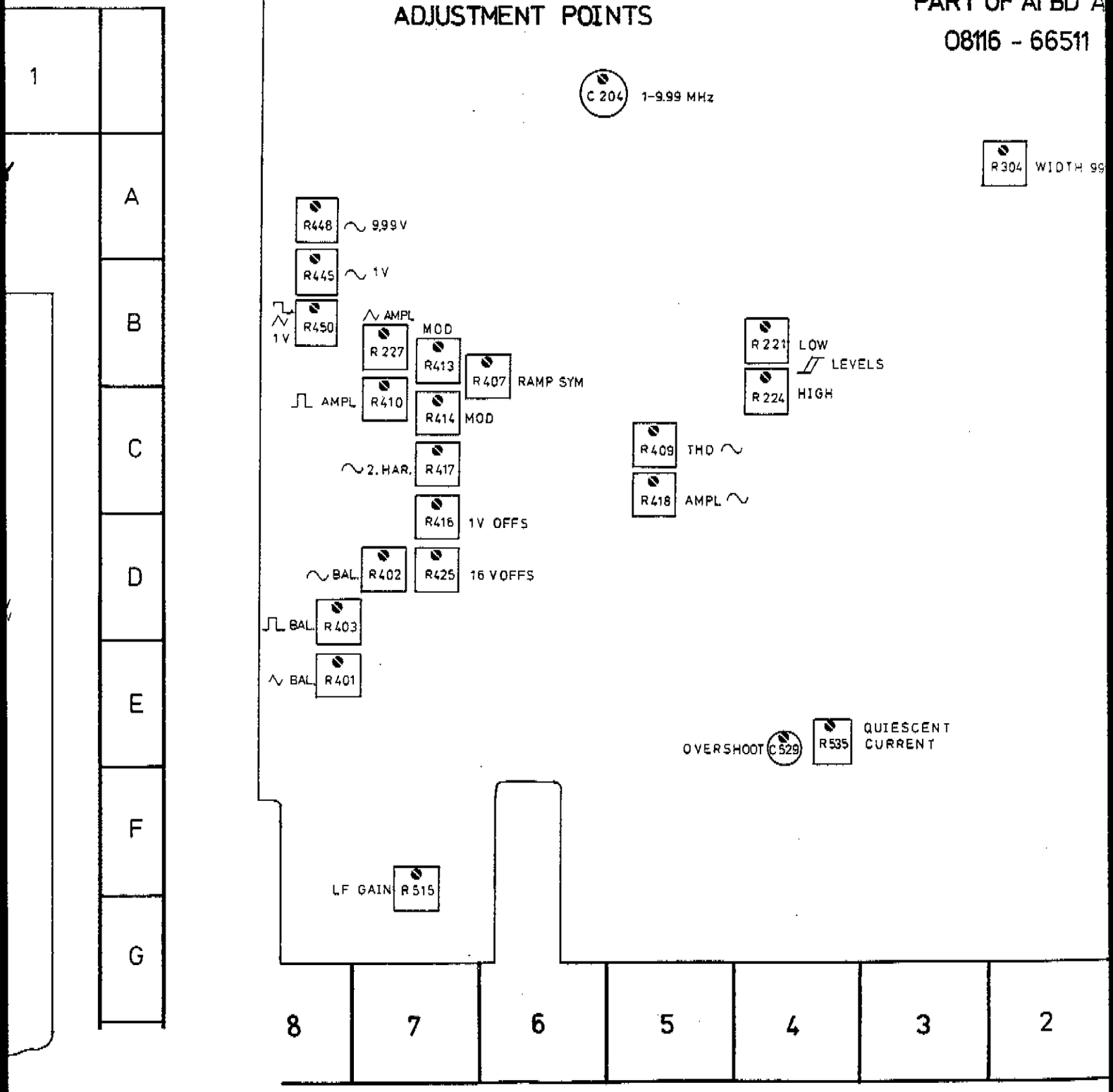
ADJUSTMENT POINTS

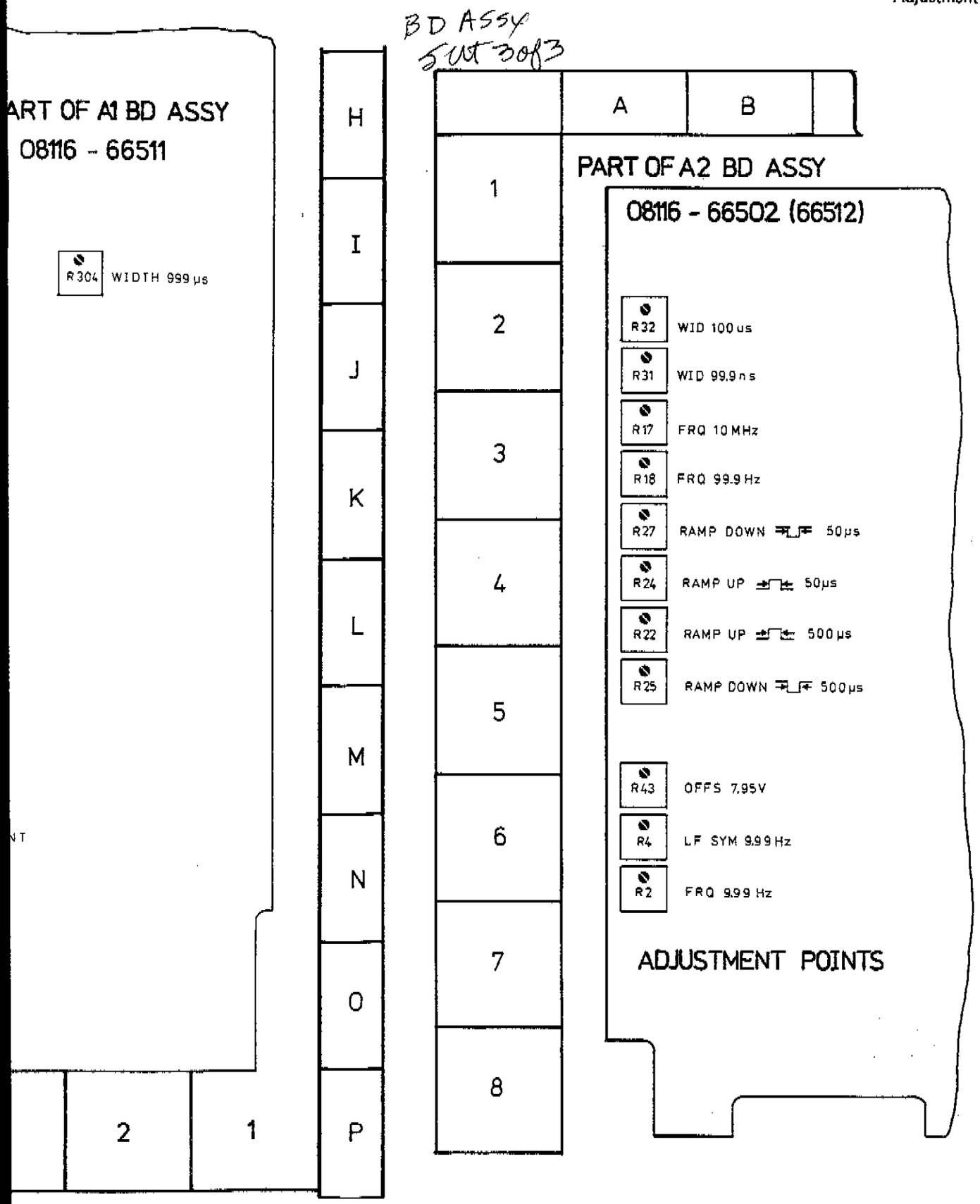


BD Assy
Sat2083

ADJUSTMENT POINTS

PART OF A1 BD A
08116 - 66511




BD ASSY
SHT 3 OF 3
ART OF A1 BD ASSY
08116 - 66511
R304 WIDTH 999 µs
H
I
J
K
L
M
N
O
P
2
1
A
B
1
2
3
4
5
6
7
8
PART OF A2 BD ASSY
08116 - 66502 (66512)
R32 WID 100 us
R31 WID 99.9 n s
R17 FRQ 10 MHz
R18 FRQ 99.9 Hz
R27 RAMP DOWN 50µs
R24 RAMP UP 50µs
R22 RAMP UP 500µs
R25 RAMP DOWN 500µs
R43 OFFS 7.95V
R4 LF SYM 9.99 Hz
R2 FRQ 9.99 Hz
ADJUSTMENT POINTS

SECTION VI
REPLACEABLE PARTS

6–1 INTRODUCTION

6–2 This section contains information for ordering parts. Table 6–1 lists abbreviations used in the parts lists and elsewhere in the manual. Table 6–3 lists all replaceable parts in reference designator order.

6–3 ABBREVIATIONS

6–4 Table 6–1 lists abbreviations used in the parts lists, schematics and elsewhere in the manual. In some cases two forms of the abbreviations are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts lists are always all capitals. However, in the schematics and other parts of the manual, the same abbreviations may have upper and lower case letters.

6–5 REPLACEABLE PARTS

6–6 Table 6–3 is the list of replaceable parts and is organised as follows:

a. Mainframe (chassis) parts in alphanumerical order by reference designation.
b. Electrical assemblies and their components in alpha-numerical order by reference designation.

Reference designators are of the form A3R9 i.e. resistor 9 assembly 3. The blue pages at the end of this section list the parts required for Option 001.

6–7 The information given for each part consists of the following:

a. The Hewlett-Packard part number.
b. The description of the part.
c. Part number check digit (CD).

6–8 ORDERING INFORMATION

6–9 To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with check digit), indicate the quantity required, and address the order to the nearest Hewlett-Packard office (list of Sales/Service offices at the rear of this manual). The check digit will ensure accurate and timely processing of your order.

6–10 To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required, address the order to the nearest Hewlett-Packard office.

6–11 DIRECT MAIL ORDER SYSTEM (USA)

6–12 Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices – to provide these advantages, a check or money order must accompany each order.

6–13 Mail order forms and specific ordering information is available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6–1. Abbreviations for Replaceable Parts List

REFERENCE DESIGNATIONS

A . . . . . assembly
AT . . . attenuator; isolator; termination
B . . . . . fan; motor
BT . . . . . battery
C . . . . . capacitor
CP . . . . . coupler
CR . . . . . diode; diode thyristor; varactor
DC . . . directional coupler
DL . . . . . delay line
DS . . . . . annunciator; signaling device (audible or visual); lamp; LED
E . . . . . miscellaneous electrical part
F . . . . . fuse
FL . . . . . filter
H . . . . . hardware
HY . . . . . circulator
J . . . . electrical connector (stationary portion); jack
K . . . . . relay
L . . . . . coil; inductor
M . . . . . meter
MP . . . . . miscellaneous mechanical part
P . . . . electrical connector (movable portion); plug
Q . . . . . transistor: SCR; triode thyristor
R . . . . . resistor
RT . . . . . thermistor
S . . . . . switch
T . . . . . transformer
TB . . . . . terminal board
TC . . . . . thermocouple
TP . . . . . test point
U . . . . . integrated circuit; microcircuit
V . . . . . electron tube
VR . . . . voltage regulator; breakdown diode
W . . . . cable; transmission path; wire
X . . . . . socket
Y . . . . crystal unit (piezoelectric or quartz)
Z . . . . tuned cavity; tuned circuit

ABBREVIATIONS

A . . . . . ampere
ac . . . . alternating current
ACCESS . . . . . accessory
ADJ . . . . . adjustment
A/D . . . . analog-to-digital
AF . . . . audio frequency
AFC . . . . . automatic frequency control
AGC . . . . . automatic gain control
AL . . . . . aluminum
ALC . . . . automatic level control
AM . . . amplitude modulation
AMPL . . . . . amplifier
APC . . . . automatic phase control
ASSY . . . . . assembly
AUX . . . . . auxiliary
avg . . . . . average
AWG . . . . . American wire gauge
BAL . . . . . balance
BCD . . . . . binary coded decimal
BD . . . . . board
BE CU . . . . . beryllium copper
BFO . . . . beat frequency oscillator
BH . . . . . binder head
BKDN . . . . . breakdown
BP . . . . . bandpass
BPF . . . . . bandpass filter
BRS . . . . . brass
BWO . . . . backward-wave oscillator
CAL . . . . . calibrate
ccw . . . . counter-clockwise
CER . . . . . ceramic
CHAN . . . . . channel
cm . . . . . centimeter
CMO . . cabinet mount only
COAX . . . . . coaxial
COEF . . . . . coefficient
COM . . . . . common
COMP . . . . . composition
COMPL . . . . . complete
CONN . . . . . connector
CP . . . . . cadmium plate
CRT . . . cathode-ray tube
CTL . . . . complementary transistor logic
CW . . . . continuous wave
cw . . . . . clockwise
cm . . . . . centimeter
D/A . . . . . digital-to-analog
dB . . . . . decibel
dBm . . . . decibel referred to 1 mW
dc . . . . . direct current
deg . . degree (temperature interval or difference)
. . ^{o} . . . degree (plane angle)
^{o}C . . . . . degree Celsius (centigrade)
^{o}F . . . . degree Fahrenheit
^{o}K . . . . . degree Kelvin
DEPC . . deposited carbon
DET . . . . . detector
diam . . . . . diameter
DIA . . . diameter (used in parts list)
DIFF AMPL . . . differential amplifier
div . . . . . division
DPDT . . . . . double-pole, double-throw
DR . . . . . drive
DSB . . . . double sideband
DTL . . . . diode transistor logic
DVM . . . digital voltmeter
ECL . . . . emitter coupled logic
EMF . . electromotive force
EDP . . . . . electronic data processing
ELECT . . . . . electrolytic
ENCAP . . . . . encapsulated
EXT . . . . . external
F . . . . . farad
FET . . . . . field-effect transistor
F/F . . . . . flip-flop
FH . . . . . flatt head
FIL H . . . . . fillister head
FM . frequency modulation
FP . . . . . front panel
FREQ . . . . . frequency
FXD . . . . . fixed
g . . . . . gram
GE . . . . . germanium
GHz . . . . . gigahertz
GL . . . . . glass
GRD . . . . . ground(ed)
H . . . . . henry
h . . . . . hour
HET . . . . . heterodyne
HEX . . . . . hexagonal
HD . . . . . head
HDW . . . . . hardware
HF . . . . . high frequency
HG . . . . . mercury
HI . . . . . high
HP . . . . . Hewlett-Packard
HPF . . . . . high pass filter
HR . . . . . hour (used in parts list)
HV . . . . . high voltage
Hz . . . . . Hertz
IC . . . . . integrated circuit
ID . . . . . inside diameter
IF . . . . . intermediate frequency
IMPG . . . . . impregnated
in . . . . . inch
INCD . . . . . incandescent
INCL . . . . . include(s)
INP . . . . . input
INS . . . . . insulation
INT . . . . . internal
kg . . . . . kilogram
kHz . . . . . kilohertz
kΩ . . . . . kilohm
kV . . . . . kilovolt
lb . . . . . pound
LC . . . . . inductance-capacitance
LED . . light-emitting diode
LF . . . . . low frequency
LG . . . . . long
LH . . . . . left hand
LIM . . . . . limit
LIN . . . . linear taper (used in parts list)
lin . . . . . linear
LK WASH . . . lock washer
LO . . . low; local oscillator
LOG . . . logarithmic taper (used in parts list)
log . . . . . logarithm(ic)
LPF . . . . . low pass filter
LV . . . . . low voltage
m . . . . . meter (distance)
mA . . . . . milliampere
MAX . . . . . maximum
MΩ . . . . . megohm
MEG . . . . meg (10^{6}) (used in parts list)
MET FLM . . . . metal film
MET OX . . . metallic oxide
MF . . . medium frequency; microfarad (used in parts list)
MFR . . . . . manufacturer
mg . . . . . milligram
MHz . . . . . megahertz
mH . . . . . millihenry
mho . . . . . mho
MIN . . . . . minimum
min . . . . . minute (time)
. . . . . minute (plane angle)
MINAT . . . . . miniature
mm . . . . . millimeter
MOD . . . . . modulator
MOM . . . . . momentary
MOS . . . . . metal-oxide semiconductor
ms . . . . . millisecond
MTG . . . . . mounting
MTR . . . meter (indicating device)
mV . . . . . millivolt
mVac . . . . . millivolt, ac
mVdc . . . . . millivolt, dc
mVpk . . . . millivolt, peak
mVp-p . . . millivolt, peak-to-peak
mVrms . . . . millivolt, rms
mW . . . . . milliwatt
MUX . . . . . multiplex
MY . . . . . mylar
μA . . . . . microampere
μF . . . . . microfarad
μH . . . . . microhenry
μmho . . . . . micromho
μs . . . . . microsecond
μV . . . . . microvolt
μVac . . . . . microvolt, ac
μVdc . . . . . microvolt, dc
μVp-p . . . microvolt, peak-to-peak
μVrms . . . . microvolt, rms
μW . . . . . microwatt
nA . . . . . nanoampere
NC . . . . . no connection
N/C . . . . . normally closed
NE . . . . . neon
NEG . . . . . negative
nF . . . . . nanofarad
NI PL . . . . . nickel plate
N/O . . . . . normally open
NOM . . . . . nominal

NOTE

All abbreviations in the parts list will be in upper-case.

Table 6–1. Abbreviations for Replaceable Parts List (cont'd)

NORM . . . . . normal
NPN . . . negative-positive-negative
NPO . . . . negative-positive zero (zero temperature coefficient)
NRFR . . not recommended for field replacement
NSR . . . . . not separately replaceable
ns . . . . . nanosecond
nW . . . . . nanowatt
OBD . order by description
OD . . . . outside diameter
OH . . . . . oval head
OP AMPL . . . . operational amplifier
OPT . . . . . option
OSC . . . . . oscillator
OX . . . . . oxide
oz . . . . . ounce
Ω . . . . . ohm
P . . . . peak (used in parts list)
PAM . . . . pulse-amplitude modulation
PC . . . . . printed circuit
PCM . . pulse-code modulation; pulse-count modulation
PDM . . . . . pulse-duration modulation
pF . . . . . picofarad
PH BRZ . phosphor bronze
PHL . . . . . Phillips
PIN . . . . positive-intrinsic-negative
PIV . . . . . peak inverse voltage
pk . . . . . peak
PL . . . . . phase lock
PLO . . . . . phase lock oscillator
PM . . . . phase modulation
PNP . . . . positive-negative-positive
P/O . . . . . part of
POLY . . . . . polystyrene
PORC . . . . . porcelain
POS . . positive; position(s) (used in parts list)
POSN . . . . . position
POT . . . . . potentiometer
p-p . . . . . peak-to-peak
PP . . . peak-to-peak (used in parts list)
PPM . . . . . pulse-position modulation
PREAMPL . . . preamplifier
PRF. . . . . pulse-repetition frequency
PRR . . . . pulse repetition rate
ps . . . . . picosecond
PT . . . . . point
PTM . . . . . pulse-time modulation
PWM . . . . . pulse-width modulation
PWV . . . . . peak working voltage
RC . resistance-capacitance
RECT . . . . . rectifier
REF . . . . . reference
REG . . . . . regulated
REPL . . . . . replaceable
RF . . . . . radio frequency
RFI . . . . . radio frequency interference
RH . . . . round head; right hand
RLC . . . . . resistance-inductance-capacitance
RMO . . . rack mount only
rms . . . . root-mean-square
RND . . . . . round
ROM . . read-only memory
R&P . . . . . rack and panel
RWV . . . . reverse working voltage
S . . . scattering parameter
s . . . . . second (time)
" . . second (plane angle)
S-B . . . . slow-blow (fuse) (used in parts list)
SCR . . . silicon controlled rectifier; screw
SE . . . . . selenium
SECT . . . . . sections
SEMICON . . . . . semiconductor
SHF . . . . . superhigh frequency
SI . . . . . silicon
SIL . . . . . silver
SL . . . . . slide
SNR . . signal-to-noise ratio
SPDT . . . . . single-pole, double-throw
SPG . . . . . spring
SR . . . . . split ring
SPST . . . . . single-pole, single-throw
SSB . . . . single sideband
SST . . . . . stainless steel
STL . . . . . steel
SQ . . . . . square
SWR . . standing-wave ratio
SYNC . . . . . synchronize
T . . timed (slow-blow fuse)
TA . . . . . tantalum
TC . . . . . temperature compensating
TD . . . . . time delay
TERM . . . . . terminal
TFT . . thin-film transistor
TGL . . . . . toggle
THD . . . . . thread
THRU . . . . . through
TI . . . . . titanium
TOL . . . . . tolerance
TRIM . . . . . trimmer
TSTR . . . . . transistor
TTL . . transistor-transistor logic
TV . . . . . television
TVI television interference
TWT . . traveling wave tube
U . . . . micro (10^6) (used in parts list)
UF . . . microfarad (used in parts list)
UHF . . ultrahigh frequency
UNREG . . . . unregulated
V . . . . . volt
VA . . . . . voltampere
Vac . . . . . volts, ac
VAR . . . . . variable
VCO . . . voltage-controlled oscillator
Vdc . . . . . volts, dc
VDCW . . volts, dc, working (used in parts list)
V(F) . . . . . volts, filtered
VFO . . variable-frequency oscillator
VHF . . . . . very-high frequency
Vpk . . . . . volts, peak
Vp-p . . volts, peak-to-peak
Vrms . . . . . volts, rms
VSWR . . . voltage standing wave ratio
VTO . . . . . voltage-tuned oscillator
VTVM . . . . Vacuum-tube voltmeter
V(X) . . . . . volts, switched
W . . . . . watt
W . . . . . with
WIV . . . . working inverse voltage
WW . . . . . wirewound
W/O . . . . . without
YIG . . yttrium-iron-garnet
Z_o . . . . . characteristic impedance

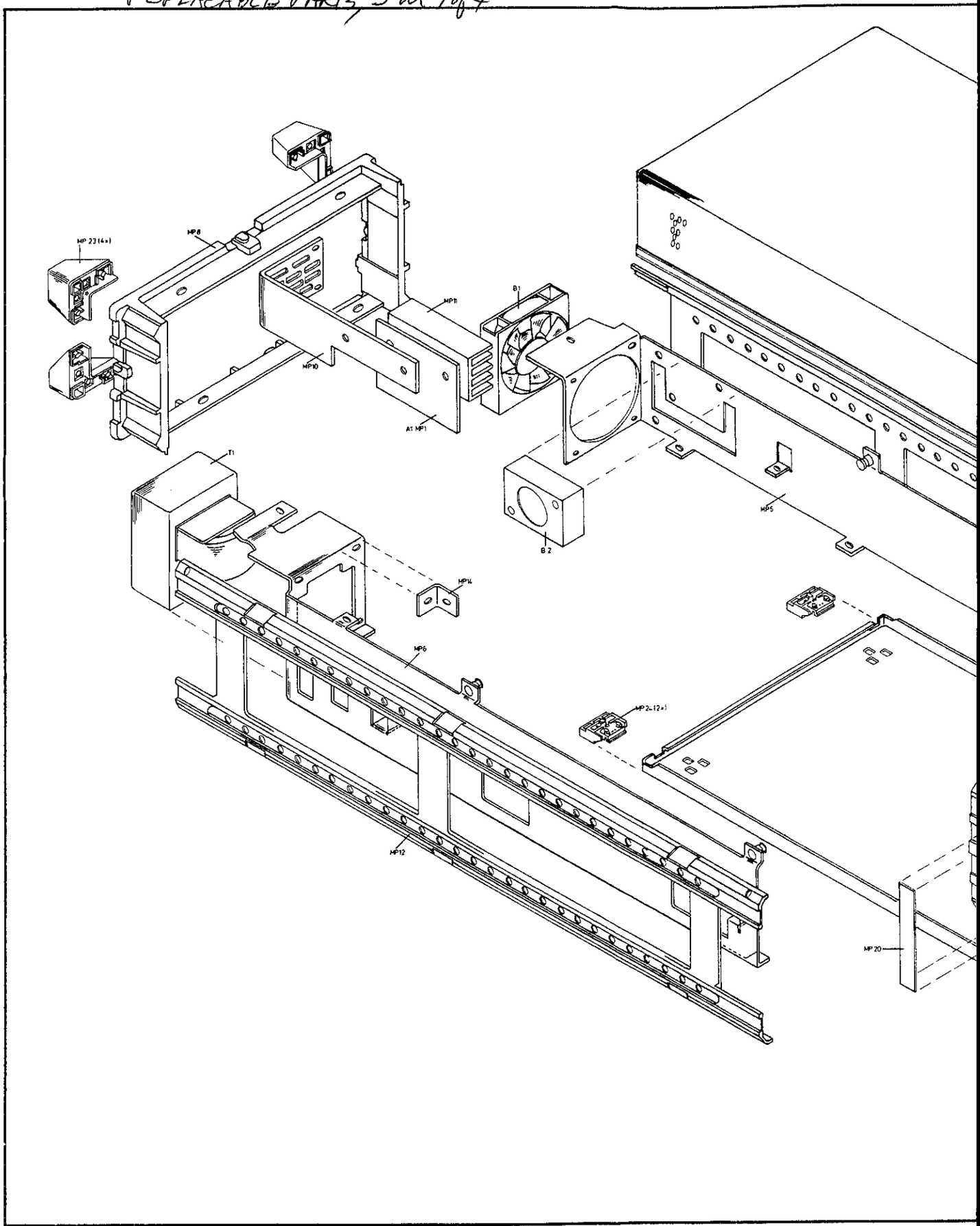
MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

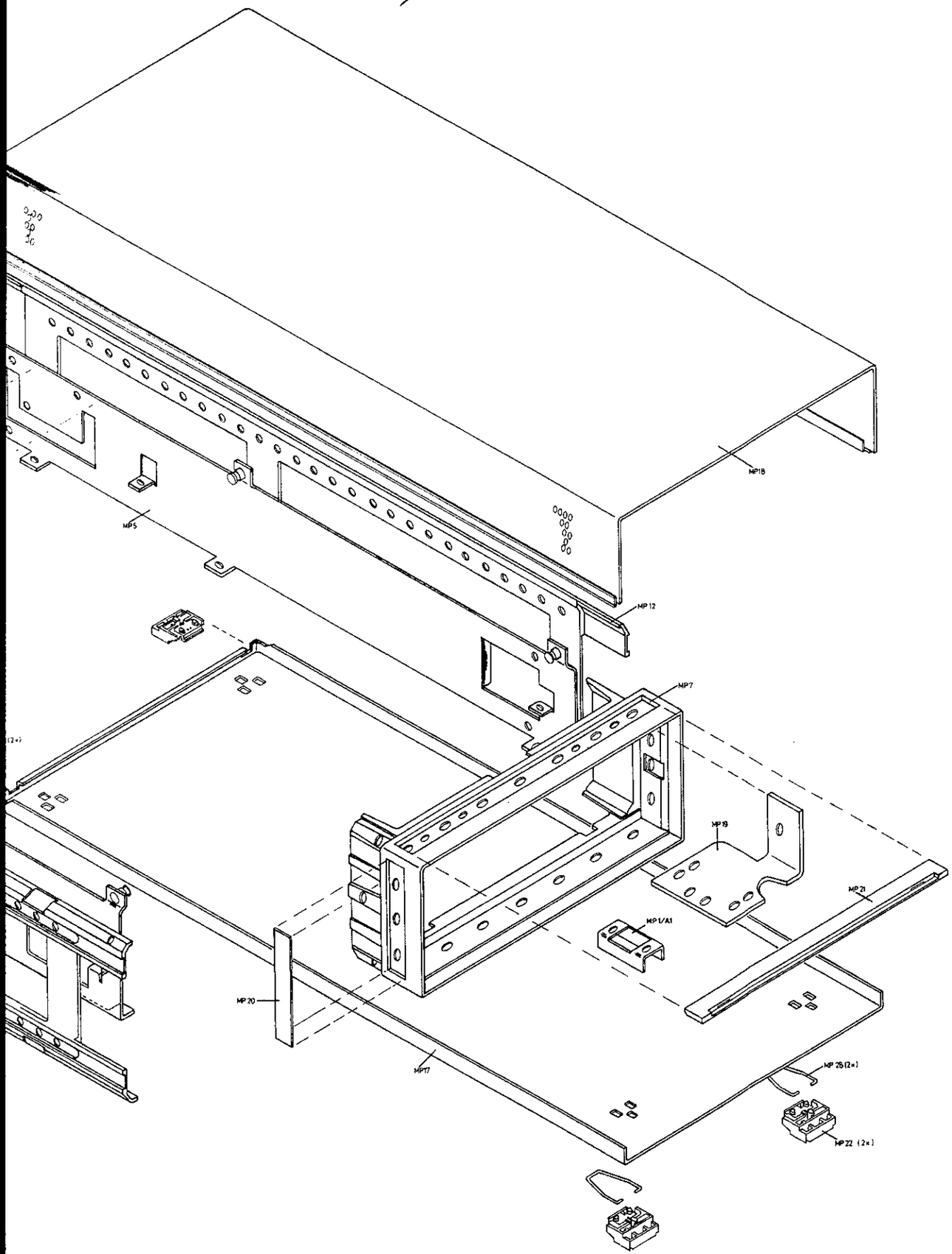
NOTE

All abbreviations in the parts list will be in upper-case.

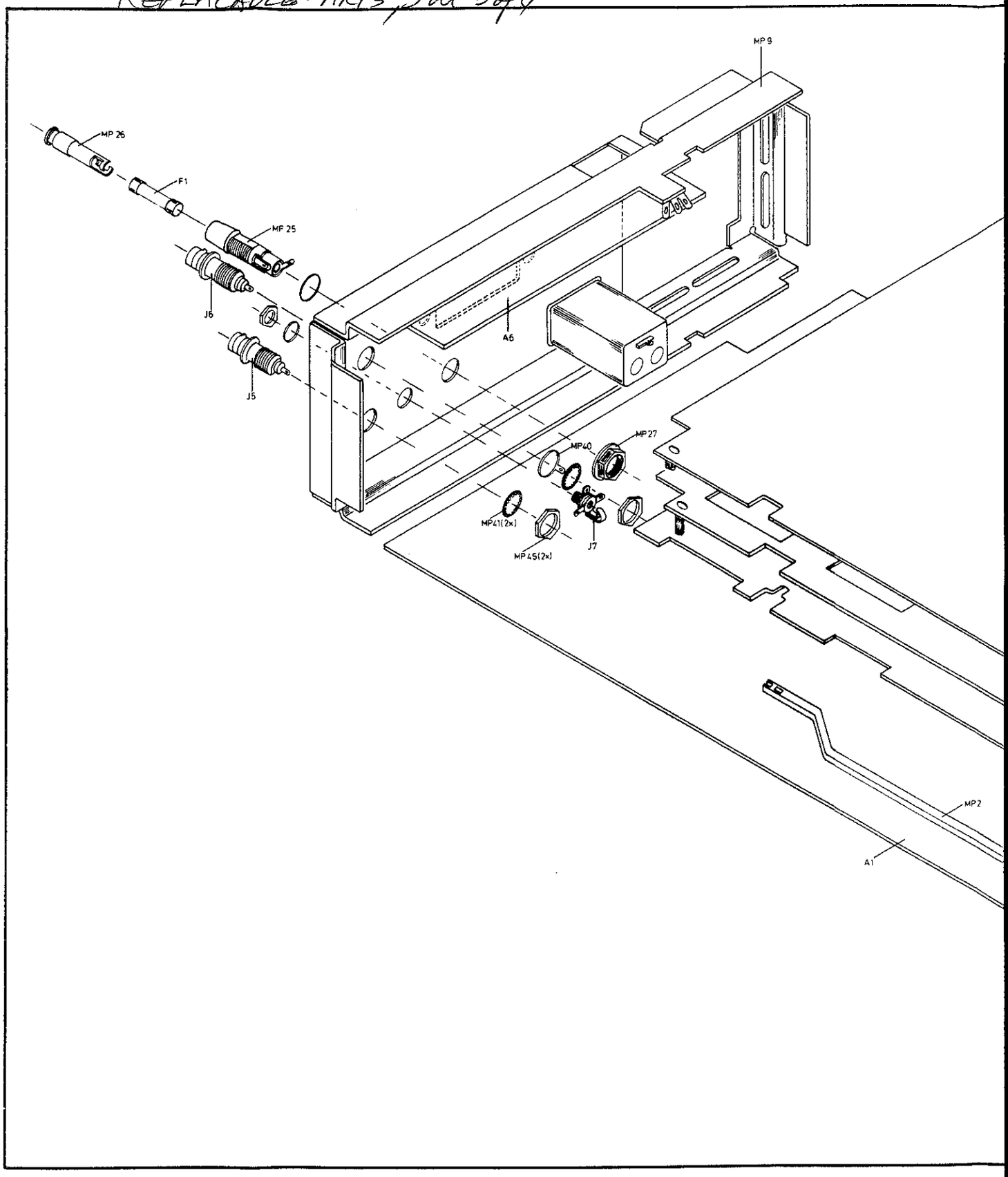
REPLACABLE PARTS, SHT 1 OF 4



REPLACABLE PARTS, SUA 28/4



Replacable Parts, Set 3044



REPLACABLE PARTS Sht 40/4

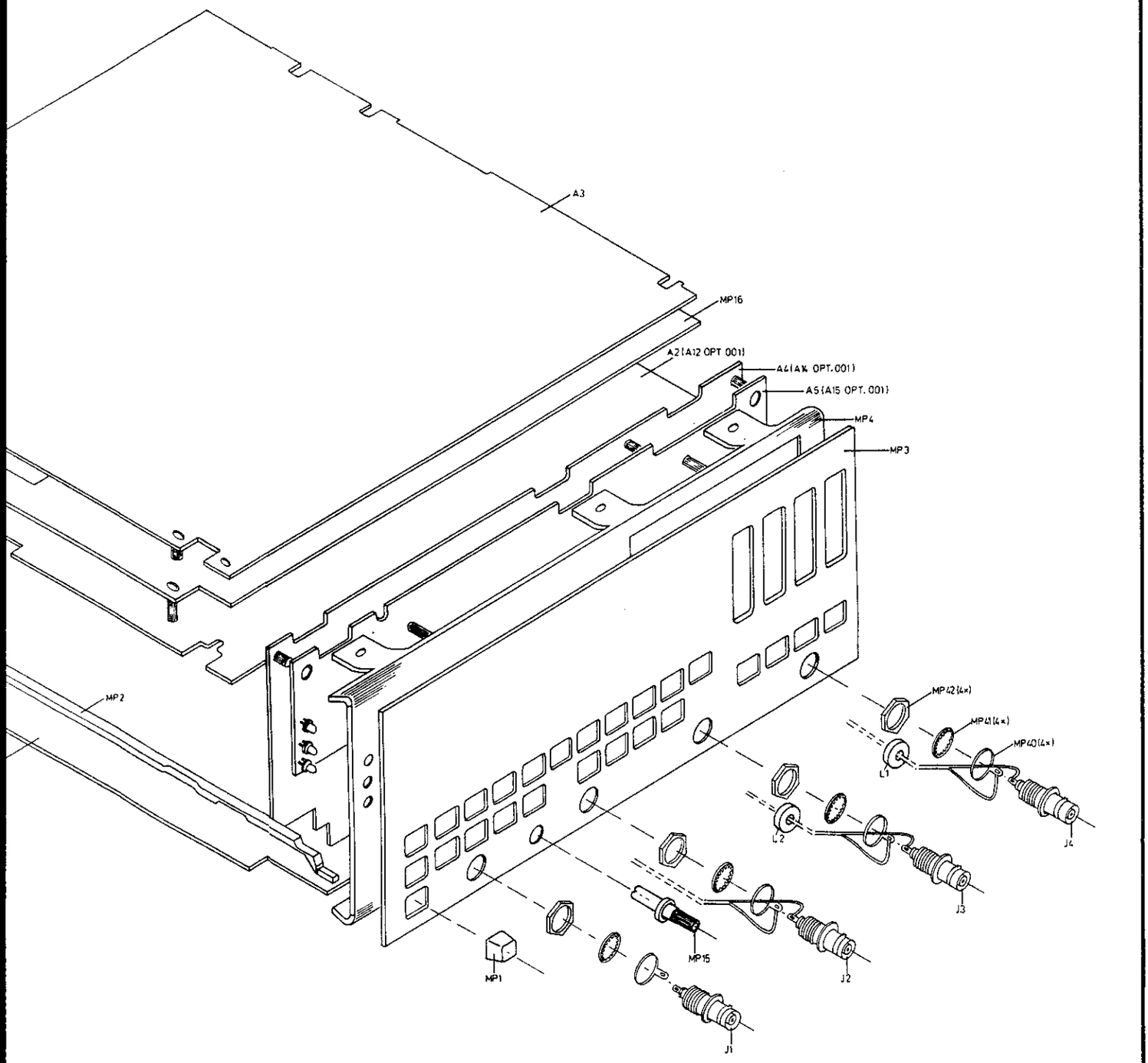


Table 6-3. Replaceable Parts

REFERENCE DESIGNATOR	CD	H-P PART NUMBER	DESCRIPTION	
FRAME				
A1		08116-66511	BD AY-MAIN	
A2	5	08116-66502	BD AY-CONTROL	
A3	7	08116-66503	BD AY-MICROPRCR	
A4	8	08116-66504	BD AY-KEY	
A5	9	08116-66505	BD AY DISPLAY	
A6		08116-66506	BD AY HPIB	
B1	3	3160-0266	FAN TUBE AXIAL	
B2	8	3160-0310	MODULE MOTOR CON	
F1	8	2110-0043	FUSE 1.5 FER	
F1	2	2110-0063	FUSE .75 FER	
FL1		9135-0035	FILTER, LINE	
J1	1	1250-0083	CONN BNC BLKHD	
J2	1	1250-0083	CONN BNC BLKHD	
J3	1	1250-0083	CONN BNC BLKHD	
J4	1	1250-0083	CONN BNC BLKHD	
L1	5	9170-0013	CORE FERRA .375	
L2	5	9170-0013	CORE FERRA .375	
MP1	5	5041-0531	KEY	
MP2	1	5040-9317	SHAFT-POWER-SW	
MP3	7	4040-1972	PANEL FRONT	
MP4	5	08116-00202	PANEL-SUB	
MP5		08112-04156	BRACKET FAN	
MP6		08112-04153	BRACKET-XFMR	
MP7	8	5020-8813	FRAME FRONT	
MP8		08116-21103	FRM REAR(MODIFY)	
MP9		5061-2116	PANEL REAR	
MP10		08112-21101	HEATSINK-REAR	
MP11		08112-21105	HEATSINK-POWER	
MP12	0	5020-8831	SIDE STRUT 17IN	
MP13	0	5020-8831	SIDE STRUT 17IN	
MP14		08112-04154	KEEPER	
MP15	6	5040-1136	KNOB LONG	
MP16		08112-00601	SHIELD	
MP17	4	08112-04158	COVER-BOTTOM	
MP18		08116-04101	COVER TOP 31/2HM	
MP19		08116-21102	HEATSINK OUTPUT	
MP20	7	5001-0438	TRIM STRIP	
MP21	0	5040-7203	TRIM STRIP	
MP22	8	5040-7201	FOOT	
MP23	2	5040-7221	FOOT REAR	
MP24	3	5040-7222	RR FEET NON-SKID	
MP25	8	2110-0564	FUSEHOLDER BODY	
MP26	9	2110-0565	FUSEHOLD CAP/UL	
MP27	3	2110-0569	NUT HEX	
MP28	5	1460-1345	TILT STAND	
MP30		1400-0290	BRACKET 90°	
MP31		1400-0024	CABLE CLAMP	
MP32	4	0380-0644	MTG STUD	
MP33		08116-40601	COVER-PLASTIC	
MP40	5	0360-1190	TERM-LUG SLDR	
MP41	3	2190-0016	WASH-LOCK INT3/8	
MP42	8	2950-0043	NUT-HEX .375-32	
T1		08112-61101	XFMR-PWR	

Table 6-3. Replaceable Parts

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A1			08116-66511	BD AY-MAIN
A1	C1		0180-3159	C-F ELCO 10000UF
A1	C2		0180-3158	C-F ELCO 6800UF
A1	C3		0180-3160	C-F ELCO 2200UF
A1	C4		0180-3160	C-F ELCO 2200UF
A1	C5		0180-3152	C-FXD 2200UF 40V
A1	C6	6	0180-3008	C-F 470UF 10%
A1	C7	7	0180-2984	C-F 47UF 20% 50V
A1	C8	7	0180-2984	C-F 47UF 20% 50V
A1	C9	7	0180-2984	C-F 47UF 20% 50V
A1	C10	7	0180-2984	C-F 47UF 20% 50V
A1	C11	9	0180-2962	C-F 220UF 10V
A1	C12	9	0180-2962	C-F 220UF 10V
A1	C13	9	0180-2962	C-F 220UF 10V
A1	C14	9	0160-2055	C-F .01UF CER
A1	C15	9	0160-2055	C-F .01UF CER
A1	C16	9	0160-2055	C-F .01UF CER
A1	C17	9	0160-2055	C-F .01UF CER
A1	C18	1	0160-3097	C-F .47UF CER
A1	C19	1	0160-3097	C-F .47UF CER
A1	C100	5	0160-0576	C-F .1UF 20% CER
A1	C101	5	0160-0576	C-F .1UF 20% CER
A1	C102	9	0160-0174	C-F .47UF 25VCER
A1	C103	5	0160-0576	C-F .1UF 20% CER
A1	C104	0	0160-0571	C-F 470PF20% CER
A1	C105	5	0160-0174	C-F .47UF 25V
A1	C106	5	0160-0576	C-F .1UF 20% CER
A1	C107	7	0180-0229	C-F 33UF 10V
A1	C108	5	0160-0576	C-F .1UF 20% CER
A1	C110	9	0160-0174	C-F .47UF 25VCER
A1	C112	1	0180-2249	C-F 47UF ±10% 20V
A1	C113	1	0180-2249	C-F 47UF ±10% 20V
A1	C114	7	0180-0229	C-F 33UF 10V
A1	C115	7	0180-0229	C-F 33UF 10V
A1	C151	1	0160-3873	C-F 4.7PF 200V
A1	C152	5	0160-0576	C-F .1UF 20% CER
A1	C153	5	0160-0576	C-F .1UF 20% CER
A1	C154	4	0160-4387	C-F 47PF 200V
A1	C200	6	0160-3878	C-F .001UF 100V
A1	C201	6	0160-3878	C-F .001UF 100V
A1	C202	7	0160-3879	C-F .01UF 100V
A1	C204	2	0121-0046	C-VAR 9-35PF
A1	C205	1	0160-4318	C-F 330PF 1%
A1	C206	9	0160-2675	C-F 3900PF 300V
A1	C207	4	0160-5426	C-F .039UF 1%63V
A1	C208	2	0160-5424	C-F .39UF 1% 40V
A1	C209	3	0160-3726	C-F 1UF 10% 100V
A1	C210	9	0160-3839	C-F 2.2UF 10%
A1	C211	1	0160-0572	C-F 2200PF CER
A1	C212	5	0160-0576	C-F .1UF 20% CER
A1	C213	9	0160-0174	C-F .47UF 25VCER
A1	C214	5	0160-0576	C-F .1UF 20% CER
A1	C215	5	0160-0576	C-F .1UF 20% CER
A1	C216	0	0160-4383	C-F 6.8PF 200V
A1	C217	2	0160-3874	C-F 10PF 200V
A1	C220	5	0160-0576	C-F .1UF 20% CER
A1	C221	5	0160-3878	C-F .001UF 100V
A1	C222	5	0160-3878	C-F .001UF 100V
A1	C223	0	0160-4383	C-F 6.8PF 200V
A1	C224	5	0160-0576	C-F .1UF 20% CER
A1	C225	6	0160-3878	C-F .001UF 100V
A1	C226	9	0160-0174	C-F .47UF 25VCER
A1	C227	9	0160-0174	C-F .47UF 25VCER
A1	C230	3	0160-4386	C-F 33PF 5% 200V
A1	C231	5	0160-0576	C-F .1UF 20% CER
A1	C235		0160-4494	C-F 39 PF 200V 10%
A1	C240	9	0160-0174	C-F .47UF 25VCER
A1	C241	5	0160-0576	C-F .1UF 20% CER
A1	C260	5	0160-0576	C-F .1UF 20% CER
A1	C261	5	0160-0576	C-F .1UF 20% CER
A1	C262	7	0160-3879	C-F .01UF 100V
A1	C263	5	0160-0576	C-F .1UF 20% CER
A1	C264 #		0160-4040	C-F 1nF 100V 5%
A1	C300	2	0160-3874	C-F 10PF 200V
A1	C301	5	0160-0576	C-F .1UF 20% CER
A1	C302	5	0160-0576	C-F .1UF 20% CER
A1	C303	7	0160-3879	C-F .01UF 100V
A1	C304	6	0160-3878	C-F .001UF 100V
A1	C305	5	0160-0576	C-F .1UF 20% CER
A1	C306	7	0160-3879	C-F .01UF 100V
A1	C400	7	0160-3879	C-F .01UF 100V
A1	C401	1	0160-0572	C-F 2200PF CER
A1	C402	9	0160-0174	C-F .47UF 25VCER
A1	C403	5	0160-0576	C-F .1UF 20% CER
A1	C404	9	0160-0174	C-F .47UF 25VCER
A1	C405	5	0160-0576	C-F .1UF 20% CER
A1	C406	7	0160-4512	C-F 120PF 5%
A1	C408		0160-0576	C-F .1UF 20%
A1	C501	3	0160-0574	C-F .022UF CER
A1	C502	7	0160-4547	C-F 150PF 200V 5%
A1	C503	9	0160-0174	C-F .47UF 25VCER
A1	C504	9	0160-0174	C-F .47UF 25VCER
A1	C505	7	0160-3879	C-F .01UF 100V
A1	C506	1	0160-0572	C-F 2200PF CER
A1	C507	1	0160-3097	C-F .47UF CER
A1	C508	1	0160-3097	C-F .47UF CER
A1	C509	2	0160-0573	C-F 4700PF 20%
A1	C510	2	0160-0573	C-F 4700PF 20%
A1	C511	7	0160-3879	C-F .01UF 100V
A1	C512	5	0160-0576	C-F .1UF 20% CER
A1	C513	5	0160-0576	C-F .1UF 20% CER
A1	C514	5	0160-0576	C-F .1UF 20% CER
A1	C515	5	0160-0576	C-F .1UF 20% CER
A1	C516	5	0160-0576	C-F .1UF 20% CER
A1	C517	5	0160-0576	C-F .1UF 20% CER
A1	C518	5	0160-0576	C-F .1UF 20% CER
A1	C519	1	0160-3097	C-F .47UF CER
A1	C520	1	0160-3097	C-F .47UF CER
A1	C521	1	0160-3097	C-F .47UF CER
A1	C522	1	0160-3097	C-F .47UF CER
A1	C523	5	0180-0582	C-F 270UF 40V
A1	C524	5	0180-0582	C-F 270UF 40V
A1	C525 #	0	0160-5738	C-F 6.8PF
A1	C526	5	0160-0576	C-F .1UF 20% CER
A1	C527 #	4	0160-4350	C-F 68PF 200V
A1	C528	7	0160-4380	C-F 1PF 200V
A1	C529	0	0121-0466	C-VAR 1-3PF 100V
A1	C530 #	7	0160-4380	C-F 1PF 200V
A1	C531	0	0160-3568	C-F 2.7PF 200V
A1	C533	5	0160-0576	C-F .1UF 20% CER
A1	C534	5	0160-0576	C-F .1UF 20% CER
A1	C535	5	0160-0576	C-F .1UF 20% CER
A1	C536	5	0160-0576	C-F .1UF 20% CER

Table 6-3. Replaceable Parts

REFERENCE DESIGNATOR		CD	H-P PART NUMBER	DESCRIPTION
A1	C537	5	0160-0576	C-F .1UF 20% CER
A1	C538 *	8	0160-4381	C-F 1,5PF 200V
A1	C539	6	0160-4389	C-F 100PF
A1	C541		0160-3879	C-F .01UF 100V
A1	C550	5	0160-0576	C-F .1UF 20% CER
A1	CR1	3	1901-0638	DIO AY-SI 100V
A1	CR2	7	1906-0096	DIO-FULL WAVE BR
A1	CR3	7	1906-0096	DIO-FULL WAVE BR
A1	CR4	1	1901-1098	DIO-SWIT.1N4150
A1	CR5	1	1901-1098	DIO-SWIT.1N4150
A1	CR6	1	1901-1098	DIO-SWIT.1N4150
A1	CR7	1	1901-1098	DIO-SWIT.1N4150
A1	CR8	1	1901-1098	DIO-SWIT.1N4150
A1	CR9	1	1901-1098	DIO-SWIT.1N4150
A1	CR101	3	1901-0539	DIO SCHOTTKY
A1	CR151	1	1901-1098	DIO-SWIT.1N4150
A1	CR152	1	1901-1098	DIO-SWIT.1N4150
A1	CR153	3	1901-0539	DIO SCHOTTKY
A1	CR154	3	1901-0539	DIO SCHOTTKY
A1	CR201	1	1901-1098	DIO-SWIT.1N4150
A1	CR202	1	1901-1098	DIO-SWIT.1N4150
A1	CR203	3	1901-0539	DIO SCHOTTKY
A1	CR204	3	1901-0539	DIO SCHOTTKY
A1	CR300	1	1901-1098	DIO-SWIT.1N4150
A1	CR301	1	1901-1098	DIO-SWIT.1N4150
A1	CR302	1	1901-1098	DIO-SWIT.1N4150
A1	CR501	7	1901-0179	DIO SI 15V .75NS
A1	CR502	7	1901-0179	DIO SI 15V .75NS
A1	CR503	7	1901-0179	DIO SI 15V .75NS
A1	CR504	7	1901-0179	DIO SI 15V .75NS
A1	CR505	7	1901-0050	DIO SWIT. 80V 200
A1	CR506	7	1901-0050	DIO SWIT. 80V 200
A1	CR507	1	1901-1098	DIO-SWIT.1N4150
A1	CR508	1	1901-1098	DIO-SWIT.1N4150
A1	CR509	1	1901-1098	DIO-SWIT.1N4150
A1	CR510	1	1901-1098	DIO-SWIT.1N4150
A1	CR511	1	1901-1098	DIO-SWIT.1N4150
A1	CR512	1	1901-1098	DIO-SWIT.1N4150
A1	CR513		1901-0732	DIO-PWR 1KV 1A
A1	CR514		1901-0732	DIO-PWR 1KV 1A
A1	F1	6	2110-0297	FUSE 5A 125V
A1	F2	6	2110-0297	FUSE .5A 125V
A1	J1		1251-5184	CONN 7 PIN
A1	J2	2	1251-3119	CONN 20PIN RIBN
A1	J3	8	1251-3305	CONN-4-PIN
A1	K201	5	0490-1137	RELAY-REED 1A
A1	K202	5	0490-1137	RELAY-REED 1A
A1	K501	5	0490-1137	RELAY-REED 1A
A1	K502	5	0490-1137	RELAY-REED 1A
A1	K503	5	0490-1137	RELAY-REED 1A
A1	K504	5	0490-1137	RELAY-REED 1A
A1	K505	5	0490-1137	RELAY-REED 1A
A1	K506	5	0490-1137	RELAY-REED 1A
A1	L100	0	9170-0894	CORE MAGNETIC
A1	L101	0	9170-0894	CORE MAGNETIC
A1	L102	0	9170-0894	CORE MAGNETIC
A1	L103	0	9170-0894	CORE MAGNETIC
A1	L260	3	9100-2254	COIL-CHOKE .39UH
A1	L261	0	9170-0894	CORE MAGNETIC
A1	L300	0	9170-0894	CORE MAGNETIC
A1	L301	0	9170-0894	CORE MAGNETIC
A1	L500	0	9170-0894	CORE MAGNETIC
A1	L501	0	9170-0894	CORE MAGNETIC
A1	L502	0	9170-0894	CORE MAGNETIC
A1	L503	0	9170-0894	CORE MAGNETIC
A1	L504	0	9170-0894	CORE MAGNETIC
A1	L505	0	9170-0894	CORE MAGNETIC
A1	MP1		08112-21104	HEATSINK
A1	MP2		08112-05401	PLATE INSULATOR
A1	MP3		08112-05401	PLATE INSULATOR
A1	MP4	6	00180-09104	CLIP-GROUND
A1	MP100		08112-04155	BRACKET-POTI
A1	MP200	0	1205-0235	HEAT SINK
A1	MP500		08116-04151	XSTR HEATSINK
A1	MP501	3	1205-0329	HT-SINK SGL
A1	Q1	5	1854-0368	XSTR 2N5191
A1	Q2	1	1854-0637	XSTR SI 2219A
A1	Q3	5	1854-0368	XSTR 2N5191
A1	Q4	1	1854-0637	XSTR SI 2219A
A1	Q5	9	1853-0314	XSTR 2N2905A PNP
A1	Q6	6	1853-0212	XSTR 2N5194 SI
A1	Q100	1	1854-0215	XSTR SI 2N3904
A1	Q101	2	1853-0036	XSTR SI 2N3906
A1	Q102	1	1854-0215	XSTR SI 2N3904
A1	Q200	2	1853-0036	XSTR SI 2N3906
A1	Q201	2	1853-0036	XSTR SI 2N3906
A1	Q202	2	1853-0036	XSTR SI 2N3906
A1	Q203	7	1853-0354	XSTR MPS H81
A1	Q204	7	1853-0354	XSTR MPS H81
A1	Q205	1	1854-0215	XSTR SI 2N3904
A1	Q206	1	1854-0215	XSTR SI 2N3904
A1	Q207	1	1854-0215	XSTR SI 2N3904
A1	Q208	1	1854-0215	XSTR SI 2N3904
A1	Q209	1	1854-0215	XSTR SI 2N3904
A1	Q210	1	1854-0392	XSTR SI 2N3088
A1	Q211	2	1853-0036	XSTR SI 2N3906
A1	Q212	2	1853-0036	XSTR SI 2N3906
A1	Q213	2	1853-0036	XSTR SI 2N3906
A1	Q214	2	1853-0036	XSTR SI 2N3906
A1	Q215	2	1853-0036	XSTR SI 2N3906
A1	Q220	1	1854-0215	XSTR SI 2N3904
A1	Q260	2	1854-0795	XSTR MPS-H10
A1	Q261	2	1854-0795	XSTR MPS-H10
A1	Q262	2	1853-0218	XSTR SI PNP
A1	Q263	2	1853-0218	XSTR SI PNP
A1	Q300	1	1854-0215	XSTR SI 2N3904
A1	Q301	1	1854-0215	XSTR SI 2N3904
A1	Q302	1	1854-0215	XSTR SI 2N3904
A1	Q303	1	1854-0215	XSTR SI 2N3904
A1	Q401	9	1853-0075	XSTR SI PNP
A1	Q402	2	1853-0218	XSTR SI PNP
A1	Q403	2	1853-0036	XSTR SI 2N3906
A1	Q430	2	1853-0036	XSTR SI 2N3906
A1	Q431	5	1854-0392	XSTR ST 2N 5088
A1	Q432	2	1853-0086	XSTR SI 2N5087
A1	Q433	1	1854-0215	XSTR SI 2N3904
A1	Q501	9	1854-0809	TRANS.2N 2369A
A1	Q502	9	1853-0405	XSTR SI 2N4209
A1	Q503	9	1854-0354	XSTR SI NPN
A1	Q504	9	1853-0357	XSTR SI PNP
A1	Q505	7	1853-0312	XSTR PNP 2N5160
A1	Q506	9	1854-0784	XSTR NPN 2N3866A
A1	Q507	7	1854-0477	XSTR NPN 2N2222A
A1	Q508	9	1854-0784	XSTR NPN 2N3866A
A1	Q509	7	1853-0312	XSTR PNP 2N5160

Table 6-3. Replaceable Parts

REFERENCE DESIGNATOR		CD	H-P PART NUMBER	DESCRIPTION
A1	Q510	9	1854-0637	XSTR 2N2219A
A1	Q511	7	1853-0314	XSTR 2N2905A
A1	Q512	9	1853-0637	XSTR 2N2219A
A1	Q513	7	1853-0314	XSTR 2N2905A
A1	Q514	1	1854-0215	XSTR SI 2N3904
A1	Q515	2	1853-0036	XSTR SI 2N3906
A1	Q590	1	1854-0215	XSTR SI 2N3904
A1	Q591	1	1854-0215	XSTR SI 2N3904
A1	R1	8	0698-3615	R-F 47 5%
A1	R2	7	0812-0111	R-F .05 3% 3W
A1	R3	0	0698-4508	R-F 78.7K1%
A1	R4	0	0698-0085	R-F 2.61K1%
A1	R5	6	0812-0045	R-F .15 5% 3W
A1	R6	1	0757-0460	R-F 61.9K 1%
A1	R7	0	0698-0085	R-F 2.61K1%
A1	R8	0	0698-0085	R-F 2.61K1%
A1	R9	5	0757-0464	R-F 90.9K1%
A1	R10	7	0812-0111	R-F .05 3% 3W
A1	R11	3	0698-4460	R-F 649 1% .125W
A1	R12	7	2100-3211	R-TRMR 1K 10%
A1	R13	0	0757-0401	R-F 100 1% .125W
A1	R14	8	0698-6320	R-F 5K.1% .125W
A1	R15	8	0698-8863	R-F 5.2K .1%
A1	R16	9	0698-3442	R-F 237 1% .125W
A1	R17	9	0757-0434	R-F 3.65K1%
A1	R18	7	2100-3211	R-TRMR 1K 10%
A1	R19	7	2100-3211	R-TRMR 1K 10
A1	R20	9	0757-0434	R-F 3.65K1%
A1	R21	9	0698-3442	R-F 237 1% .125W
A1	R22		0698-4421	R-F 249 1% .125W
A1	R23	2	0698-4435	R-F 2.49K1%
A1	R24	5	2100-0554	R-V 500 10% .5W
A1	R25	5	2100-0554	R-V 500 10% .5W
A1	R26	2	0698-4435	R-F 2.49K1%
A1	R27		0698-4421	R-F 249 1% .125W
A1	R28	3	1810-0037	R-NETWORK DIP
A1	R100	8	0698-3540	R-F 15.4K1%
A1	R101	6	0757-0449	R-F 20K1% .125W
A1	R102	6	0757-0449	R-F 20K1% .125W
A1	R103	6	0757-0449	R-F 20K1% .125W
A1	R104	0	0698-3154	R-F 4.22K 1%
A1	R105	1	0757-0410	R-F 301 1% .125W
A1	R106		2100-3976	R-VAR 10K 20%
A1	R107	7	0698-3359	R-F 12.7K1%
A1	R108	6	0698-4497	R-F 48.7K 1%
A1	R109	2	0698-4435	R-F 2.49K1%
A1	R110	0	0757-0401	R-F 100 1% .125W
A1	R111	8	0698-3178	R-F 487 1% .125W
A1	R112	5	1810-0203	R-NETWORK 7X470
A1	R113	8	0698-3152	R-F 3.48K 1%
A1	R114	8	0698-3178	R-F 487 1% .125W
A1	R115	0	0757-0401	R-F 100 1% .125W
A1	R116	8	1810-0280	R-NETWORK 9X10K
A1	R117	3	1810-0243	R-NETWORK 8X6.8K
A1	R118	5	1810-0279	R-NETWORK 4.7K
A1	R119	3	0757-0280	R-F 1K1% .125W F
A1	R120	3	0757-0420	R-F 750 1% .125W
A1	R121	4	0757-0439	R-F 6.81K1%
A1	R122	1	0757-0410	R-F 301 1% .125W
A1	R123	4	0698-3444	R-F 316 .125W 1%
A1	R124	1	0698-7214	R-F 121 1% .05W
A1	R125	8	0698-3178	R-F 487 1% .125W
A1	R130		2100-3212	R-VAR 200 10%
A1	R150	5	1810-0279	R-NETWORK 4.7K
A1	R151	9	0757-0442	R-F 10K1% .125W
A1	R152	9	0757-0442	R-F 10K1% .125W
A1	R153	9	0757-0442	R-F 10K1% .125W
A1	R154	7	0757-0200	R-F 5.62K1%
A1	R155	8	0698-4514	R-F 105K1% .125W
A1	R157	1	0698-3155	R-F 4.64K 1% .125
A1	R158	5	1810-0279	R-NETWORK 4.7K
A1	R200	7	0698-4422	R-F 1.27K1%
A1	R201	7	0698-4422	R-F 1.27K1%
A1	R202	1	1810-0332	R-NETWORK 680
A1	R204	5	0698-7226	R-F 383 1% .05W
A1	R205	9	0698-7220	R-F 215 1% .05W
A1	R206	3	0698-7216	R-F 147 1% .05W
A1	R207	9	1810-0281	R-NETWORK SIP
A1	R208	1	1810-0332	R-NETWORK 680
A1	R209	8	1810-0206	R-NETWORK 7X10K
A1	R210	4	0698-8827	R-F 1M 1% .125W
A1	R211	4	0698-8827	R-F 1M 1% .125W
A1	R213	2	0698-7215	R-F 133 1% .05W
A1	R215	0	0698-3152	R-F 3.48K 1%
A1	R216	9	0698-4367	R-F 20.5 1%
A1	R217	8	0698-3433	R-F 28.7 1%
A1	R219	7	0757-0440	R-F 7.5K 1% 125W
A1	R220 *	7	0757-0281	R-F 2.74K 1%
A1	R221	6	2100-3252	RES-TRMR 5K 10%
A1	R222	7	0757-0440	R-F 7.5K 1% 125W
A1	R223 *	7	0757-0281	R-F 2.74K 1%
A1	R224	6	2100-3252	RES-TRMR 5K 10%
A1	R225	4	0698-3439	RES 178 1% .125W
A1	R226	8	0698-4429	R-F 1.87K 1%
A1	R227	5	2100-0554	R-V 500 10% 5W
A1	R228	4	0698-8819	R-F 3.83 1% 1/8W
A1	R229	1	0757-0410	R-F 301 1% .125W
A1	R230	3	0757-0280	R-F 1K1% .125W F
A1	R231	3	0757-0420	R-F 750 1% 125W
A1	R232	2	0698-6324	R-F 187 1% 125W
A1	R233	1	0757-0410	R-F 301 1% 125W
A1	R234	1	0757-0410	R-F 301 1% 125W
A1	R235	4	0698-4073	R-F 1M10% .125W
A1	R236	4	0698-4073	R-F 1M10% .125W
A1	R237	4	0698-4073	R-F 1M10% .125W
A1	R238	4	0698-4073	R-F 1M10% .125W
A1	R239	4	0698-4073	R-F 1M10% .125W
A1	R240	1	0698-3155	R-F 4.64K 1% .125
A1	R241	3	0757-0280	R-F 1K1% 125W F
A1	R242	2	0698-4469	R-F 1.15K1%
A1	R243	5	0757-0274	R-F 1.21K1%
A1	R244	8	0698-0083	R-F 1.96K1%
A1	R245	4	0757-0405	R-F 162 1% .125W
A1	R246	3	0698-3446	R-F 383 1% .125W
A1	R260	8	0698-3178	R-F 487 1% .125W
A1	R261	9	0698-3442	R-F 237 1% .125W
A1	R262	0	0757-0419	R-F 681 1% .125W
A1	R263		0698-4421	R-F 249 1% .125W
A1	R264	6	0757-0499	R-F 27.4 1% .25W
A1	R265	7	0757-1000	R-F 51.1 1% .5W
A1	R266	3	0757-0389	R-F 33.2 1%
A1	R267	6	0757-0803	R-F 182 1% .5W
A1	R268	6	0757-0803	R-F 182 1% .5W
A1	R269	9	0757-1094	R-F 1.47K1%
A1	R270	3	0698-4460	R-F 649 1% .125W

Table 6-3. Replaceable Parts

REFERENCE DESIGNATOR		CD	H-P PART NUMBER	DESCRIPTION
A1	R271	5	0698-4404	R-F 105 1% .125W
A1	R272	8	0698-3433	R-F 28.7 1%
A1	R300	0	0757-0401	R-F 100 1% .125W
A1	R301	8	0698-3178	R-F 487 1% .125W
A1	R302	8	0698-3178	R-F 487 1% .125W
A1	R303	9	0698-3228	R-F 49.9K1%
A1	R304	6	2100-3210	R-VAR 10K 10% 5W
A1	R305	Q	0757-0401	R-F 100 1% .125W
A1	R306	1	0757-0460	R-F 61 9K 1%
A1	R307	3	0698-4486	R-F 24.9K1%
A1	R308	3	0757-0280	R-F 1K1% .125W F
A1	R309*	7	0757-0401	R-F 100 .125W 1%
A1	R310*	6	0757-0283	R-F 2K1% .125W F
A1	R400	8	0698-3540	R-F 15.4K1%
A1	R401	0	2100-3214	R-V 100K 10% .5W
A1	R402	0	2100-3214	R-V 100K 10% .5W
A1	R403	0	2100-3214	R-V 100K 10% .5W
A1	R404	4	0698-4446	R-F 267 .125W 1%
A1	R405	1	0757-0426	R-F 1.3K .125W 1%
A1	R406	1	0757-0426	R-F 1.3K .125W 1%
A1	R407	7	2100-3211	R-TRMR 1K 10%
A1	R408	4	0698-4446	R-F 267 .125W 1%
A1	R409	9	2100-0558	RES-TRMR 20K 10%
A1	R410	7	2100-3211	R-TRMR 1K 10%
A1	R411	9	0757-0278	R-F 1.78K1%
A1	R412	9	0698-7220	R-F 215 1% .05W
A1	R413	9	2100-0558	RES-TRMR 20K 10%
A1	R414	9	2100-0558	RES-TRMR 20K 10%
A1	R415	0	0698-7205	R-F 51.1 1% .05W
A1	R416	9	2100-0558	RES-TRMR 20K 10%
A1	R417	9	2100-0558	RES-TRMR 20K 10%
A1	R418	9	2100-0558	RES-TRMR 20K 10%
A1	R419	1	0698-3428	R-F 14.7 1%
A1	R420	1	0698-3428	R-F 14.7 1%
A1	R421	0	0698-7221	R-F 237 1% .05W
A1	R422	1	0757-0288	R-F 9.09K 1% .125
A1	R423	3	0698-3438	R-F 147 1% .125W
A1	R424	3	0757-0280	R-F 1K1% .125W F
A1	R425	0	2100-0567	R-VAR 2K 10% .5W
A1	R426	3	0757-0280	R-F 1K1% .125W F
A1	R427	3	0698-3438	R-F 147 1% .125W
A1	R428 *	1	0698-7264	R-F 14.7K .05W 1%
A1	R430	3	0698-4444	R-F 4.87K1%
A1	R431	3	0698-4444	R-F 4 87K1%
A1	R432	4	0757-0273	R-F 3 01K1%
A1	R433	3	0698-4444	R-F 4.87K1%
A1	R434	3	0698-4444	R-F 4.87K1%
A1	R435	3	0698-3446	R-F 383 1% .125W
A1	R436	5	0698-3258	R-F 5.36K1%
A1	R437	0	0698-4425	R-F 1.54K1%
A1	R438	1	0698-3155	R-F 4.64K 1% 125
A1	R439 *	4	0757-0444	R-F 12.1K 1%
A1	R440	0	0757-0419	R-F 681 1% .125W
A1	R441	7	0698-3432	R-F 26.1 1%
A1	R445	9	2100-3214	R-VAR 100K 10%
A1	R446	6	0757-0449	R-F 20K1% .125W
A1	R447	4	0698-8958	R-F 511K 1%
A1	R449	9	0698-3450	R-F 42.2K 1%
A1	R450	0	2100-3214	R-V 100K 10% .5W
A1	R451	3	0698-4486	R-F 24.9K1%
A1	R452	1	0757-0460	R-F 61.9K 1%
A1	R453	7	0698-4498	R-F 53.6K1%
A1	R501	8	0698-7196	R-F 21.5 2% .05W
A1	R502	9	0757-0385	R-F 22.1 1%
A1	R503	0	0698-4392	R-F 71.5 1/8W 1%
A1	R504	9	0757-0294	R-F 17.8 1%
A1	R505	2	0757-0346	R-F 10 1% .125W
A1	R506	7	0698-3440	R-F 196 1% .125W
A1	R507		0698-0644	R-F 7.87 1%
A1	R508	3	0757-0462	R-F 75K1% .125W
A1	R509		0698-4421	R-F 249 1% .125W
A1	R510	7	0757-0440	R-F 7.5K 1% .125W
A1	R511	7	0698-3359	R-F 12.7K1%
A1	R512	7	0698-3359	R-F 12.7K1%
A1	R513	5	0698-3498	R-F 8 66K1%
A1	R514	3	0698-4460	R-F 649 1% .125W
A1	R515	1	2100-0568	R-VAR 100
A1	R516	0	0757-0443	R-F 11K1% .125W
A1	R517	0	0757-0443	R-F 11K1% .125W
A1	R518	2	0698-4386	R-F 59.0 1/8W 1%
A1	R519	2	0698-4386	R-F 59.0 1/8W 1%
A1	R520	3	0757-0280	R-F 1K1% .125W F
A1	R521	3	0757-0280	R-F 1K1% .125W F
A1	R522	3	0757-0280	R-F 1K1% .125W F
A1	R523	3	0757-0280	R-F 1K1% .125W F
A1	R524	0	0757-0401	R-F 100 1% .125W
A1	R525	6	0757-0283	R-F 2K1% .125W F
A1	R526	6	0757-0283	R-F 2K1% .125W F
A1	R527	0	0757-0401	R-F 100 1% .125W
A1	R528	2	0698-3495	R-F 866 1% .125W
A1	R529	2	0698-3495	R-F 866 1% .125W
A1	R530	3	0757-1022	R-F 1.78K 1%
A1	R531	3	0757-1022	R-F 1.78K 1%
A1	R532	3	0757-0751	R-F 7.5K 1% .25W
A1	R533	2	0698-3429	R F 19.6 1%
A1	R534	2	0698-3429	R F 19.6 1%
A1	R535	7	2100-3211	R-TRMR 1K 10%
A1	R536	1	0698-7221	R-F 237 .05 1%
A1	R537	2	0698-3429	R F 19.6 1%
A1	R538	2	0698-3429	R F 19.6 1%
A1	R539	7	0698-8820	R-F 4.64 1% .25W
A1	R540	7	0698-8820	R-F 4 64 1% .25W
A1	R541	2	0698-3495	R-F 866 1% .125W
A1	R542	2	0698-3495	R-F 866 1% .125W
A1	R543	2	0757-0346	R-F 10 1% .125W
A1	R544	2	0757-0346	R-F 10 1% .125W
A1	R545	2	0757-0346	R-F 10 1% .125W
A1	R546	2	0757-0346	R-F 10 1% .125W
A1	R547	3	0766-0025	R-F 101 2% 3W MO
A1	R548	3	0766-0025	R-F 101 2% 3W MO
A1	R549	3	0757-0818	R-F 825 1% .5W
A1	R550	1	0698-4864	R-F 499 1% .5W
A1	R551	8	0757-1001	R-F 56.2 1% .5W
A1	R552	3	0757-0280	R-F 1K1% .125W F
A1	R553	8	0698-8369	R-F 2.7 .125W 5%
A1	R554	9	0698-4367	R-F 20.5 1%
A1	R555	9	0698-4367	R-F 20.5 1%

Table 6-3. Replaceable Parts

REFERENCE DESIGNATOR		CD	H-P PART NUMBER	DESCRIPTION
A1			08116-66511	BD AY-MAIN
A1	R556 *	0	0698-7195	R-F 19.6
A1	R558 *	4	0698-7209	R-F 75 1% .05W
A1	R559	5	0757-0399	R-F 82.5 1%
A1	R560	5	0757-0399	R-F 82.5 1%
A1	R561		0757-0279	R-F 3.16K .125W 1%
A1	R590	1	0757-0460	R-F 61.9K 1%
A1	R591	7	0698-3226	R-F 6.49K1%
A1	R592	9	0757-0442	R-F 10K1% .125W
A1	S1	2	3101-2091	SWITCH PUSHBUT
A1	U1	3	1826-0315	IC LM348
A1	U2	3	1826-0315	IC LM348
A1	U3	7	1826-0393	IC-LINEAR LM317T
A1	U4	9	1826-0527	IC LM337T
A1	U5	7	1826-0393	IC-LINEAR LM317T
A1	U6	9	1826-0527	IC LM337T
A1	U100	1	1820-0810	IC MC 10116
A1	U101	0	1826-0346	IC LM358N
A1	U102	1	1820-0802	IC-ECL 10102
A1	U103	6	1820-1730	IC OCTFF74LS273
A1	U104	5	1820-1359	IC MC10174P MUXR
A1	U110	3	1820-1216	IC-SN74LS138
A1	U150	6	1820-1730	IC OCTFF74LS273
A1	U151	0	1826-0207	IC LM 318 OP AMP
A1	U152	2	1820-1546	IC-4052B
A1	U200	9	1826-0753	IC 3400 4B
A1	U201		1826-0955	IC SLOPE GEN
A1	U202	7	1826-0111	IC-DUAL OP AMPL
A1	U203	4	1820-1225	IC DGTL FLIPFLOP
A1	U204	9	1826-0501	IC-CMOS 4053B
A1	U205	2	1820-1546	IC-4052B
A1	U210	7	1820-1997	IC SN74LS374CP
A1	U300		5180-2410	IC TIMING SEL
A1	U301	9	1820-1212	IC SN74LS112
A1	U302	6	1820-1491	IC-SN74LS367N
A1	U400	2	1820-1546	IC-4052B
A1	U401		1826-0923	SHAPER SEL TEMP
A1	U501	9	1826-0635	IC 714
A1	U502	9	1826-0635	IC 714
A1	U503	7	1820-1997	IC SN74LS374CP
A1	VR1	7	1902-0680	DIO 6.2V 5% .25W
A1	VR200	7	1902-0680	DIO 6.2V 5% .25W
A1	VR501	0	1902-3182	DIO 12.1V 5% .4W
A1	VR502	0	1902-3182	DIO 12.1V 5% .4W
A1	W2	0	8159-0005	JUMPER
A1	W3	0	8159-0005	JUMPER
A1	W4	0	8159-0005	JUMPER
A1	W5	0	8159-0005	JUMPER
A1	W7		5180-2401	CBL RBN 150 MM
A1	W8		08116-61605	CABLE ASSY. SIG.O/P
A1	W9		08116-61607	CABLE ASSY. TRIG."
A1	W10		08116-61609	CABLE ASSY. TRIGI/P
A1	W11		08116-61608	CABLE ASSY. CNTRI/P

REFERENCE DESIGNATOR		CD	H-P PART NUMBER	DESCRIPTION
A2			08116-66502	BD AY-CONTROL
A2	C1	9	0160-3839	C-F 2.2UF 10%
A2	C2	6	0160-3878	C-F .001UF 100V
A2	C4	0	0180-2856	C-F 47UF 10% 25V
A2	C5	5	0160-0576	C-F .1UF 20% CER
A2	C7	3	0160-4386	C-F 33PF 5% 200V
A2	C8	3	0160-4386	C-F 33PF 5% 200V
A2	C9	7	0160-3879	C-F .01UF 100V
A2	C10	0	0180-2856	C-F 47UF 10% 25V
A2	C11	0	0180-2856	C-F 47UF 10% 25V
A2	C12	7	0160-3879	C-F .01UF 100V
A2	C14	7	0160-3879	C-F .01UF 100V
A2	C15	3	0160-3718	C-F .047 UF 250V
A2	C16	0	0180-2856	C-F 47UF 10% 25V
A2	C17	5	0160-0576	C-F .1UF 20% CER
A2	C18	5	0160-0576	C-F .1UF 20% CER
A2	C19	5	0160-0576	C-F .1UF 20% CER
A2	C23	5	0160-0576	C-F .1UF 20% CER
A2	C26	5	0160-0576	C-F .1UF 20% CER
A2	C29	5	0160-0576	C-F .1UF 20% CER
A2	CR1	1	1901-1098	DIO-SWIT.1N4150
A2	CR2	1	1901-1098	DIO-SWIT.1N4150
A2	CR3	1	1901-1098	DIO-SWIT.1N4150
A2	CR4	1	1901-1098	DIO-SWIT.1N4150
A2	CR7	9	1901-0535	DIO SCHOTTKY
A2	CR8	9	1901-0535	DIO SCHOTTKY
A2	CR9	9	1901-0535	DIO SCHOTTKY
A2	CR10	9	1901-0535	DIO SCHOTTKY
A2	CR11	9	1901-0535	DIO SCHOTTKY
A2	CR12	9	1901-0535	DIO SCHOTTKY
A2	J4	2	1251-3119	CONN 20PIN RIBN
A2	J5	2	1251-3119	CONN 20PIN RIBN
A2	K1	5	0490-1137	RELAY-REED 1A
A2	K2	5	0490-1137	RELAY-REED 1A
A2	K3	5	0490-1137	RELAY-REED 1A
A2	K4	5	0490-1137	RELAY-REED 1A
A2	Q1	1	1854-0215	XSTR SI 2N3904
A2	Q2	2	1853-0036	XSTR SI 2N3906
A2	Q3	2	1854-0472	XSTR SI MPS A14
A2	Q4	2	1854-0472	XSTR SI MPS A14
A2	Q5	2	1853-0036	XSTR SI 2N3906
A2	R1	7	0757-0200	R-F 5.62K1%
A2	R2	5	2100-0554	R-V 500 10% .5W
A2	R3	3	0757-0420	R-F 750 1% .125W
A2	R4	6	2100-3210	R-VAR 10K 10% .5W
A2	R6	5	0698-4123	R-F 499 1% .125W
A2	R7	3	0698-4014	R-F 787 1% .125W
A2	R8	6	0757-0283	R-F 2K1% .125W F
A2	R9	6	0757-0449	R-F 20K1% .125W
A2	R10	5	0757-0472	R-F 200K1% .125W
A2	R11	4	0698-8827	R-F 1M 1% .125W
A2	R12	4	0698-8827	R-F 1M 1% .125W
A2	R14	5	0698-3258	R-F 5.36K1%
A2	R15	3	0698-4014	R-F 787 1% .125W
A2	R16	1	1810-0316	R-NETWORK 8X10K
A2	R17	0	2100-3214	R-V 100K 10% .5W
A2	R18	0	2100-3214	R-V 100K 10% .5W
A2	R19	1	0757-0428	R-F 1.62K 1%

Table 6-3. Replaceable Parts

REFERENCE DESIGNATOR		CD	H-P PART NUMBER	DESCRIPTION
A2	R20	3	0698-3446	R-F 383 1% .125W
A2	R21		1810-0470	R-NETWORK 8X2.2K
A2	R22	0	2100-3214	R-V 100K 10% .5W
A2	R23		0757-0476	R-F 301K 1% .125
A2	R24	5	2100-0554	R-V 500 10% .5W
A2	R25	0	2100-3214	R-V 100K 10% .5W
A2	R26		0757-0476	R-F 301K 1% .125
A2	R27	5	2100-0554	R-V 500 10% .5W
A2	R28	1	0698-4442	R-F 4.42K1%
A2	R29	8	0757-0417	R-F 562 1% .125W
A2	R30	9	0698-3152	R-F 3.48 k
A2	R31	0	2100-0567	R-VAR 2K 10% .5W
A2	R32	0	2100-0567	R-VAR 2K 10% .5W
A2	R33	3	0757-0458	R-F 51.1k
A2	R35	0	0757-0401	R-F 100 1% .125W
A2	R36	0	0757-0401	R-F 100 1% .125W
A2	R41	6	0698-6360	R-F 10K.1% .125W
A2	R42	6	0698-6360	R-F 10K.1% .125W
A2	R43	0	2100-3252	R-TRMR 5%
A2	R44	6	0757-0465	R-F 100K1% .125W
A2	R45	1	0698-3155	R-F 4.64K 1%.125
A2	R46	6	0757-0465	R-F 100K1% .125W
A2	R47	3	0698-4486	R-F 24.9K1%
A2	R48	4	0698-4487	R-F 25.5K 1%
A2	R50	8	1810-0206	R-NETWORK 7X10K
A2	R51	3	0757-0280	R-F 1K1% .125W F
A2	R52	1	0698-3452	R-F 147K1% .125W
A2	R54	8	0757-0277	R-F 49.9 1%
A2	R55	1	0698-3444	R-F 316 1% .125W
A2	R56	2	0698-6324	R-F 187 1% .125W
A2	U1	9	1826-0519	IC TL071CC
A2	U2	9	1826-0519	IC TL071CC
A2	U3	2	1820-1885	IC-SN74LS173
A2	U4	5	1826-0276	IC 78L05 V RGLTR
A2	U5	9	1826-0753	IC 3400 4B
A2	U6	3	1826-0729	IC-CONV 7522JN
A2	U7	9	1826-0635	IC 714
A2	U8	4	1826-0639	IC-7524JN
A2	U9	9	1826-0635	IC 714
A2	U10	4	1826-0639	IC-7524JN
A2	U11	9	1826-0635	IC 714
A2	U12	3	1826-0521	IC-TL 072CP
A2	U13	3	1826-0729	IC-CONV 7522JN
A2	U14	3	1820-1216	IC-SN74LS138
A2	U15	6	1820-1730	IC OCTFF74LS273
A2	U16	9	1826-0501	IC-CMOS 4053B
A2	U17	9	1826-0501	IC-CMOS 4053B
A2	U19	1	1820-1199	IC SN74LS 04
A2	U20	3	1820-1216	IC-SN74LS138
A2	U21	6	1820-1730	IC OCTFF74LS273
A2	U22	6	1820-1730	IC OCTFF74LS273
A2	U23	6	1820-1730	IC OCTFF74LS273
A2	U24		1826-0697	IC CONV 18-DIP-P
A2	U25	9	1826-0635	IC 714
A2	U26	9	1826-0635	IC 714
A2	U27	3	1826-0729	IC-CONV 7522JN
A2	U28	3	1826-0521	IC-TL 072CP
A2	U31	0	1826-0180	IC TIMER NE555E
A2	U40	9	1820-1197	IC SN74LS00
A2	U43	6	1820-1730	IC OCTFF74LS273

REFERENCE DESIGNATOR		CD	H-P PART NUMBER	DESCRIPTION
A2	VR1	4	1902-0786	DIO-ZNR 9V 5%.5W
A2	VR2	7	1902-0949	DIO-ZNR 4.3V
A2	W1	0	8159-0005	JUMPER
A2	W2	0	8159-0005	JUMPER
A3			08116-66503	BD AY-MICROPRCR
A3	BT1	6	1420-0251	BATTERY-NICAD
A3	C1	3	0160-4493	C-F 27PF 5% 200V
A3	C2	3	0160-4493	C-F 27PF 5% 200V
A3	C3	5	0160-0576	C-F .1UF 20% CER
A3	C4	5	0160-0576	C-F .1UF 20% CER
A3	C5	5	0160-0576	C-F .1UF 20% CER
A3	C6	0	0180-2856	C-F 47UF 10% 25V
A3	C7	5	0180-2207	C-F 100UF 10V
A3	C8	0	0180-2856	C-F 47UF 10% 25V
A3	C9	5	0160-0576	C-F .1UF 20% CER
A3	C11	5	0160-0576	C-F .1UF 20% CER
A3	C12	5	0160-0576	C-F .1UF 20% CER
A3	C13	5	0160-0576	C-F .1UF 20% CER
A3	C14	5	0160-0576	C-F .1UF 20% CER
A3	C15	5	0160-0576	C-F .1UF 20% CER
A3	C16	5	0160-0576	C-F .1UF 20% CER
A3	C17	5	0160-0576	C-F .1UF 20% CER
A3	C18	5	0160-0576	C-F .1UF 20% CER
A3	C19	5	0160-0576	C-F .1UF 20% CER
A3	C20	5	0160-0576	C-F .1UF 20% CER
A3	C21	5	0160-0576	C-F .1UF 20% CER
A3	C22	5	0160-0576	C-F .1UF 20% CER
A3	C23	5	0160-0576	C-F .1UF 20% CER
A3	C24	5	0160-0576	C-F .1UF 20% CER
A3	C25	5	0160-0576	C-F .1UF 20% CER
A3	C26	5	0160-0576	C-F .1UF 20% CER
A3	C27	5	0160-0576	C-F .1UF 20% CER
A3	C28	5	0160-0576	C-F .1UF 20% CER
A3	C29	5	0160-3877	C-F 100PF 200V
A3	C30	5	0160-0576	C-F .1UF 20% CER
A3	C31	5	0160-0576	C-F .1UF 20% CER
A3	C32	5	0160-0576	C-F .1UF 20% CER
A3	C33	5	0160-0576	C-F .1UF 20% CER
A3	C34	5	0160-0576	C-F .1UF 20% CER
A3	C36	5	0160-0576	C-F 1UF 20% CER
A3	CR1	9	1901-0535	DIO SCHOTTKY
A3	CR2	9	1901-0535	DIO SCHOTTKY
A3	CR3	1	1901-1098	DIO-SWIT.1N4150
A3	CR4	1	1901-1098	DIO-SWIT.1N4150
A3	J1	0	1251-3141	CONN 50PIN RIBN
A3	J2	8	1251-0541	CONN 34PIN RIBN
A3	J3	0	1251-3167	CONNECTOR 4 PIN
A3	MP1	7	1400-0824	CABLE STRAP
A3	P1	5	1258-0124	PIN PROG JUMPER
A3	Q1	9	1853-0281	XSTR SI 2907A
A3	R1	8	1810-0280	R-NETWORK 9X10K
A3	R2	7	0698-8812	R-F 1 1% .125W
A3	R3	3	1810-0277	R-NETWORK 9X2.2K
A3	R4	7	1810-0338	R-NETWORK 8X100
A3	R5	7	1810-0338	R-NETWORK 8X100

Table 6-3. Replaceable Parts

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A3			08116-66503	BD AY-MICROPRCR
A3	R6	3	0757-0412	R-F 365 1% .125W
A3	R7	6	0757-0407	R-F 200 1% .125W
A3	R8	6	0757-0465	R-F 100K1% .125W
A3	R9	6	0757-0465	R-F 100K1% .125W
A3	R10	3	1810-0037	R-NETWORK DIP
A3	R11	8	1810-0503	R-NETWORK 3.3K
A3	R12	1	1810-0316	R-NETWORK 8X10K
A3	R13	8	1810-0206	R-NETWORK 7X10K
A3	R14	9	1810-0330	R-NETWORK 8X470
A3	R15		1810-0280	R-NETWORK 9X10K
A3	R16		1810-0378	R-NETWORK 47K
A3	R17	7	0698-8812	R-F 1 1% .125W
A3	R18	3	0757-0280	R-F 1K1% .125W F
A3	R19	3	0757-0280	R-F 1K1% .125W F
A3	R20	3	0757-0280	R-F 1K1% .125W F
A3	RT1	5	0837-0050	THMS 1K DIS
A3	TP8		0360-0535	TERM TEST POINT
A3	U1	2	1820-2099	IC MPU MC6802P
A3	U2	4	1820-2075	IC SN74LS245
A3	U3	3	1820-2024	IC SN74LS244
A3	U4	3	1820-2024	IC SN74LS244
A3	U5	3	1818-3103	ROM B
A3	U6	4	1818-3104	ROM A
A3	U7	5	1818-3105	ROM 9
A3	U8	6	1818-3106	ROM 8
A3	U9	7	1818-3107	ROM 7
A3	U10	7	1818-1330	IC RAM 444C
A3	U11	7	1818-1330	IC RAM 444C
A3	U12	3	1820-1216	IC-SN74LS138
A3	U13	3	1820-1216	IC-SN74LS138
A3	U14	3	1820-1216	IC-SN74LS138
A3	U15	3	1820-1414	IC 74LS12
A3	U16	7	1820-1997	IC SN74LS374CP
A3	U17	3	1820-2861	IC 74 F/38
A3	U18	6	1820-1730	IC OCTFF74LS273
A3	U19	1	1820-1298	IC-SN74LS251
A3	U20	7	1820-1426	IC-SN74LS145
A3	U21	3	1820-2024	IC SN74LS244
A3	U22	4	1820-2132	IC ICM7218A
A3	U23	7	1820-1997	IC SN74LS374CP
A3	U24	7	1820-1997	IC SN74LS374CP
A3	U25	4	1820-2075	IC SN74LS245
A3	U26	3	1820-2024	IC SN74LS244
A3	U27	7	1826-0161	IC-LM 324N
A3	U28	8	1858-0058	XSTR QUAD PNP
A3	U29	3	1858-0053	XSTR QUAL NPN
A3	U30	8	1820-2219	IC
A3	U31	3	1820-2058	IC MC3448AL
A3	U32	3	1820-2058	IC MC3448AL
A3	U33	3	1820-2058	IC MC3448AL
A3	U34	3	1820-2058	IC MC3448AL
A3	U35	1	1820-1416	IC SN74LS14N
A3	U36	7	1820-1640	IC SN74LS366N
A3	U37	7	1820-1195	IC SN74LS175N
A3	U38	8	1818-3108	ROM 6
A3			8159-0005	JUMPER
A3	W4	0	5180-2405	CBL RBN 350 MM
A3	Y1	2	0410-0762	QUARTZ 4MHZ

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A4			08116-66504	BD AY-KEY
A4	DS1	3	1990-0665	LAMP-SOLID STATE
A4	DS2	3	1990-0665	LAMP-SOLID STATE
A4	DS3	3	1990-0665	LAMP-SOLID STATE
A4	DS4	3	1990-0665	LAMP-SOLID STATE
A4	DS5	3	1990-0665	LAMP-SOLID STATE
A4	DS6	3	1990-0665	LAMP-SOLID STATE
A4	DS7	3	1990-0665	LAMP-SOLID STATE
A4	DS8	3	1990-0665	LAMP-SOLID STATE
A4	MP8	6	5041-0285	KEY-CAP PRL-G LT
A4	MP9	6	5041-0285	KEY-CAP PRL-G LT
A4	MP10	6	5041-0285	KEY-CAP PRL-G LT
A4	DS11	3	1990-0665	LAMP-SOLID STATE
A4	DS12	3	1990-0665	LAMP-SOLID STATE
A4	DS13	3	1990-0665	LAMP-SOLID STATE
A4	DS14	3	1990-0665	LAMP-SOLID STATE
A4	DS15	3	1990-0665	LAMP-SOLID STATE
A4	MP15	6	5041-0285	KEY-CAP PRL-G LT
A4	MP16	6	5041-0285	KEY-CAP PRL-G LT
A4	DS17	3	1990-0665	LAMP-SOLID STATE
A4	MP17	6	5041-0285	KEY-CAP PRL-G LT
A4	DS18	3	1990-0665	LAMP-SOLID STATE
A4	MP20	6	5041-0285	KEY-CAP PRL-G LT
A4	MP21	6	5041-0285	KEY-CAP PRL-G LT
A4	MP22	6	5041-0285	KEY-CAP PRL-G LT
A4	MP23	6	5041-0285	KEY-CAP PRL-G LT
A4	MP24	6	5041-0285	KEY-CAP PRL-G LT
A4	J1		1251-6255	CONN-POST 20F
A4	J2		1251-6255	CONN-POST 20F
A4	MP1	5	5041-0309	CAP KEY QUARTER
A4	MP2	5	5041-0309	CAP KEY QUARTER
A4	MP7	0	5041-0726	KEY CAP LCL
A4	MP11	5	5041-0276	KEY-CAP PRL-GRAY
A4	MP13	7	5041-0351	KEY-CAP SRF-G LT
A4	MP14	7	5041-0351	KEY-CAP SRF-G LT
A4	MP18	7	5041-0351	KEY-CAP SRF-G LT
A4	MP19	7	5041-0351	KEY-CAP SRF-G LT
A4	S1	7	5060-9436	SW P-BTN SINGLE
A4	S3	7	5060-9436	SW P-BTN SINGLE
A4	S7	7	5060-9436	SW P-BTN SINGLE
A4	S8	7	5060-9436	SW P-BTN SINGLE
A4	S9	7	5060-9436	SW P-BTN SINGLE
A4	S10	7	5060-9436	SW P-BTN SINGLE
A4	S11	7	5060-9436	SW P-BTN SINGLE
A4	S13	7	5060-9436	SW P-BTN SINGLE
A4	S14	7	5060-9436	SW P-BTN SINGLE
A4	S15	7	5060-9436	SW P-BTN SINGLE
A4	S16	7	5060-9436	SW P-BTN SINGLE
A4	S17	7	5060-9436	SW P-BTN SINGLE
A4	S18	7	5060-9436	SW P-BTN SINGLE
A4	S19	7	5060-9436	SW P-BTN SINGLE
A4	S20	7	5060-9436	SW P-BTN SINGLE
A4	S21	7	5060-9436	SW P-BTN SINGLE
A4	S22	7	5060-9436	SW P-BTN SINGLE
A4	S23	7	5060-9436	SW P-BTN SINGLE
A4	S24	7	5060-9436	SW P-BTN SINGLE
A4	W1	8	5180-2403	CBL RBN 260 MM

Table 6-3. Replaceable Parts

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A5			08116-66505	BD AY DISPLAY
A5	DS1	6	1990-0486	LED-VISIBLE RED
A5	DS4		1990-0806	LED HLMP-2300RED
A5	DS5	5	1990-0774	LED HLMP 2600
A5	DS6	5	1990-0774	LED HLMP 2600
A5	DS7	5	1990-0774	LED HLMP 2600
A5	DS15	6	1990-0486	LED-VISIBLE RED
A5	DS16	6	1990-0486	LED-VISIBLE RED
A5	DS17	6	1990-0486	LED-VISIBLE RED
A5	DS18		1990-0806	LED HLMP-2300RED
A5	DS19	6	1990-0486	LED-VISIBLE RED
A5	DS20	6	1990-0486	LED-VISIBLE RED
A5	DS21	6	1990-0486	LED-VISIBLE RED
A5	DS22	6	1990-0486	LED-VISIBLE RED
A5	DS23	6	1990-0486	LED-VISIBLE RED
A5	DS24	6	1990-0486	LED-VISIBLE RED
A5	DS25	6	1990-0486	LED-VISIBLE RED
A5	DS26	6	1990-0486	LED-VISIBLE RED
A5	DS27	6	1990-0486	LED-VISIBLE RED
A5	DS28	6	1990-0486	LED-VISIBLE RED
A5	DS33	6	1990-0486	LED-VISIBLE RED
A5	DS34	6	1990-0486	LED-VISIBLE RED
A5	DS35	6	1990-0486	LED-VISIBLE RED
A5	DS36	6	1990-0486	LED-VISIBLE RED
A5	DS37	6	1990-0486	LED-VISIBLE RED
A5	DS38	6	1990-0486	LED-VISIBLE RED
A5	DS40	6	1990-0486	LED-VISIBLE RED
A5	DS41	2	1990-0846	DISPLAY SOLID ST
A5	DS42	2	1990-0846	DISPLAY SOLID ST
A5	DS43	2	1990-0846	DISPLAY SOLID ST
A5	DS44	2	1990-0846	DISPLAY SOLID ST
A5	J1		1251-7431	CONN POST 20M
A5	J2		1251-7431	CONN POST 20M
A5	S1		3101-2529	SW RPR
A5	S2		3101-2529	SW RPR
A5	S3		3101-2529	SW RPR
A5	S4		3101-2529	SW RPR
A6			08116-66506	BD AY HPIB
A6	S1	1	3101-1860	SW AY-SL
A6	J1		1251-3283	CONN R&P MICRO
A6	W2		5180-2404	CABLE RBN 300 N.N.

Table 6-3. Replaceable Parts

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
FRAME				
A2		8	08116-66512	BD AY-CONTR. OPT
A4		0	08116-66514	BD AY-KEY OPT
A5		1	08116-66515	BD AY-DISPL OPT
J5		1	1250-0083	CONN BNC BLKHD
J6		1	1250-0083	CONN BNC BLKHD
J7		9	1251-2291	JACK TELE
MP3		8	4040-1973	PANEL FRONT
MP9			08116-60254	PANEL REAR
MP45		8	2950-0001	NUT-HEX 318-32TH
A2			08116-66512	BD AY-CONTR. OPT
A2	C1	9	0160-3839	C-F 2.2UF 10%
A2	C2	6	0160-3878	C-F .001UF 100V
A2	C4	0	0180-2856	C-F 47UF 10% 25V
A2	C5	5	0160-0576	C-F .1UF 20% CER
A2	C7	3	0160-4386	C-F 33PF 5% 200V
A2	C8	3	0160-4386	C-F 33PF 5% 200V
A2	C9	7	0160-3879	C-F .01UF 100V
A2	C10	0	0180-2856	C-F 47UF 10% 25V
A2	C11	0	0180-2856	C-F 47UF 10% 25V
A2	C12	7	0160-3879	C-F .01UF 100V
A2	C13	5	0160-3877	C-F 100PF 200V
A2	C14	7	0160-3879	C-F .01UF 100V
A2	C15	3	0160-3718	C-F .047 UF 250V
A2	C16	0	0180-2856	C-F 47UF 10% 25V
A2	C17	5	0160-0576	C-F .1UF 20% CER
A2	C18	5	0160-0576	C-F .1UF 20% CER
A2	C19	5	0160-0576	C-F .1UF 20% CER
A2	C20	5	0160-3877	C-F 100PF 200V
A2	C21	3	0160-4386	C-F 33PF 5% 200V
A2	C22	5	0160-0576	C-F .1UF 20% CER
A2	C23	5	0160-0576	C-F .1UF 20% CER
A2	C24	5	0160-0576	C-F .1UF 20% CER
A2	C25	5	0160-0576	C-F .1UF 20% CER
A2	C26	5	0160-0576	C-F .1UF 20% CER
A2	C27	5	0160-0576	C-F .1UF 20% CER
A2	C28	5	0160-0576	C-F .1UF 20% CER
A2	C29	5	0160-0576	C-F .1UF 20% CER
A2	C30	5	0160-0576	C-F .1UF 20% CER
A2	C31	5	0160-0576	C-F .1UF 20% CER
A2	CR1	1	1901-1098	DIO-SWIT 1N4150
A2	CR2	1	1901-1098	DIO-SWIT 1N4150
A2	CR3	1	1901-1098	DIO-SWIT 1N4150
A2	CR4	1	1901-1098	DIO-SWIT 1N4150
A2	CR5	1	1901-1098	DIO-SWIT 1N4150
A2	CR6	1	1901-1098	DIO-SWIT 1N4150
A2	CR7	9	1901-0535	DIO SCHOTTKY
A2	CR8	9	1901-0535	DIO SCHOTTKY
A2	CR9	9	1901-0535	DIO SCHOTTKY
A2	CR10	9	1901-0535	DIO SCHOTTKY
A2	CR11	9	1901-0535	DIO SCHOTTKY
A2	CR12	9	1901-0535	DIO SCHOTTKY
A2	CR13	9	1901-0535	DIO SCHOTTKY
A2	CR14	1	1901-1098	DIO-SWIT 1N4150
A2	CR15	1	1901-1098	DIO-SWIT 1N4150
A2	CR16	1	1901-1098	DIO-SWIT 1N4150
A2	CR17	1	1901-1098	DIO-SWIT 1N4150
A2	F1	1	2110-0343	FUSE 250A 125V
A2	F2	1	2110-0343	FUSE 250A 125V
A2	J4	2	1251-3119	CONN 20PIN RIBN
A2	J5	2	1251-3119	CONN 20PIN RIBN
A2	K1	5	0490-1137	RELAY-REED 1A
A2	K2	5	0490-1137	RELAY-REED 1A
A2	K3	5	0490-1137	RELAY-REED 1A
A2	K4	5	0490-1137	RELAY-REED 1A
A2	L1	0	9170-0894	CORE MAGNETIC
A2	L2	0	9170-0894	CORE MAGNETIC
A2	Q1	1	1854-0215	XSTR SI 2N3904
A2	Q2	2	1853-0036	XSTR SI 2N3906
A2	Q3	2	1854-0472	XSTR SI MPS A14
A2	Q4	2	1854-0472	XSTR SI MPS A14
A2	Q5	2	1853-0036	XSTR SI 2N3906
A2	Q6	1	1854-0215	XSTR SI 2N3904
A2	Q7	2	1853-0036	XSTR SI 2N3906
A2	R1	7	0757-0200	R-F 5.62K1%
A2	R2	5	2100-0554	R-V 500 10% .5W
A2	R3	3	0757-0420	R-F 750 1% .125W
A2	R4	6	2100-3210	R-VAR 10K 10% .5W
A2	R6	5	0698-4123	R-F 499 1% .125W
A2	R7	3	0698-4014	R-F 787 1% .125W
A2	R8	6	0757-0283	R-F 2K1% .125W F
A2	R9	6	0757-0449	R-F 20K1% .125W
A2	R10	5	0757-0472	R-F 200K1% .125W
A2	R11	4	0698-8827	R-F 1M 1% .125W
A2	R12	4	0698-8827	R-F 1M 1% .125W
A2	R13	1	0698-3444	R-F 316 1% .125W
A2	R14	5	0698-3258	R-F 5.36K1%
A2	R15	3	0698-4014	R-F 787 1% .125W
A2	R16	1	1810-0316	R-NETWORK 8X10K
A2	R17	0	2100-3214	R-V 100K 10% .5W
A2	R18	0	2100-3214	R-V 100K 10% .5W
A2	R19	1	0757-0428	R-F 1.62K 1%
A2	R20	3	0698-3446	R-F 383 1% .125W
A2	R21		1810-0470	R-NETWORK 8X2.2K
A2	R22	0	2100-3214	R-V 100K 10% .5W
A2	R23		0757-0476	R-F 301K 1% .125
A2	R24	5	2100-0554	R-V 500 10% .5W
A2	R25	0	2100-3214	R-V 100K 10% .5W
A2	R26		0757-0476	R-F 301K 1% .125
A2	R27	5	2100-0554	R-V 500 10% .5W
A2	R28	1	0698-4442	R-F 4.42K1%
A2	R29	8	0757-0417	R-F 562 1% .125W
A2	R30	9	0698-3153	R-F 3.83K1%
A2	R31	0	2100-0567	R-VAR 2K 10% .5W
A2	R32	0	2100-0567	R-VAR 2K 10% .5W
A2	R33	3	0698-4444	R-F 4.87K1%
A2	R35	0	0757-0401	R-F 100 1% .125W
A2	R36	0	0757-0401	R-F 100 1% .125W
A2	R37	9	0757-0442	R-F 10K1% .125W
A2	R38	9	0698-4424	R-F 1.4K1% .125W
A2	R39	9	0757-0442	R-F 10K1% .125W
A2	R40	3	0757-0280	R-F 1K1% .125W F
A2	R41	6	0698-6360	R-F 10K.1% .125W
A2	R42	6	0698-6360	R-F 10K.1% .125W
A2	R43	0	2100-0567	R-VAR 2K 10% .5W
A2	R44	6	0757-0465	R-F 100K1% .125W

Table 6-3. Replaceable Parts

REFERENCE DESIGNATOR		CD	H-P PART NUMBER	DESCRIPTION
A2	R45	1	0698-3155	R-F 4.64K 1%.125
A2	R46	6	0757-0465	R-F 100K1% .125W
A2	R47	3	0698-4486	R-F 24.9K1%
A2	R48	4	0698-4487	R-F 25.5K 1%
A2	R50	8	1810-0206	R-NETWORK 7X10K
A2	R51	3	0757-0280	R-F 1K1% .125W F
A2	R52	1	0698-3452	R-F 147K1% .125W
A2	R54	8	0757-0277	R-F 49.9 1%
A2	R55	1	0698-3444	R-F 316 1% .125W
A2	R56	2	0698-6324	R-F 187 1% .125W
A2	R57	3	0757-0280	R-F 1K1% .125W F
A2	R58	3	0757-0280	R-F 1K1% .125W F
A2	R59	3	1810-0243	R-NETWORK 8X6.8K
A2	R60	7	1810-0205	R-NETWORK 7X4.7K
A2	R61	8	1810-0206	R-NETWORK 7X10K
A2	R62	5	1810-0203	R-NETWORK 7X470
A2	R63	5	1810-0203	R-NETWORK 7X470
A2	R64	5	1810-0203	R-NETWORK 7X470
A2	R65	8	0698-3441	R-F 215 1% .125W
A2	R66	1	0757-0428	R-F 1.62K 1%
A2	R67	1	0757-0428	R-F 1.62K 1%
A2	U1	9	1826-0519	IC TL071CC
A2	U2	9	1826-0519	IC TL071CC
A2	U3	2	1820-1885	IC-SN74LS173
A2	U4	5	1826-0276	IC 78L05 V RGLTR
A2	U5	9	1826-0753	IC-TL 074 ACN
A2	U6	3	1826-0729	IC-CONV 7522JN
A2	U7	9	1826-0635	IC 714
A2	U8	4	1826-0639	IC-7524JN
A2	U9	9	1826-0635	IC 714
A2	U10	4	1826-0639	IC-7524JN
A2	U11	9	1826-0635	IC 714
A2	U12	3	1826-0521	IC-TL 072CP
A2	U13	3	1826-0729	IC-CONV 7522JN
A2	U14	3	1820-1216	IC-SN74LS138
A2	U15	6	1820-1730	IC OCTFF74LS273
A2	U16	9	1826-0501	IC-CMOS 4053B
A2	U17	9	1826-0501	IC-CMOS 4053B
A2	U18	6	1820-1730	IC OCTFF74LS273
A2	U19	1	1820-1199	IC SN74LS 04
A2	U20	3	1820-1216	IC-SN74LS138
A2	U21	6	1820-1730	IC OCTFF74LS273
A2	U22	6	1820-1730	IC OCTFF74LS273
A2	U23	6	1820-1730	IC OCTFF74LS273
A2	U24		1826-0697	IC CONV 18-DIP-P
A2	U25	9	1826-0635	IC 714
A2	U26	9	1826-0635	IC 714
A2	U27	3	1826-0729	IC-CONV 7522JN
A2	U28	3	1826-0521	IC-TL 072CP
A2	U29	3	1826-0729	IC-CONV 7522JN
A2	U30	3	1826-0521	IC-TL 072CP
A2	U31	0	1826-0180	IC TIMER NE555E
A2	U32	0	1820-0801	IC DGTL MC 10101
A2	U33	7	1820-1400	IC MC10104P
A2	U34	7	1820-1400	IC MC10104P
A2	U35	3	1820-0820	IC MC10135L
A2	U36	3	1820-0820	IC MC10135L
A2	U37	1	1820-1686	IC MC 10103
A2	U38	5	1820-1052	IC DGTL MC 10125
A2	U39	3	1820-1282	IC 74LS109 TTL
A2	U40	9	1820-1197	IC SN74LS00
A2	U41	7	1820-1278	IC 74LS 191
A2	U42	7	1820-1278	IC 74LS 191
A2	U43	6	1820-1730	IC OCTFF74LS273
A2	VR1	4	1902-0786	DIO-ZNR 9V 5% .5W
A2	VR2	7	1902-0949	DIO ZNR 4.3V
A2	W2	0	8159-0005	JUMPER
A2	W3	0	8159-0005	JUMPER
	A4		08116-66514	BD AY-KEY OPT
A4	DS1	3	1990-0665	LAMP-SOLID STATE
A4	DS2	3	1990-0665	LAMP-SOLID STATE
A4	DS3	3	1990-0665	LAMP-SOLID STATE
A4	DS4	3	1990-0665	LAMP-SOLID STATE
A4	DS5	3	1990-0665	LAMP-SOLID STATE
A4	DS6	3	1990-0665	LAMP-SOLID STATE
A4	DS7	3	1990-0665	LAMP-SOLID STATE
A4	DS8	3	1990-0665	LAMP-SOLID STATE
A4	DS9	3	1990-0665	LAMP-SOLID STATE
A4	DS10	3	1990-0665	LAMP-SOLID STATE
A4	DS11	3	1990-0665	LAMP-SOLID STATE
A4	DS12	3	1990-0665	LAMP-SOLID STATE
A4	DS13	3	1990-0665	LAMP-SOLID STATE
A4	DS14	3	1990-0665	LAMP-SOLID STATE
A4	DS15	3	1990-0665	LAMP-SOLID STATE
A4	DS16	3	1990-0665	LAMP-SOLID STATE
A4	DS17	3	1990-0665	LAMP-SOLID STATE
A4	DS18	3	1990-0665	LAMP-SOLID STATE
A4	J1		1251-6255	CONN-POST 20F
A4	J2		1251-6255	CONN-POST 20F
A4	MP1	5	5041-0309	CAP KEY QUARTER
A4	MP2	5	5041-0309	CAP KEY QUARTER
A4	MP3	5	5041-0309	CAP KEY QUARTER
A4	MP4	7	5041-0351	KEY-CAP SRF-G LT
A4	MP5	7	5041-0351	KEY-CAP SRF-G LT
A4	MP6	7	5041-0351	KEY-CAP SRF-G LT
A4	MP7	0	5041-0726	KEY CAP LCL
A4	2MP8	6	5041-0285	KEY-CAP PRL-G LT
A4	2MP9	6	5041-0285	KEY-CAP PRL-G LT
A4	2MP10	6	5041-0285	KEY-CAP PRL-G LT
A4	MP11	5	5041-0276	KEY-CAP PRL-GRAY
A4	MP12	5	5041-0276	KEY-CAP PRL-GRAY
A4	MP13	7	5041-0351	KEY-CAP SRF-G LT
A4	MP14	7	5041-0351	KEY-CAP SRF-G LT
A4	2MP15	6	5041-0285	KEY-CAP PRL-G LT
A4	2MP16	6	5041-0285	KEY-CAP PRL-G LT
A4	2MP17	6	5041-0285	KEY-CAP PRL-G LT
A4	MP18	7	5041-0351	KEY-CAP SRF-G LT
A4	MP19	7	5041-0351	KEY-CAP SRF-G LT
A4	2MP20	6	5041-0285	KEY-CAP PRL-G LT
A4	MP21	6	5041-0285	KEY-CAP PRL-G LT
A4	MP22	6	5041-0285	KEY-CAP PRL-G LT
A4	MP23	6	5041-0285	KEY-CAP PRL-G LT
A4	MP24	6	5041-0285	KEY-CAP PRL-G LT
A4	S1	7	5060-9436	SW P-BTN SINGLE
A4	S2	7	5060-9436	SW P-BTN SINGLE
A4	S3	7	5060-9436	SW P-BTN SINGLE
A4	S4	7	5060-9436	SW P-BTN SINGLE
A4	S5	7	5060-9436	SW P-BTN SINGLE
A4	S6	7	5060-9436	SW P-BTN SINGLE
A4	S7	7	5060-9436	SW P-BTN SINGLE
A4	S8	7	5060-9436	SW P-BTN SINGLE

Table 6-3. Replaceable Parts

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A4	S9	7	5060-9436	SW P-BTN SINGLE
A4	S10	7	5060-9436	SW P-BTN SINGLE
A4	S11	7	5060-9436	SW P-BTN SINGLE
A4	S12	7	5060-9436	SW P-BTN SINGLE
A4	S13	7	5060-9436	SW P-BTN SINGLE
A4	S14	7	5060-9436	SW P-BTN SINGLE
A4	S15	7	5060-9436	SW P-BTN SINGLE
A4	S16	7	5060-9436	SW P-BTN SINGLE
A4	S17	7	5060-9436	SW P-BTN SINGLE
A4	S18	7	5060-9436	SW P-BTN SINGLE
A4	S19	7	5060-9436	SW P-BTN SINGLE
A4	S20	7	5060-9436	SW P-BTN SINGLE
A4	S21	7	5060-9436	SW P-BTN SINGLE
A4	S22	7	5060-9436	SW P-BTN SINGLE
A4	S23	7	5060-9436	SW P-BTN SINGLE
A4	S24	7	5060-9436	SW P-BTN SINGLE
A4	W1	8	5180-2403	CBL RBN 260 MM
A5			08116-66515	BD AY-DISPL OPT
A5	DS1	6	1990-0486	LED-VISIBLE RED
A5	DS2	5	1990-0774	LED HLMP 2600
A5	DS3	5	1990-0774	LED HLMP 2600
A5	DS4	5	1990-0774	LED HLMP 2600
A5	DS5	5	1990-0774	LED HLMP 2600
A5	DS6	5	1990-0774	LED HLMP 2600
A5	DS7	5	1990-0774	LED HLMP 2600
A5	DS8		1990-0806	LED HLMP-2300RED
A5	DS15	6	1990-0486	LED-VISIBLE RED
A5	DS16	6	1990-0486	LED-VISIBLE RED
A5	DS17		1990-0486	LED-VISIBLE RED
A5	DS18		1990-0806	LED HLMP-2300RED
A5	DS19	6	1990-0486	LED-VISIBLE RED
A5	DS20	6	1990-0486	LED-VISIBLE RED
A5	DS21	6	1990-0486	LED-VISIBLE RED
A5	DS22	6	1990-0486	LED-VISIBLE RED
A5	DS23	6	1990-0486	LED-VISIBLE RED
A5	DS24	6	1990-0486	LED-VISIBLE RED
A5	DS25	6	1990-0486	LED-VISIBLE RED
A5	DS26	6	1990-0486	LED-VISIBLE RED
A5	DS27	6	1990-0486	LED-VISIBLE RED
A5	DS28	6	1990-0486	LED-VISIBLE RED
A5	DS29	6	1990-0486	LED-VISIBLE RED
A5	DS30	6	1990-0486	LED-VISIBLE RED
A5	DS31	6	1990-0486	LED-VISIBLE RED
A5	DS32	6	1990-0486	LED-VISIBLE RED
A5	DS33	6	1990-0486	LED-VISIBLE RED
A5	DS34	6	1990-0486	LED-VISIBLE RED
A5	DS35	6	1990-0486	LED-VISIBLE RED
A5	DS36	6	1990-0486	LED-VISIBLE RED
A5	DS37	6	1990-0486	LED-VISIBLE RED
A5	DS38	6	1990-0486	LED-VISIBLE RED
A5	DS39	6	1990-0486	LED-VISIBLE RED
A5	DS40	6	1990-0486	LED-VISIBLE RED
A5	DS41	2	1990-0846	DISPLAY SOLID ST
A5	DS42	2	1990-0846	DISPLAY SOLID ST
A5	DS43	2	1990-0846	DISPLAY SOLID ST
A5	DS44	2	1990-0846	DISPLAY SOLID ST
A5	J1		1251-7431	CONN POST 20M
A5	J2		1251-7431	CONN POST 20M
A5	J3	5	1251-7429	CONN POST 5MALE

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A5	S1		3101-2529	SW RPR
A5	S2		3101-2529	SW RPR
A5	S3		3101-2529	SW RPR
A5	S4		3101-2529	SW RPR

SECTION VII
BACKDATING

7–1 INTRODUCTION

7–2 This section contains backdating information, which adapts this manual to instruments with serial numbers lower than that shown on the title page.

7–3 CHANGE SEQUENCE

7–4 Changes are listed in the serial number order that they occurred in the manufacture of the instrument. However, in adapting this manual to an instrument with a particular serial number, apply the changes in the reverse order. That is, begin with the latest change that applies to the serial number in question. Table 7–1 lists the serial numbers to which each change applies. Where changes to components occur, alter the associated schematic and layout diagram as necessary.

Table 7–1. Manual Backdating Changes

Instrument Serial Number	Make Manual Changes
2124G00129	1 to 32
118, 117, 116, 109 and lower	
2124G00140 and lower	2 to 32
2124G00160 and lower	3 to 32
2124G00194	4 to 32
189, 180, 176 and lower	
2124G00285 and lower	5 to 32
2124G00365 and lower	6 to 32
2124G00405 and lower	7 to 32
2124G00505 and lower	8 to 32
2124G00565 and lower	9 to 32
2124G00635 and lower	10 to 32
2124G00695 and lower	11 to 32
2124G00755 and lower	12 to 32
2124G01085 and lower	13 to 32
2124G01165 and lower	14 to 32
2124G01235 and lower	15 to 32
2124G01285 and lower	16 to 32
2124G01335 and lower	17 to 32
2124G01485 and lower	18 to 32
2124G01735 and lower	19 to 32
2124G01905 and lower	20 to 32
2124G01940 and lower	21 to 32
2124G02085 and lower	22 to 32
2124G02145 and lower	23 to 32
2334G02345 and lower	24 to 32
2334G02495 and lower	25 to 32
2334G02570 and lower	26 to 32
2334G02620 and lower	27 to 32
2334G02645 and lower	28 to 32
2334G02670 and lower	29 to 32
2334G02695 and lower	30 to 32
2334G02845 and lower	31 to 32
2334G02895 and lower	32

CHANGE 1

For serial numbers 2124G00129, 118, 117, 116, 109 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116–66501	VR200	DIO ZNR 5.11 V	5 %	1902–0041
		R226	R–F 1.62K	1 %	0757–0428
		R240	R–F 3.32K	1 %	0757–0433
		R243	R–F 2.05K	1 %	0698–4431
		R411	R–F 1.47K	1 %	0757–1094

CHANGE 2

For serial number 2124G00140 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:

A2	08116–66502	C4	C–F	47uF	50 V	0180–2984
		C10	C–F	47uF	50 V	0180–2984
		C11	C–F	47uF	50 V	0180–2984
		C16	C–F	47uF	50 V	0180–2984
A2	08116–66512	as above.				
A3	08116–66503	C6	C–F	47uF	50 V	0180–2984
		C8	C–F	47uF	50 V	0180–2984
A1	08116–66501	C406	C–F	100 pF		0160–4389
		C407	C–F	100 pF		0160–4389
		C525	C–F	4.7 pF		0160–3873
		C527	C–F	33 pF		0160–4386
		C532	C–F	22 pF		0160–3875
		R412	R–F	511		0698–7229
		R421	R–F	IK		0698–7236
		R557	R–F	56.2		0698–7206
		W1	Jumper			8159–0005
		W6	Jumper			8159–0005
		L506	Core mag			9170–0894
		L507	Core mag			9170–0894
		R228	R–F	11	1 %	0757–0378
		R103	R–F	511	1 %	0757–0416
		R309	R–F	51.1	1 %	0757–0394

CHANGE 3

For serial number 2124G00160 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116–66501	C501	C–F	0.1uF	20 %	0160–0576
		R157	R–F	5.36K	1 %	0698–3258
		R309	R–F	51.1K	1 %	0757–0394
MP9		PNL REAR				08116–60253

CHANGE 4

For serial number 2124G00194, 189, 180, 176 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116–66501	R528	R–F	825	1 %	0757–0421
		R529	R–F	825	1 %	0757–0421
		R541	R–F	825	1 %	0757–0421
		R542	R–F	825	1 %	0757–0421
		R513	R–F	8.25K	1 %	0698–7258
		R422	R–F	6.19K	1 %	0757–0290
		PC BD				08116–26501
A2	08116–66502	R49	R–V	2K	10 %	2100–0567
A2	08116–66512	as above				

4 a) Substitute the following information for existing **Adjustment Procedures.**
Pages affected: 5–7, 5–8, 5–9, 5–10 and 5–12.

4 b) Page 5–7 to read:

5–11 SHAPER

EQUIPMENT

Digital Voltmeter (RMS), LF Spectrum Analyser, Low Pass Filter as shown in figure 5–3.

PROCEDURE

1. Turn A1R413 fully CW
   Turn A1R418 fully CCW

Square Amplitude

2. Set 8116A:

MODE	NORM
FRQ	1.00 kHz
DTY	50 %
AMP	9.99 V
OFS	0.00 mV
OUTPUT	square, normal enabled

Set DVM: AC, 10 V Range

Connect 8116A output via 50 Ohm feedthrough to DVM.
Adjust A1R410 for 5.060 V ± 30 mV RMS

3. Set 8116A:

AMP	16.0 V

Check amplitude > 8.06 V (typ. 8.082 V).

4. Set 8116A:

AMP	1.00 V

Adjust A2 R49 for 0.506 V ± 3 mV RMS

Square Normal/Complement Balance

5. Set 8116A:

AMP	16.0 V
OFS	0.00 mV
OUTPUT	square, normal/complement as required, enabled

Set DVM: DC, 10 V Range.
Use DVM built in filter function, otherwise use set up as shown in figure 5–3.

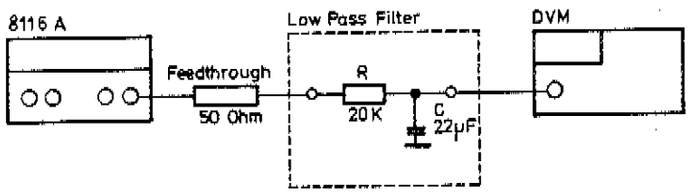


Figure 5–3. Low-pass filter test setup

Change 8116A output mode from normal to complement and back. Adjust A1R403 for minimum difference (< 5 mV) between normal and complement output mode.

4 c) Page 5–8 to read:

Triangle Amplitude

6. Set 8116A:

AMP . . . . . 9.99 V
OUTPUT . . . . . triangle, normal, enabled

Set DVM: AC, 10 V Range

Adjust A1R227 for 2.918 V ± 15 mV RMS

7. Set 8116A:

AMP . . . . . 16.0 V

Check that amplitude > 4.64 V

2nd Harmonic Distortion

8. Set 8116A:

FRQ . . . . . 3.00 kHz
AMP . . . . . 16.0 V
OUTPUT . . . . . sine, normal/complement as required enabled

Connect 8116A output via 50 Ohm (2 W) feedthrough to LF Spectrum Analyzer adjusting the input amplifier so that the fundamental equals 0 dB on display.

Preadjust A1R409 for minimum 3rd harmonic in normal mode. Adjust A1R417 for minimum 2nd harmonic in normal mode. Change 8116A from normal to complement mode and back. Adjust A1R407 for minimum difference between the 2nd harmonics in normal and complement mode.

Note: 2nd harmonic should be < –48 dB for both normal and complement modes.
Thedifference between normal and complement mode must not exceed 5 dB. To achieve this, alternating adjustment of A1R417 and A1R407 may be necessary.

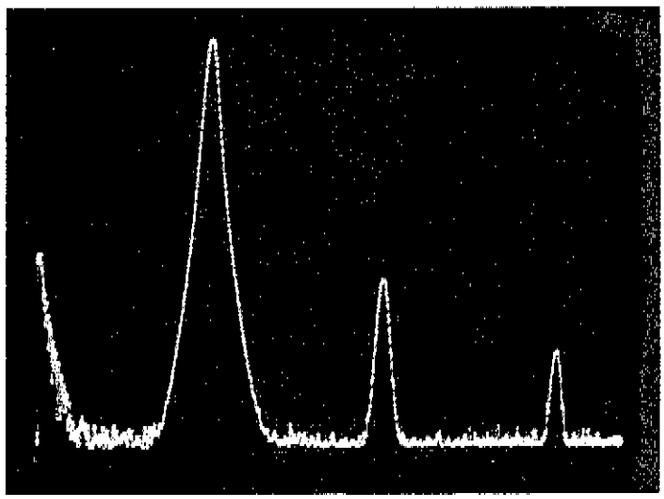


Figure 5–4. 2nd harmonic Distortion Adjust

Sine Normal/Complement balance

9. Set 8116A:

FRQ . . . . . 1.00 kHz
AMP . . . . . 16.00 V
OFS . . . . . 0.00 mV
OUTPUT . . . . . sine, normal/complement as required enabled

Set DVM: DC, 10 V Range

Connect 8116A output via 50 Ohm feedthrough to DVM. Use DVM built in filter function, otherwise use set-up as shown in figure 5–3.

Change 8116A output mode from normal to complement and back. Adjust A1R402 for minimum difference (< 5 mV) between normal and complement output mode

If the adjustment is not possible, change * value A1R439 (see table 5–1) and repeat the procedure from step 5.

Sine Amplitude/THD

10. Set 8116A:

FRQ . . . . . 1.00 kHz
AMP . . . . . 9.99 V

Set DVM: AC, 10 V Range

4 d) Page 5–9 to read:

Connect 8116A via 50 Ohm feedthrough to DVM.
Adjust A1 R418 for 3.532 V ± 10 mV RMS.

11. Set 8116A:

AMP . . . . . 1.00 V

Check that amplitude is 0.354 V ± 5 mV RMS.

12. Set 8116A:

FRQ . . . . . 3.00 kHz
AMP . . . . . 9.99 V
OUTPUT . . . . . normal

Connect 8116A output via 50 Ohm feedthrough to LF Spectrum Analyzer adjusting its input amplifier so that the fundamental equals 0 dB on display.
Adjust A1R409 for minimum 3rd harmonic.
It should be < −50 dB

13. Repeat steps 10 through 12 until values are within the given limits.

14. Set 8116A:

FRQ . . . . . 1.00 kHz
AMP . . . . . 16.0 V

Connect 8116A output via 50 Ohm feedthrough to DVM. Readjust A1 R418 for 5.660 V ± 3 mV RMS .

Triangle Normal/Complement Balance

15. Set 8116A:

FRQ . . . . . 1.00 kHz
AMP . . . . . 16.0 V
OFS . . . . . 0.00 mV
OUTPUT . . . . . triangle, normal/complement as required enabled

Set DVM: DC, 10 V Range

Connect 8116A output via 50 Ohm feedthrough to DVM, use built-in filter function, otherwise use set-up as shown in figure 5–3.

Change 8116A output mode from normal to complement and back. Adjust A1R401 for minimum difference (< 5 mV) between normal and complement output mode.
If adjustment is not possible, change * value A1R439 (see table 5–1) and repeat the procedure from step 5.

Sine Offset

16. Set 8116A:

AMP . . . . . 16.0 V
OFS . . . . . 0.00 mV
OUTPUT . . . . . sine, normal, enabled

Adjust A1R425 for 0.00 V ± 10 mV.

17. Set 8116A:

AMP . . . . . 1.00 V

Adjust A1R416 for 0.00 V ± 5 mV.

Square low Amplitude

18. Set 8116A:

AMP . . . . . 1.00 V
OFS . . . . . 0.00 mV
OUTPUT . . . . . square, normal, enabled

Set DVM: AC, 10 V Range

Connect 8116A output via 50 Ohm feedthrough to DVM
Check that amplitude is 0.510 V ± 5 mV RMS

THD Check

19. Set 8116A:

FRQ . . . . . 3.00 kHz
AMP . . . . . 1.00 V

Connect 8116A output via 50 Ohm feedthrough to LF Spectrum Analyzer and adjusting the input amplifier so that the fundamental equals 0 dB on display.

4 e) Page 5–10 to read:

Check that 2nd harmonic < –45 dB in both normal and complement modes.

20. Set 8116A;

FRQ . . . . . 50 MHz
AMP . . . . . 100 mV

Connect 8116A output to HF Spectrum Analyzer (50 Ohm feedthrough or termination) and adjust its input amplifier so that fundamental equals 0 dB on display.

Check that 2nd and 3rd harmonic < –27 dB in both normal and complement.

5–12 OFFSET

EQUIPMENT
Digital Voltmeter

PROCEDURE

1. Set 8116A:

MODE . . . . . NORM
FRQ . . . . . 1.00 kHz
DTY . . . . . 50 %
AMP . . . . . 100 mV
OFS . . . . . +7.95 V
OUTPUT . . . . . sine, normal, enabled

Set DVM: DC, 10 V Range

Connect 8116A output via 50 Ohm feedthrough to DVM. Use DVM built in filter function, otherwise use set-up shown in figure 5–3.
Adjust A2 R43 for +7.95 V ± 50 mV

2. Set 8116A:

OFS . . . . . –7.95 V

Check that offset equals –7.95 V ± 50 mV.

3. Set 8116A:

AMP . . . . . 10.0 mV
OFS . . . . . 795 mV

Check that offset equals 795 mV ± 4 mV.

4 f) Page 5–12 to read:

7. Verify that envelope distortion < 40 dB. All harmonics of the sideband should be at least 42 dB lower than the modulation sidebands.

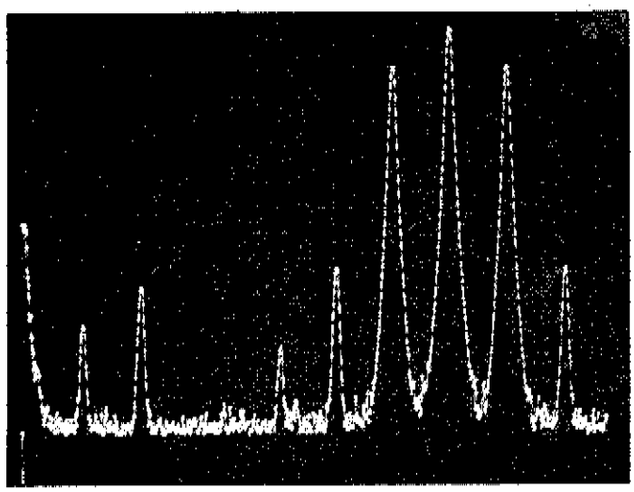


Figure 5–8. AM Envelope Distortion

8. Recheck and, if necessary, readjust steps 9, 10/11 and 15 of paragraph 5–11 SHAPER.

9. Verify again step 7.

CHANGE 5

For serial numbers 2124G00285 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116–66511	C216	C–F	15pF	200 V	0160–4385
		R226	R–F	2.15K	1 %	0698–0084
DELETE		R70	R–F	150	1 %	0757–0284
		R71	R–F	150	1 %	0757–0284
		R72	R–F	150	1 %	0757–0284

CHANGE 6

For serial number 2124G00365 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:

A3	08116–66503	DELETE C9 C–F 0.1uF 20 %				0160–0567
MP2		SHAFT PWR SW				08112–43701
A1	08116–66511	Q400	XSTR SEL PAIR			5180–2409
		R208	R–F	196	1 %	0689–7219
		R206	R–F	100	1 %	0689–7212
		MP COVER TRANS				0340–0530
		C401	C–F	4700pF	20 %	0160–0573
		R415	R–F	75	1 %	0689–7209
		R421	R–F	511	1 %	0689–7229
		R588	R–F	51.1	1 %	0689–7205
DELETE		R437	R–F	1.54K	1 %	0698–4425

CHANGE 7

For serial number 2124G00405 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:

A2	08116–66502	U24	IC LIN D/A CONV			1826–0874
		C31	C–F	0.1uF	20 %	0160–0576
		R30	R–F	3.83K	1 %	0698–3153
A2	08116–66512	as above.				
MP18		FRAME REAR				5020–8814
A1	08116–66511	U300 IC RATE				

CHANGE 8

For serial number 2124G00505 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116–66511	R157	R–F	4.75K	1 %	0757–0437
		R508	R–F	64.9K	1 %	0698–4502
A2	08116–66502	R45	R–F	4.22K	1 %	0698–3154
A2	08116–66512	as above				

CHANGE 9

For serial number 2124G00565 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:

A5	08116–66505	DS41	DISPLAY NUM			1990–0531
		DS42	DISPLAY NUM			1990–0531
		DS43	DISPLAY NUM			1990–0531
		DS40	DISPLAY			1990–0649
A5	08116–66515	as above.				
A1	08116–66511	R123	R–F	442	1 %	0698–3488
DELETE		R428	R–F	14.7K	1 %	0698–7264

CHANGE 10

For serial number 2124G00635 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116–66511	R220	R–F	2.37K	1 %	0698–3150
		R223	R–F	2.37K	1 %	0698–3150
		R242	R–F	1.1K	1 %	0757–0424
DELETE		C264	C–F	1nF 100 V		0160–3878

CHANGE 11

For serial number 2124G00695 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116–66511	RT1	THMS	5K		0837–0035
		R429	R–F	31.6K	1 %	0698–7272
DELETE		R235	R–F	IM	10 %	0698–4073
		R236	R–F	IM	10 %	0698–4073
		R237	R–F	IM	10 %	0698–4073
		R238	R–F	IM	10 %	0698–4073
		R239	R–F	IM	10 %	0698–4073
		U401	SHAP SEL AMP			5180–2416
		MP200	HEAT SINK			1205–0235
		C502	C–F	68pF	200 V	0160–4350

Make the following changes to schematic A3 08116–66503 (Service Block 3):

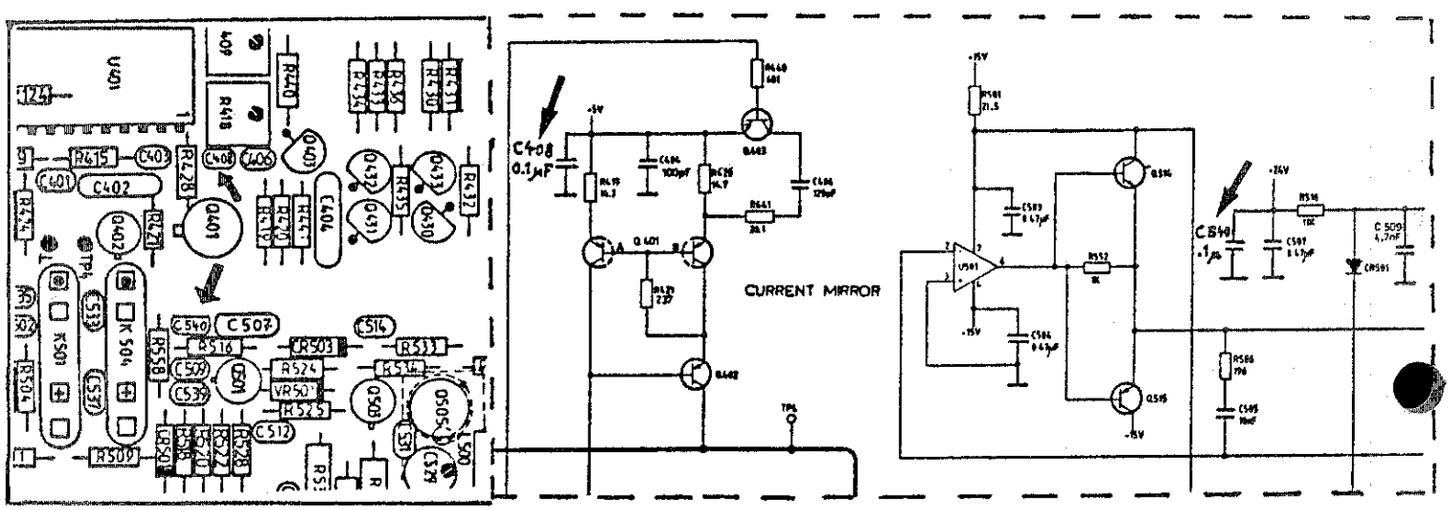
a) A3 U13 Pin 5 from EVMA to ground
b) A3 U13 Pin 7 from +5 V to VMA
c) A3 U12 Pin 4, 5 from EVMA to ground
d) A3 U12 Pin 6 from +5 V to VMA

CHANGE 12

For serial number 2124G00755 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116–66511					
	ADD	C408	C–F	0.1uF	20 %	0160–0576
		C540	C–F	0.1uF	20 %	0160–0576

On Service Sheet 7, change A1 Board Assy Main 08116-66511 and the Component Locator as follows:



CHANGE 13

For serial numbers 2124G01085 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:

A2	08116–66502	VR2 DIO ZNR 5.6 V	1902–0952
A2	08116–66512	as above	

CHANGE 14

For serial numbers 2124G01185 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116–66511	F1/F2 Fuse .5A				2110–0297
		U401	IC SHAPER			1826–0923
		C502	C–F	68pF	200 V	0160–4350
		C527	C–F	68pF	200 V	0160–4350
		C525	C–F	1.5pF	200 V	0160–4381
		R553	R–F	2.7		0698–8369
A2	08116–66502	R-TRMR 5k 10 %				2100–3252
A2	08116–66512	as above				
A3	08116–66503					
	DELETE	U35	IC SN74LS04			1820–1199
	ADD	U35	IC SN74LS14N			1820–1416

CHANGE 15

For serial numbers 2124G01235 and lower.

15 a) Page 3–18, paragraph 3–64 to read:

3–64 The 8116A responds to program codes in the Data message in the order in which they are received. When programming, therefore, ensure that the first parameter setting in the string is compatible with the current settings.

e.g. Current Settings: HIL = 2 V
LOL = 0 V

Program settings: HIL = 4 V
LOL = 2.5 V

In the example, the new HIL setting should appear first in the string. If LOL is programmed first, the new value (2.5 V) is not compatible with the current HIL setting (2 V) and therefore not accepted, a 'service request' then being sent to the controller. More information on parameter programming sequence is given under 'Error Reporting'.

15 b) Page 3–22, paragraph 3–75 to read:

3–75 Service Request. Bit 7 of the HP-IB Status Byte is usually set in conjunction with any of bits 1–4 (error indicators). However, in the case of the TIMING ERROR indication (bit 1), the 'Service Request' message can be suppressed via the command "SR 0"

e.g. (HPL) wrt 716, "SR 0"
(BASIC) OUTPUT 716; "SR0"

This is particularly useful for character strings where more than one timing parameter is programmed. The reason is best explained by an example:

e.g. Current Settings: FRQ 500 Hz
WID 1 ms
Program Settings: FRQ 1 kHz
WID 0.5 ms

Immediately upon receiving the new frequency value (first position in string), the 8116A would set SRQ true if SRQ is active, because the new value is not compatible with the current width setting. By suppressing SRQ, both new settings for frequency and width are accepted by the 8116A without any interruption to program flow by SRQ.

Note: In the permanently stored mode/parameter settings in the 8116A's ROM's, 'SR' is set to '0'. Should these settings be called up as current settings, the service request function can be re-activated for timing errors by programming 'SR' to '1'

e.g. (HPL) wrt 716, "SR1"
(BASIC) OUTPUT 716; "SR 1"

15 c) Service Block 3. ROM Test. Signature Analyses to read as follows:

Pin No.	U5	U6	U7	U8	U9	U38
9	H66F	2790	I25A	9UF6	UU53	3I3C
10	24PF	7AUA	60H2	26F4	8F34	4UUP
11	HH90	047F	F63I	355U	70I2	46P0
13	50PH	CC4H	449C	C825	A6U5	8H90
14	I43P	U42C	I8UF	C8H6	8U8U	UP5F
15	96IF	5453	OP45	70U4	H204	7079
16	5U79	4U95	22FA	94P3	IAF7	3AA8
17	C92H	79FF	FF08	398I	77A3	UF58
24	P254	P254	P254	P254	P254	P254

15 d) Page 3–21, Table 3–3. Mode / Parameter Messages (cont'd)
ADD

MESSAGE	MNEMONICS ASCII CODE
Range	
Up	RU
Down	RD

CHANGE 16

For serial numbers 2124G01285 and lower.
In Table 6–3. Replaceable Parts, make the following changes to the parts lists as stated:
A1 08116–66511 R215 R–F 3.48k 1 % 0698–3152

CHANGE 17

For serial numbers 2124G01335 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116-66511	Q210	XSTR SI 2N3904				1854-0215
		R215	R-F	681	.125 W	1%	0757-0419
		R445	R-VAR	200 k		1%	2100-3213
		R447	R-F	23.7 k		1%	0698-3158
A2	08116-66502	R43	R-VAR	2 k	.5W	10%	2100-0567
A3	08116-66503	U5	ROM B				08116-10001
		U6	ROM A				08116-10002
		U7	ROM 9				08116-10003
		U8	ROM 8				08116-10004
		U9	ROM 7				08116-10005
		U38	ROM 6				08116-10006

Change the Signatures on the Signature Layout on Page 8-9 for the following:

08116-	10001	10002	10003	10004	10005	10006

Pin No	U5	U6	U7	U8	U9	U38
9	H66F	2790	125A	9UP6	UU53	313C
10	24PF	7AUA	60H2	26P4	8P34	4UUP
11	HH90	047F	P631	355U	7012	46P0
13	50PH	CC4H	449C	C825	A6U5	8H90
14	143P	U42C	18UF	C8H6	8U8U	UP5F
15	961F	5453	0P45	70U4	H204	7079
16	5U79	4U95	22FA	94P3	1AF7	3AA8
17	C92H	79FF	FF08	3981	77A3	UF58
24	P254	P254	P254	P254	P254	P254

ADD

A1	08116-66511	R448	R-VAR	500 k	10%	2100-0580

On page 5-8 / 5-9, change steps 10 and 14 to read:

Sine Amplitude / THD

10. Set 8116A:

FRQ	1.00 kHz
AMP	9.99 V

Set DVM: AC, 10 V range

Connect 8116A via 50 Ohm feedthrough to DVM.
Adjust A1R448 for 3.532 V % 1mV RMS.

ADD

If A1R448 is too sensitive to achieve optimum adjustment, turn A1R418 a little clockwise.

14. Set 8116A:

FRQ	1.00 kHz
AMP	16.0 V

Connect 8116A output via 50 Ohm feedthrough to DVM. Readjust A1R448 for 5.660 V %2 mV RMS.

CHANGE 18

For serial numbers 2124G01485 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116-66511	C221,222	C-F	.1 µF	CER	20%	0160-0576

DELETE

A1	08116-66511	CR513,514	DIODE	PWR	1kV	1A	1901-0732
		R561	R-F	3.16 k	.125 W	1%	0757-0279

Page 5-3, para 5-6 POWER SUPPLIES, change to read:

A1 -23 V A1R19 -23 V ± 50 mV

Page 8-18, delete diodes CR513, CR514 from Diagram 7 (near Output BNC).

Change all -24 V references in manual to -23 V.

CHANGE 19

For serial numbers 2124G01735 and lower.
In Table 6-3 Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116-66511	U200	IC-TL 074 ACN	1826-0600
A2	08116-66502	U5	IC-TL 074 ACN	1826-0600
A3	08116-66503	U5	ROM B	08116-10011
		U6	ROM A	08116-10012
		U7	ROM 9	08116-10013
		U8	ROM 8	08116-10014
		U9	ROM 7	08116-10015
		U38	ROM 6	08116-10016

Change the Signatures on the Signature Layout on Page 8-9 for the following:

08116-	11011	11012	11013	11014	11015	11016

Pin No	U5	U6	U7	U8	U9	U38
9	278A	P726	873U	A4P3	HHU5	55FU
10	6A4H	PPAC	4H66	AC35	001P	384F
11	4731	U658	H178	7H9P	FA3H	H52H
13	U9H8	H7A7	30A9	9H70	936H	PH16
14	6344	CP5F	459U	61U7	64PA	6517
15	PCC0	9P52	2F1A	3061	A738	01FC
16	8P11	A30C	9C95	FH3C	PC47	P77H
17	9A08	H5UU	3719	C0C9	C5CF	HCH4
24	P254	P254	P254	P254	P254	P254

CHANGE 20

For serial numbers 2124G01905 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

A2	08116-66502	R30	R-F	3.83 k	1%	0698-3153
		R33	R-F	4.87 k	1%	0698-4444
		VR2	DIODE ZNR 6.2 V			1902-0953

CHANGE 21

For serial numbers 2124G01940 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116-66511	C264	C-F	1 nF			0160-3878
		R123	R-F	402	.125 W	1 %	0698-4453

DELETE

A1	08116-66511	C235	C-F	39 pF	200 V	1 %	0160-4494
		R130	R-VAR	200	10 %		2100-3212

On page 5-1, Table 5-1 make the following addition:

Voltage Controlled Oscillator	A1R123	383 Ohm - 536 Ohm	Decrementing R123 value decreases HF Duty Cycle

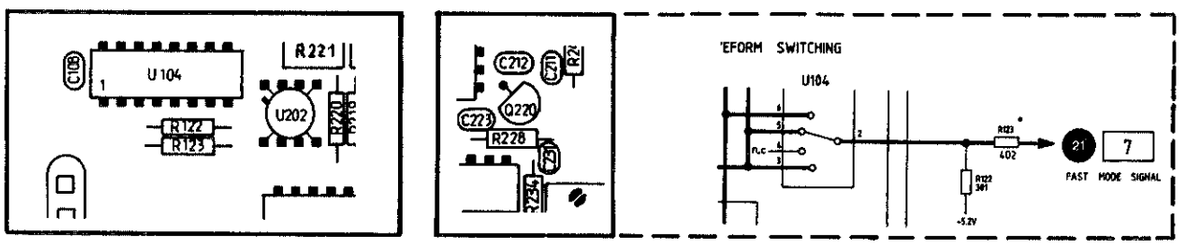
On page 5-6, change step 16 to read:

Set 8116:

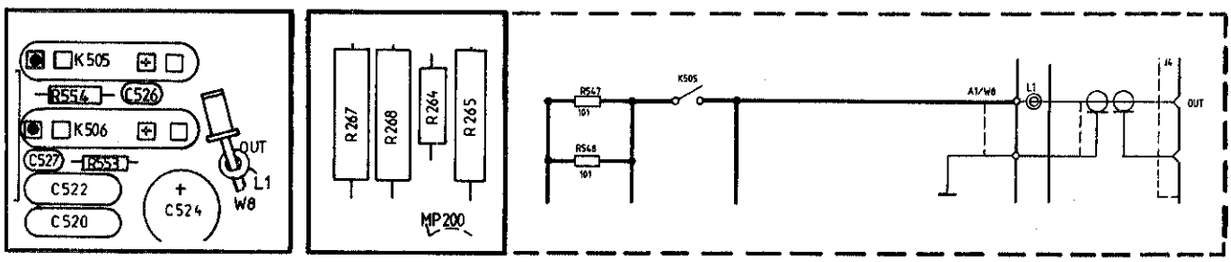
FRQ	10.0 MHz
OUTPUT	square, enabled

Check that Duty Cycle < 60 %. If not, change
value A1R123 (see table 5-1).

On page 8-16, change the Component Locator and Service sheet 6 to read:



On page 8-18, change the Component Locator and Service Sheet 7 to read:



ie. remove CR513 and CR514.

ie. remove C264.

Remove diodes CR513 and CR514 from Schematic 7 (vicinity of switch K505, Output BNC).

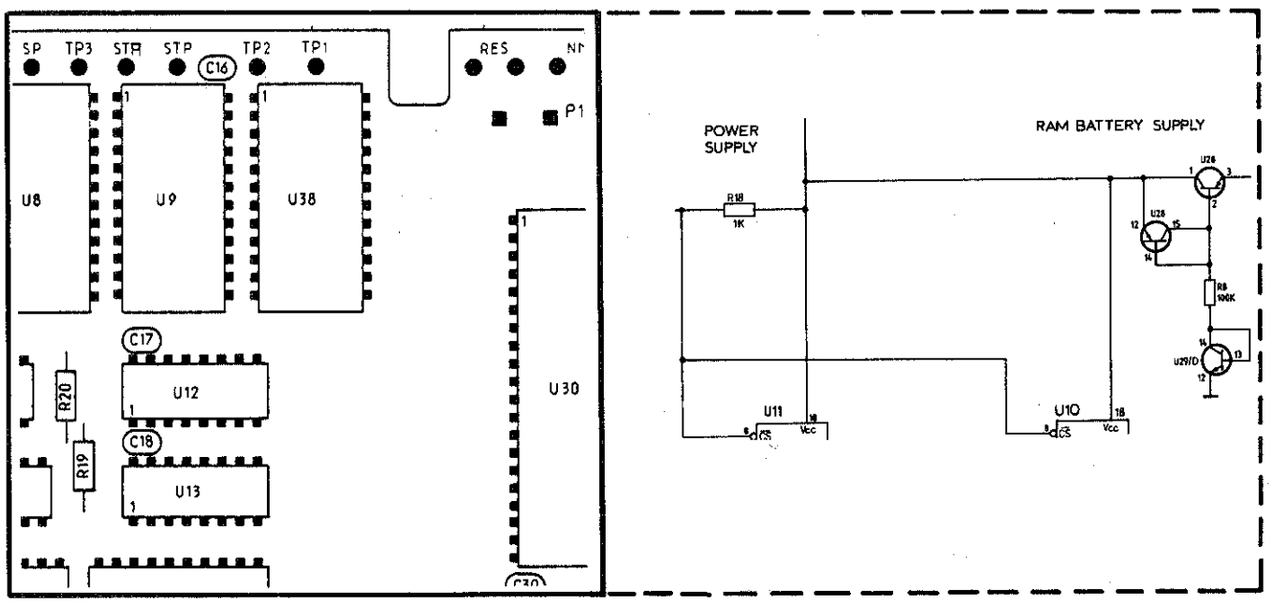
CHANGE 22

For serial numbers 2124G02085 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

DELETE

A3	08116-66503	TP5	TERM TEST POINT	0360-0535
		W2	JUMPER	8159-0005

On page 8-9, change the Component Locator and Service Sheet to read:



CHANGE 23

For serial numbers 2124G02145 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

A3	08116-66503	R15	R-NETWORK	47 k	1810-0378

CHANGE 24

For serial numbers 2334G02345 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

ADD

A2	08116-66502	C31	.1 *mF*	CER	20%	0160-0576

Perform the following changes:

A1	08116-66511	R404,408	R-F	261	.125 W	1 %	0698-3132
		R405,406	R-F	1.62 k		1 %	0757-0428
		C502	C-F	120 pF		5%	0160-4512
		C530	C-F	1 pF	200V		0160-4380
		C531	C-F	2.2 pF	200 V		0160-3872
		CR505,506	DIO SI	15 V	75 ns		1901-0179
		Q510,512	XSTR	NPN	2N3866A		1854-0784
		Q511,513	XSTR	PNP	2N5160		1853-0312

DELETE

A1	08116-66511	C541	C-F	.01 µF	100 V		0160-3879

ADD

A1	08116-66511	C525,538	C-F	1.5 pF	200 V		0160-4381
		C540	C-F	.1 µF		20 %	0160-0576
		L508,509,510,511		CORE MAGNETIC			9170-0894
		R556	R-F	237	.05 W	1 %	0698-7221

On page 8-10, in Component Locator, replace C541 with C538.

On page 8-18, Service Sheet 7 Schematic, remove C541 located between emitters of Q508 and Q509.

CHANGE 25

For serial numbers 2334G02495 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116-66511	R536	R-F	261	.05 W	1 %	0698-7222

CHANGE 26

For serial numbers 2334G02570 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116-66511	C105	C-F	.01 µF	CER	20 %	0160-0576
		C530	C-F	1 pF	200 V		0160-5380

DELETE

A1	08116-66511	C525 *	C-F	6.8 pF			0160-5738
		C538 *	C-F	1.5 pF			0160-4381
		R556 *	R-F	19.6			0698-7195

CHANGE 27

For serial numbers 2334G02620 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

ADD

A2	08116-66502	R70,71,72	R-F	150	.125	1 %	0757-0284

Perform the following change:

A3	08116-66503	U17	IC-SN74LS138	1820-0216

CHANGE 28

For serial numbers 2334G02645 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116-66511	C112,113	C-F	6.8 µF	35 V	TA	0180-0116

CHANGE 29

For serial numbers 2334G02670 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116-66511	R226	R-F	2.05 k	1 %	0698-4431

CHANGE 30

For serial numbers 2334G02695 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

A3	08116-66503	P1	WIRE FORM	1460-0579

CHANGE 31

For serial numbers 2334G02845 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

A1	08116-66511	C7,8,9,10	C-F	47 µF	50 V	20 %	0180-2984

CHANGE 32

For serial numbers 2334G02895 and lower.
In Table 6-3. Replaceable Parts, make the following changes to the parts lists as stated:

A3	08116-66503	U5	ROM B	08116-10021
		U6	ROM A	08116-10022
		U7	ROM 9	08116-10023
		U8	ROM 8	08116-10024
		U9	ROM 7	08116-10025
		U38	ROM 6	08116-10026

Change the Signatures on the Signature Layout on Page 8-9 for the following:

08116-	100021	100022	100023	100024	100025	100026

Pin No	U5	U6	U7	U8	U9	U38
9	278A	P726	752H	1P19	HHU5	55FU
10	6A4H	PPAC	2537	AC35	001P	384F
11	4731	U658	6064	P764	FA3H	H52H
13	U9H8	H7A7	431U	9H70	936H	PH16
14	6344	CP5P	9415	61U7	64PA	6517
15	PCC0	9P52	1F93	3061	A738	01FC
16	8P11	A30C	0059	FH3C	PC47	P77H
17	9A08	H5UU	8H81	C0C9	C5CF	HCH4
24	P254	P254	P254	P254	P254	P254

SECTION VIII
SERVICE

8–1 INTRODUCTION

8–2 This section contains the information to service the HP Model 8116A. The information includes theory of operation, troubleshooting, schematics, component layouts and block diagram.

8–3 The schematics and component layouts are organized as 'Service Sheets' which are identified by a large number within a square in the lower corners. A table relating these Service Sheets to board assemblies is given in Table 8–1. Schematic diagram symbols are given in Table 8–3.

Table 8–1. Index of Assemblies

Assembly	Service Sheet
A1 Main Board	2, 6, 7
A2 (A12) Control Board	5, 8
A3 Microprocessor Board	3, 4
A4 (A14) Keyboard	4
A5 (A15) Display Board	4

NOTE: The numbers given in brackets e.g. (A12) refer to the boards as used in Option 001 (Burst) instruments where they differ from the standard type.

8–4 SAFETY CONSIDERATIONS

8–5 This section contains warnings and cautions that must be followed for your protection and to avoid damage to the equipment:

WARNING

Maintenance described herein is performed with power supplied to the instrument, and protective covers removed. Such maintenance should be performed only by service-trained personnel who are aware of the hazards involved (for example, fire and electrical shock). Where maintenance can be performed without power applied, the power should be removed.
When servicing is complete, the After Service Safety Check must be performed.

8–6 AFTER SERVICE SAFETY CHECK

8–7 Execute the following checks when servicing is completed.

8–8 Disconnect power cord from line. Visually inspect interior of instrument for any sign of abnormal internally generated heat, such as discolored printed circuit boards or components, damaged insulation, or evidence of arcing. Determine cause and remedy.

8–9 Check cabinet/ground pin continuity in accordance with IEC/VDE. Flex the power cord while making the measurement to detect any intermittent discontinuity. Check internal ground connections on boards and frame. Also check resistance of any front or rear panel ground terminals marked ⏚ .

8–10 Check cabinet/line isolation in accordance with IEC/VDE. Replace any component which results in a failure or refer to production Memo or Service Note issued by product division for alternate action.

8–11 Check line fuse to verify that the proper value is installed.

8–12 Check that safety covers are installed.

8–13 Check that the coaxial and flat cables are properly connected. Check that all boards are properly fitted and the heatsink connections between the Output board A8 and front frame member are secure.

8–14 Inform Hewlett-Packard (internally, the responsible product division) of any repeated failures in the above tests or any other safety features.

8–15 SERVICE BLOCKS (THEORY/ TROUBLESHOOTING)

8–16 The theory of operation and troubleshooting is divided into Service Blocks, each Service Block corresponding to a complete function within the 8116A, except Service Block 1 which deals with overall instrument troubleshooting, including a detailed block diagram of all HP 8116A functions. The purpose of the general instrument troubleshooting is to provide a fast means of isolating a fault down to a function. The Serviceman should then proceed to the Service Block providing detailed theory of operation and troubleshooting hints

for that function. A table relating function to Service Block is given in Table 8–2.

Table 8–2. Index to Service Blocks

Service Block	Functions
1	Overview and Troubleshooting Guide
2	Power Supply
3	Microprocessor
4	Device Bus Control, Keyboard and Display Board
5	Control
6	VCO and Width Generation
7	Shaper and Output Amplifier
8	(OPT. 001) Burst, Sweep and Hold

8–17 Tables and Figures within each Service Block are given three-digit codes e.g. Figure 8–3–1. The first digit refers to the Manual Section (8), the second digit to the Service Block and the third to the Figure number, e.g. Figure 8–3–1 means Section 8, Service Block 3, Figure 1.

8–18 IC INFORMATION

8–19 Information on the three Hewlett-Packard Integrated Circuits used in the 8116A is given in Figures 8–1, 8–2 and 8–3. Detailed functional information is to be found in the Theory of Operation for each of the Service Blocks in which they appear.

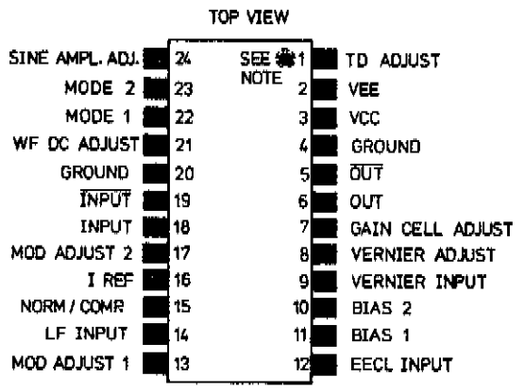


Figure 8-1 SHAPER I.C.

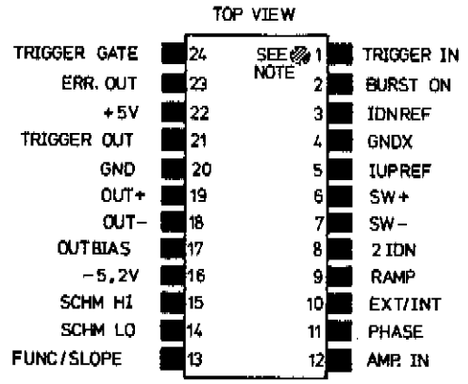


Figure 8-2 SLOPE I.C.

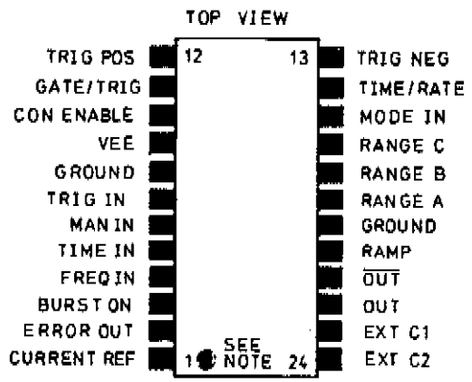


Figure 8-3 TIMING I.C.

Table 8–3. Schematic Diagram Notes (1 of 2)

The following symbols conform, as far as possible, with ANSI Y 32.2, IEEE No. 315 and ANSI Y32.14 (for the logic symbols). These standards should be consulted when further informations is required.

General

Units — Resistance values are in ohms, capacitance values in microfarads and inductance values in microhenries unless otherwise noted !

P/O — Part of

Asterisk denotes a factory selected value. The value shown is the nominal value.

Encloses front panel nomenclature.

Encloses rear panel nomenclature.

Heavy line indicates signal path.

Heavy dashed line indicates primary feedback path.

947 — Wire colour code. Same as resistor colour code. First number is wire body colour.

Wire or plug used as link.

Test point in a circuit. Point may/may not be identified on P.C. board.

Used with trimmer potentiometers or capacitors to indicate screwdriver adjustment.

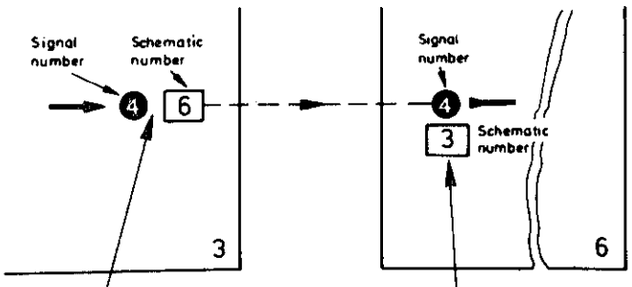
Direct connection to earth.

Ground connection to instrument chassis or frame.

Used when a number of common-return connections are at the same potential. If there is more than one such system in the same circuit, numbers are written in the triangles so that all connections with the same potential have the same number.

xV — Specific potential difference with respect to a potential reference level, eg. +10 V

Schematic Referencing



These references on a signal leaving a schematic diagram indicate the signal destination. The circle contains the signal number and the square contains the number of the schematic to which that signal goes.

These references on a signal entering a schematic diagram indicate the signal origin. The circle contains the signal number and the square contains the number of the schematic to which that signal originates.

Components

Normally open toggle switch. Circles (O) are used for the contacts to indicate a locking type switch.

Spring return, 2-position transfer switch. Triangle (▲) are used for the contacts to indicate a non-locking type switch.

2-position, 2-pole slide switch.

Air cored inductor.

Air cored transformer. The dot (●) is used, when necessary, to indicate instantaneous polarity.

Iron core

Ferrite core

bead — Ferrite bead

Varactor diode

Multi-junction diode

Diode

Zener diode

Schottky diode

Light Emitting Diode (LED)

Photodiode

Fuse

Neon

Filament lamp

SERVICE BLOCK 1

OVERVIEW AND TROUBLESHOOTING GUIDE

General

The purpose of this Service Block is to provide a brief overview of instrument functions, thus enabling the technician to quickly isolate faults to specific areas in order to perform effective troubleshooting.
Service Blocks II to VIII deal with instrument functions in depth — each Block containing operational theory and a comprehensive troubleshooting guide.
Service Block titles and the functions covered in each are as follows:

SERVICE BLOCK II Power Supply	Rectification, Regulation, Voltage and Current sensing and Power-Down detection.
SERVICE BLOCK III Microprocessor	Microprocessor Unit, ROM's, RAM's, HP-IB interfacing, Address decoding, RESET circuits and RAM battery supply.
SERVICE BLOCK IV Device Bus Control, Keyboard and Display Boards	Control board Address decoding, Key Scanner Bus, Display Driver, Keyboard assembly and Display board assembly.
SERVICE BLOCK V Control	Byte Offset latches and Offset DAC, Timer, Address decoding, Reference circuit, DAC's and Width Vernier current source.
SERVICE BLOCK VI VCO and Width Generation	Trigger Input circuits, Control Input circuits, Slope Generator IC, Timing IC and Error Feedback and Vernier Feedback.
SERVICE BLOCK VII Shaper and Output Amplifier	Shaper IC, Amplitude Modulator, Current Mirror, Pre-Attenuator, Signal Output Amplifier, Output Attenuator and Trigger Output Amplifier.
SERVICE BLOCK VIII (Opt. 001) Burst, Sweep and Hold	Burst, Blocking flip-flop, X-output Generator, Marker Output and Hold Input.

Instrument Self-Test

At switch-on, the 8116A performs a self-test in order to ascertain that all circuits are functioning correctly. Should a fault be detected, an error message will be displayed automatically. Figure 8–1–2 is a flowchart designed to aid the technician in diagnosing the general area of any fault arising. In each case, a Service Block number is given alongside the error message. The technician should then turn to that Service Block to begin troubleshooting the fault. It may sometimes be necessary to refer to more than one Service Block in order to ascertain the location of the fault, but this will be uncommon and the operational theory will give hints on associated areas which may be at the root of the problem.

Description

Whether under HP-IB or Local (frontpanel) control, the microprocessor is responsible for all data processing in the instrument. It addresses ROM's to access stored data and RAM's for current operating data.
The main Data Bus provides a highway for information between the microprocessor (with associated memory) and two secondary buses.
The first of these secondary buses is the Latched Data Bus, which is the link between the microprocessor and all frontpanel functions. These are: All LED's, Range and Vernier rocker keys, Mode and Parameter keys and the Digital Display with associated Units LED's.
The second of the secondary buses is the Device Bus, which handles all Control Data. This is data which is passed to the various DAC's to select current outputs required by the three specially developed HP IC's and their support circuitry.

These are:

1. VCO (Slope Generator) IC. — used as a triangle waveform generator up to 50 MHz, with signal generation free-running, gated or triggered. This IC is also used as a Burst Generator for Option 001 instruments.

2. Timing IC. — used as a triggerable pulse width generator, trigger source for Internal Burst Mode and for Pulse Width Modulation when an external signal is applied to the Control input port at the instrument frontpanel.
3. Shaper IC. — used primarily as a linear pre-amplifier and triangle to sine converter.

to SHAPER TEST A

All three HP integrated circuits rely upon secondary circuitry for support in order to achieve their various objectives. Information in detail about these circuits is to be found in Service Blocks II to VIII.

Troubleshooting

Whenever an instrument fault is suspected, it is recommended that the 8116A be switched OFF and ON again. The self-test routine will then be executed with the result of any fault detection being represented by an error display on the instrument frontpanel.

Figure 8–1–2 is a flowchart describing the order in which tests are performed, the error codes displayed and information as to where the fault is likely to be found. It should be noted that, if a multiple fault occurs, the error code displayed will be relevant only to the first fault detected. On successful diagnosis and remedy of the displayed error cause, the instrument will display, after switch-on, the next error code if a fault still exists.

Preparing the instrument for Service.

1. Remove all four feet at the rear of the instrument by unscrewing the fastening screws.

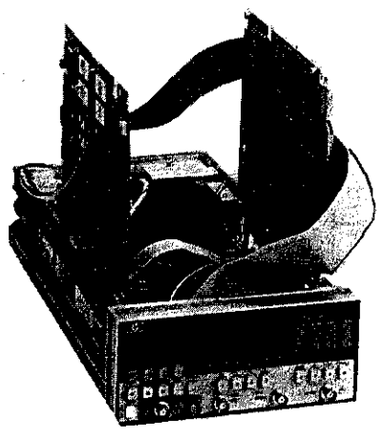
2. Remove the single screw securing the cover to the rear panel.

3. Slide the cover backwards to reveal the inside of the instrument.

4. To set the boards in the instrument to their Service positions, lift each carefully (individually) and stand in the vertical position by placing the cut-outs on the edge of the board over the locating lugs on the inside of the side panel.

   Board assy A2 (08116–66502 or 66512) control is positioned on the left when viewing the instrument from the front, with components facing outwards. Board assy A3 (08116–66503) should be located on the right.

Figure 8–1–3 shows the instrument in its Service position.



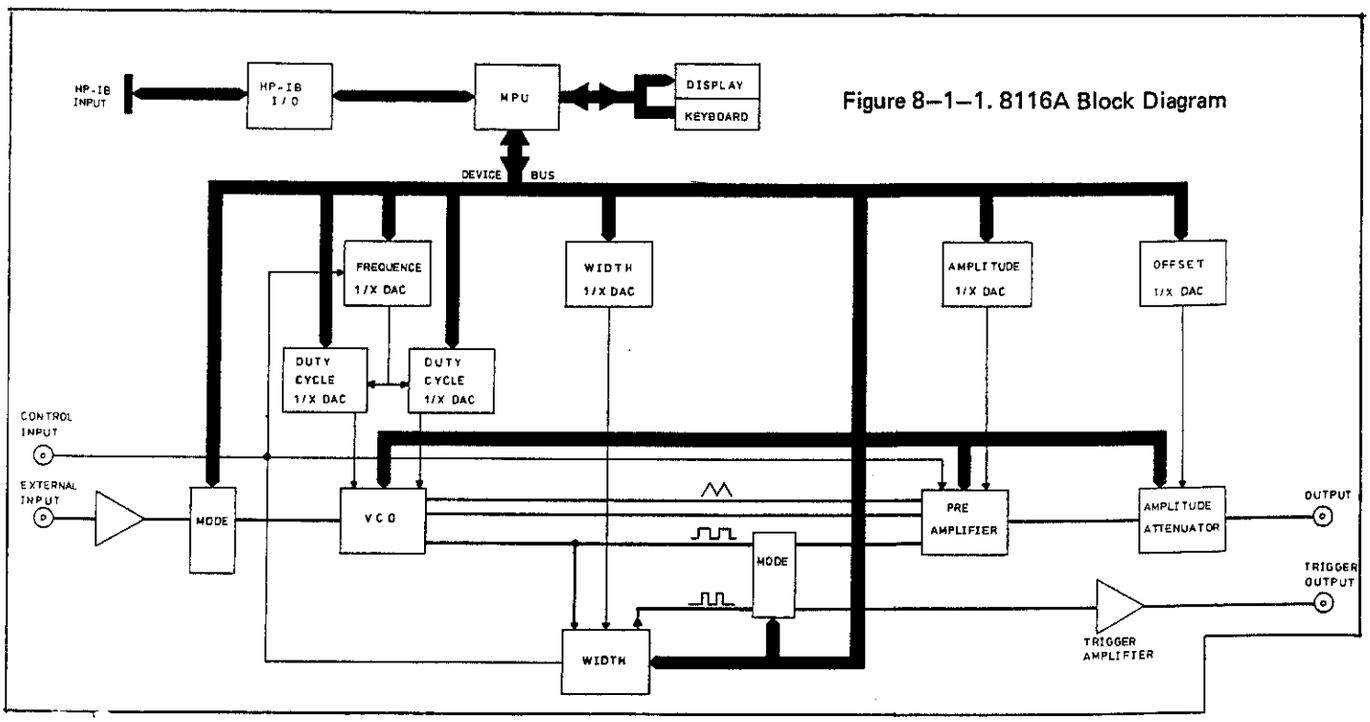
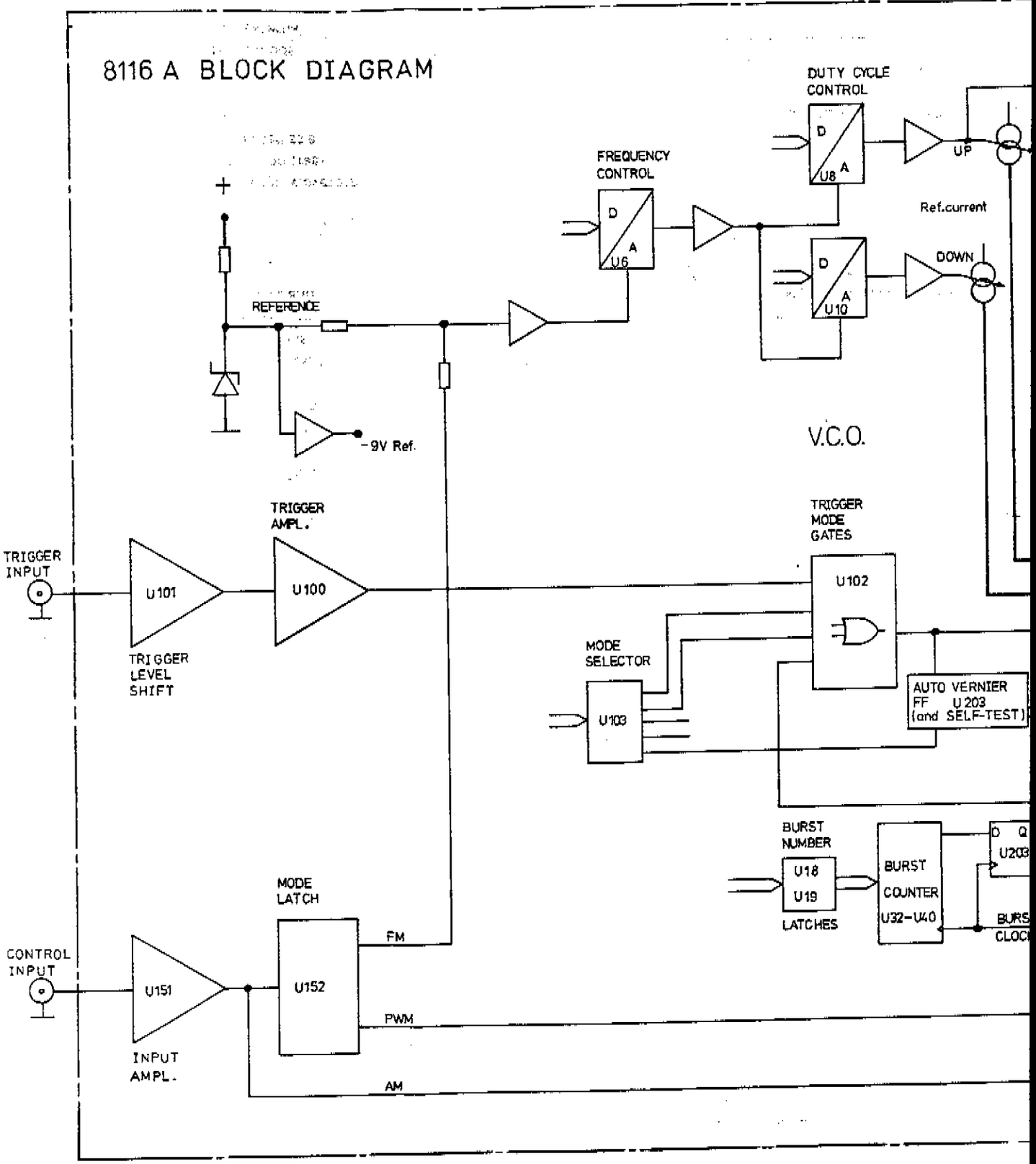
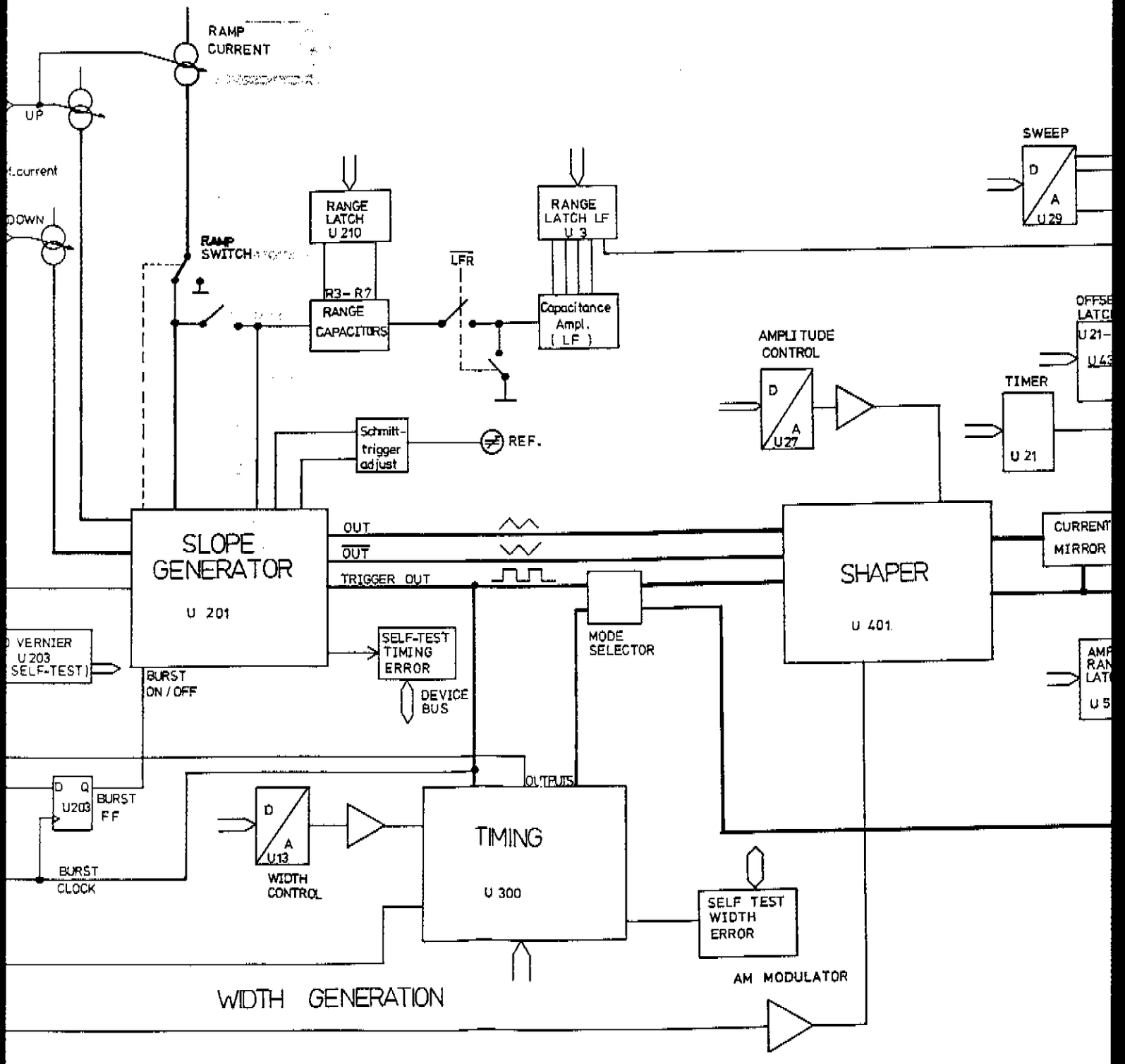


Figure 8–1–1. 8116A Block Diagram

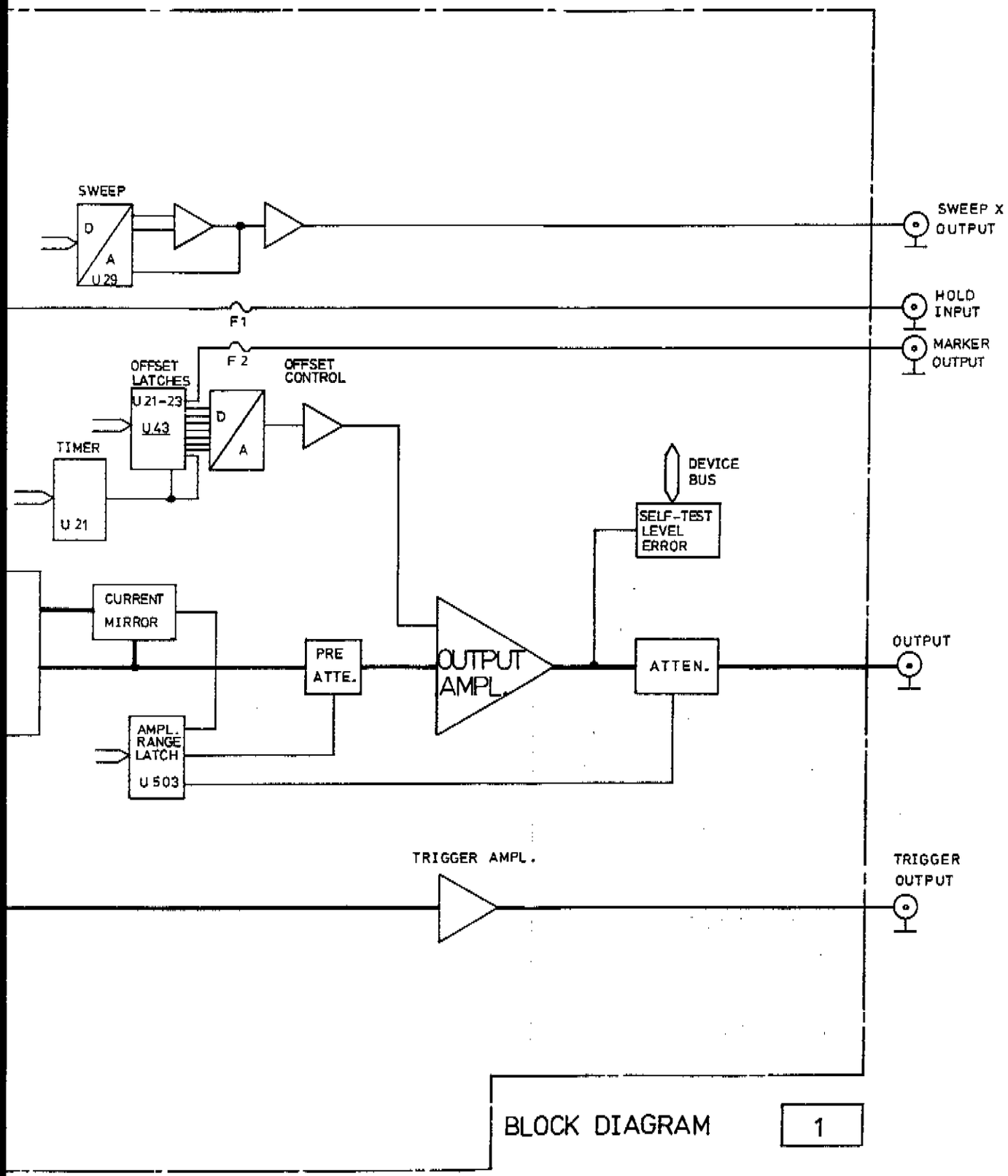
Block Diagram, Sht 1 of 3



Block Diagram, Sht 2 of 3



Block Diagram, Sht 3 of 3



BLOCK DIAGRAM 1

Fig. 8-1-2
Sht 1 of 4

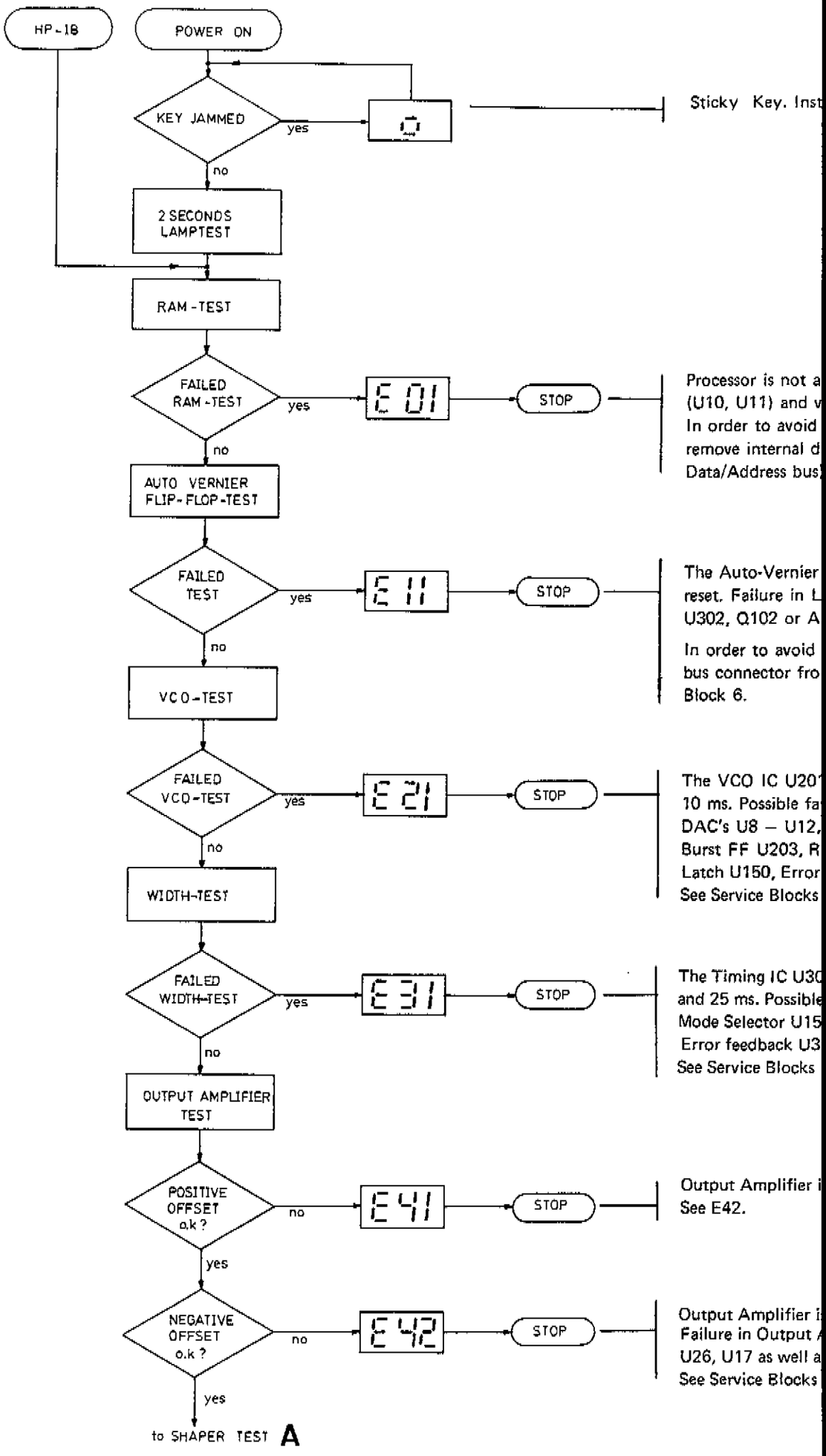


FIGURE 8-1-2.
8116A SELF-TEST
ROUTINE.

Fig. 8-1-2
Sht 2 of 4

Sticky Key. Instrument runs only when key is freed.

Processor is not able to load a test pattern into RAM's (U10, U11) and verify.
In order to avoid influence from Control or Main board remove internal device bus connector (Influence of Data/Address bus) see Service Block 3.

The Auto-Vernier FF (A1U203) can be neither set or reset. Failure in Latch U103, NOR Gate U102, Buffer U302, Q102 or A1 bd not connected.

In order to avoid control board error unplug device bus connector from A2 Control Board. See Service Block 6.

The VCO IC U201 is unable to supply a period of 10 ms. Possible fault: Frequency DAC U6, Duty cycle DAC's U8 – U12, Current Sources U200, Q200 – Q202, Burst FF U203, Reference voltage U200A, U202, U205, Latch U150, Error feedback U301, U302, Q303.
See Service Blocks 6, 5.

The Timing IC U300 is not able to generate pulses of 5 ms and 25 ms. Possible fault: Width DAC U13, U5, U17, Control Mode Selector U152. Slope Generator IC U201, Q220. Error feedback U301, U302, Q302.
See Service Blocks 6, 5.

Output Amplifier is unable to supply positive Offset.
See E42.

Output Amplifier is not able to supply negative Offset. Failure in Output Amplifier or Offset DAC A2 U24, U25, U26, U17 as well as Offset latches U21, U22, U23 and U43.
See Service Blocks 7. 5.

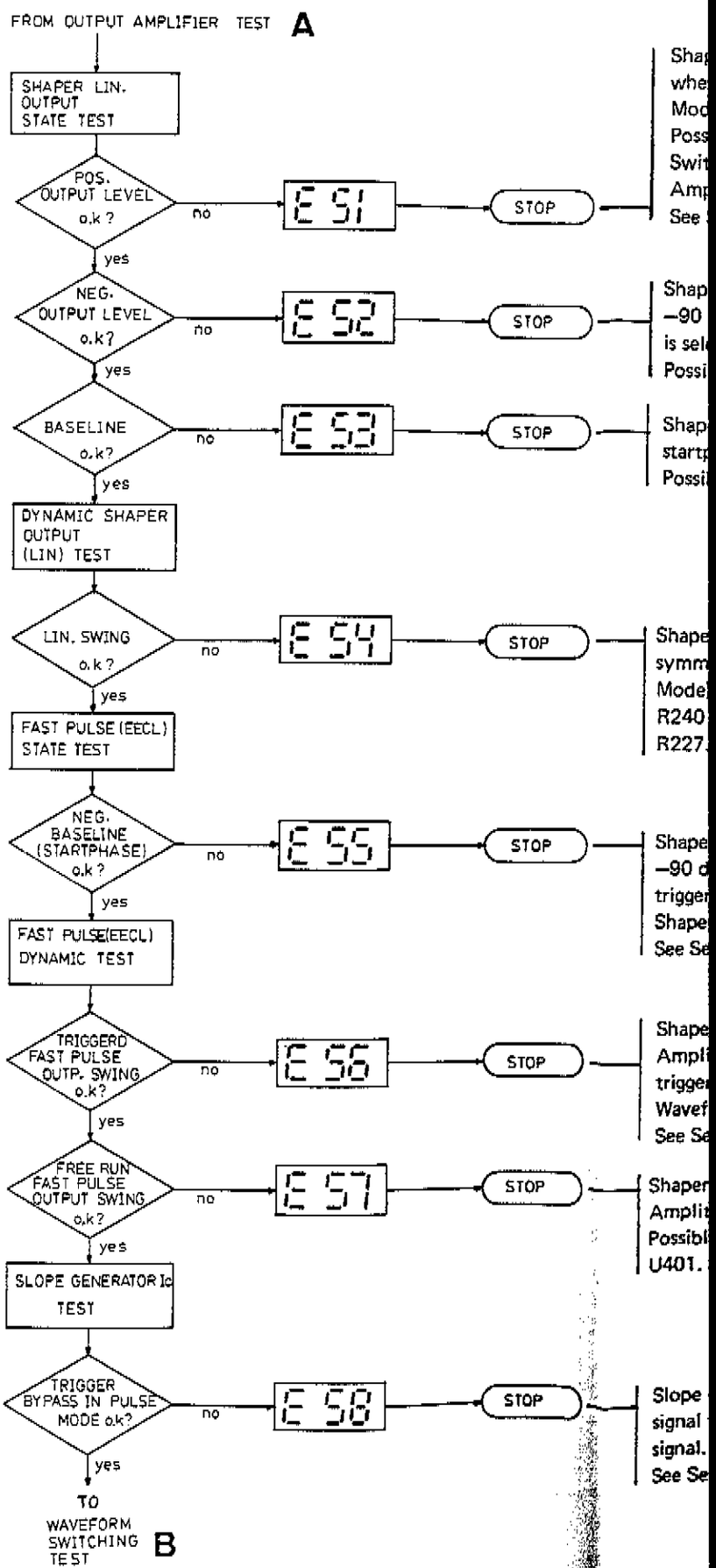


Fig 8-1-2, Skt 3 of 4

STOP — Shaper IC U401 is not able to supply positive Output when –90 degree startphase and Complement Output Mode is selected in triangle Mode (VCO not triggered). Possible failure in Slope Generator IC U201, Waveform Switching U104. Reference voltage switching U204, Amplitude DAC U27, U28, U17.
See Service Blocks 5, 6, 7.

STOP — Shaper IC U401 is not able to supply negative Output when –90 degree startphase in triangle Mode (VCO not triggered) is selected.
Possible failures: same as E51.

STOP — Shaper IC U401 supplies illegal offset when 0 degree startphase is selected (VCO not triggered).
Possible failures: same as E51.

STOP — Shaper IC U401 Output Signal is distorted and/or not symmetrical when Amplitude 15.2 V is selected (NORM Mode). Possible failure: Reference Voltage U200A, VR200, R240 to R242, U204. Slope Generator IC U201, R226, R227. See Service Blocks 6, 7.

STOP — Shaper IC U401 is not able to supply negative Output when –90 degree startphase in square Mode Selected (VCO not triggered). Possible failures: Waveform Switching U104, Shaper IC U401.
See Service Blocks 6, 7.

STOP — Shaper IC U401 is not able to supply squarewave when Amplitude 15.2 V is selected (TRIG Mode, square) and triggered. Possible failures: Trigger Slope U102, Latch U103, Waveform Switching U104, Shaper IC U401.
See Service Blocks 6, 7.

STOP — Shaper IC U401 is unable to supply a squarewave when Amplitude 15.2 V is selected (NORM Mode, square). Possible failures: Waveform Switching U104, Shaper IC U401. See Service Blocks 6, 7.

STOP — Slope Generator IC U201 can not pass the external Trigger signal to the Timing IC or Timing IC generates no output signal. Faulty U201 or faulty Timing IC U300, Q300.
See Service Block 6.

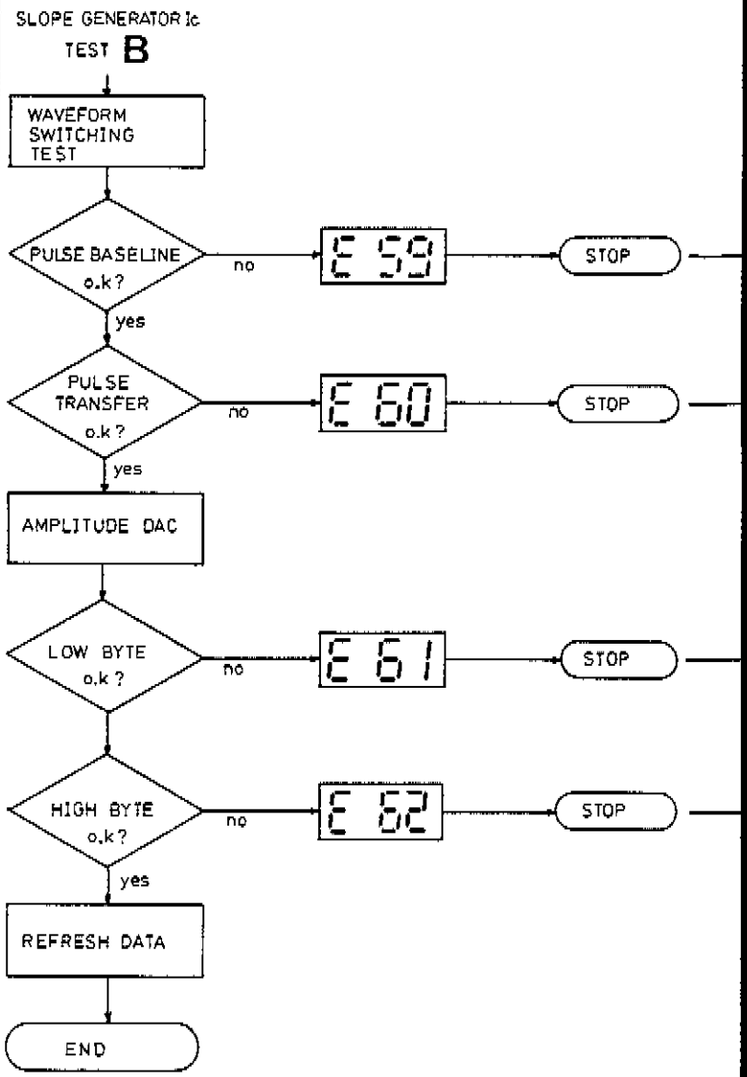


Fig. 8-1-2, Sht 4 of 4

STOP

Shaper IC U401 is not able to supply negative output when Pulse Mode is selected (not triggered). Possible failure: Waveform Switching U104, Timing IC U300, Q300.
See Service Block 6.

STOP

Shaper IC U401 is not able to supply pulses when Amplitude 15.2 V is selected in Pulse Mode (NORM Mode). Possible failure: waveform switching U104, Timing IC U300, Q300.
See Service Block 6.

STOP

Shaper IC U401 is unable to supply high positive output when Amplitude 9.19 V and Complement is selected in TRIG Mode at −90 degree startphase (not triggered). Possible fault: Amplitude DAC U27, U28, U17.
See Service Block 5.

STOP

Shaper IC U401 is not able to supply low positive output when Amplitude 1.51 V and Complement selected in TRIG Mode at −90 degree startphase (not triggered). Possible fault: Amplitude DAC U27, U28, U17.
See Service Block 5.

SERVICE BLOCK 2

POWER SUPPLY THEORY OF OPERATION

Introduction

The 8116A power supply unit occupies part of BD AY A1, and four sections, as follows:

1. Line voltage selector and transformer.
2. Bridge Rectifier circuits and regulators.
3. Voltage and current sensing circuits.
4. Power Down Detection.

1. Line voltage selection is accomplished by moving the two slider switches on the side panel of the instrument to the desired positions. The transformer provides six a.c. outputs and an earth line to the Bridge Rectifiers.

2. Bridge Rectifiers and Regulators.
   There are three rectifiers, all modular and therefore replaceable. CR1 provides +/— 5 V DC, CR2 provides +24 V DC and —23 V, and CR3 provides +/— 15 V DC. All raw supplies are smoothed by means of capacitors across the rectifier outputs (see Figure 8—2—1). The following supplies are fed to modular regulators, the output of each being adjustable by means of a potentiometer: +24 V (U3 and R18), —23 V (U4 and R19) +15 V (U5 and R24) and —15 V (U6 and R25).

A reference voltage of 6.2 V is derived from the +15 V regulated supply, using zener diode VR1 and R12. Comparators U1A and U1C perform current and voltage sensing tasks respectively.
U1C compares the output voltage with the reference voltage and drives the regulator transistor Q1 via driver transistor Q2 to zero difference.

When the current taken by the load through R2 becomes excessive, resulting in a distinct voltage drop across the resistor, the output of U1A (normally high) switches toward the negative supply of the device. This action forward-biases diode CR8. Q2 and, therefore, Q1 are effectively switched-off, and the 5.1 V supply is withdrawn.

The above principle of operation applies to the +5 V current sensor (U2D); and voltage regulator (U2C). It will be noted that op-amp U2A is used as an inverter with a gain of 1.04. However, the potential seen by the inverting input of comparator U2D will still be positive by virtue of the divider R28 (1K) and R6 (61.9K).

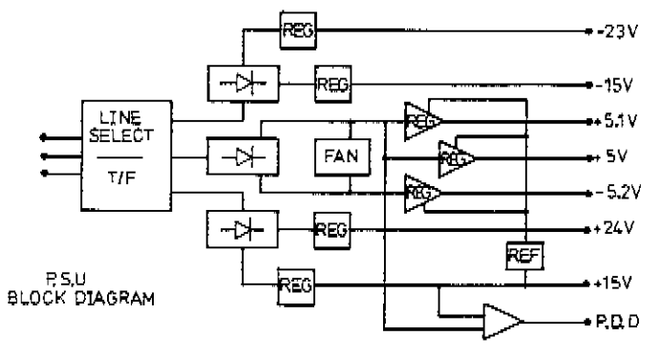


Figure 8—2—1. PSU block diagram

3. Voltage and current sensing circuits.
   The DC output of CR1, when smoothed, drives the instrument fan and provides the basis of the sensing circuits, the operation of which are described in the following text.

The —5.25 V current sensor (U1B) and voltage regulator (U1D) both adopt the same principle of operation as above, the exceptions being that the comparator output is normally of a negative status — going positive when a fault condition arises, and the reference voltage has to be negative (achieved by the inverter U2A).

4. Power Down Detection.

Power Down Detection is accomplished via comparator U2B, the output of which is normally negative due to the inverting input having a higher potential than the non-inverting input. When the instrument is turned off, the +5.1 V supply breaks down faster than the reference voltage due to the high load (uP.. etc..). This is detected by U2B, the output of which will switch towards the value of its positive supply, with the following consequences to the microprocessor board: To examine what happens when the Power Down Detect signal is sent, (instrument turn off), it is important to know the status of relevant circuits under normal operating conditions.

These are: uP bd assy A3, U27A output high, U29A on, Q1 on, thus supplying +5 Vcc to U10 and U11. U27B output low, U27C output high, enabling U29B feeding the RAM SELECT signal to the $\overline{CS}$ inputs of U10 and U11. The RAM Battery Supply is matched by Vcc and, therefore, the battery charges from the +5V supply.

U27B low output also switches U29C OFF, U27D output being high, thus ensuring that the $\overline{RESET}$ signal to the microprocessor U1) and HP-IB interface (U30) is in the false state (high).

Upon receipt of the Power Down Detect signal (positive voltage), the circuits on the microprocessor board respond as follows:

U27A output goes low, switching U29A and hence Q1 off. U27B output goes high ensuring that U27C output goes low, which turns U29B off. The +5 V (Vcc) supply has now been removed from U10 and U11, and the CS signal is in the false state (high). U27B output, now high, switches U29C on, causing U27D output to go low. Thus, the $\overline{RESET}$ signal to U1 and U30 assumes its true state (low), and both the microprocessor and HP-IB interface are inactive. Upon withdrawal of the +5 V (Vcc) supply by the action of Q1 being turned off, the battery to RAM current path is established, preventing U10 and U11 from actually being switched off. Thus the last set of data stored in the RAMs is retained.

At turn-on U27D output remains low until C4 is charged up via U12. As a result, the $\overline{RESET}$ signal (U27D output) goes high and initiates the restart sequence of the microprocessor.

Fig 8-2-2, Sht 1 of 4

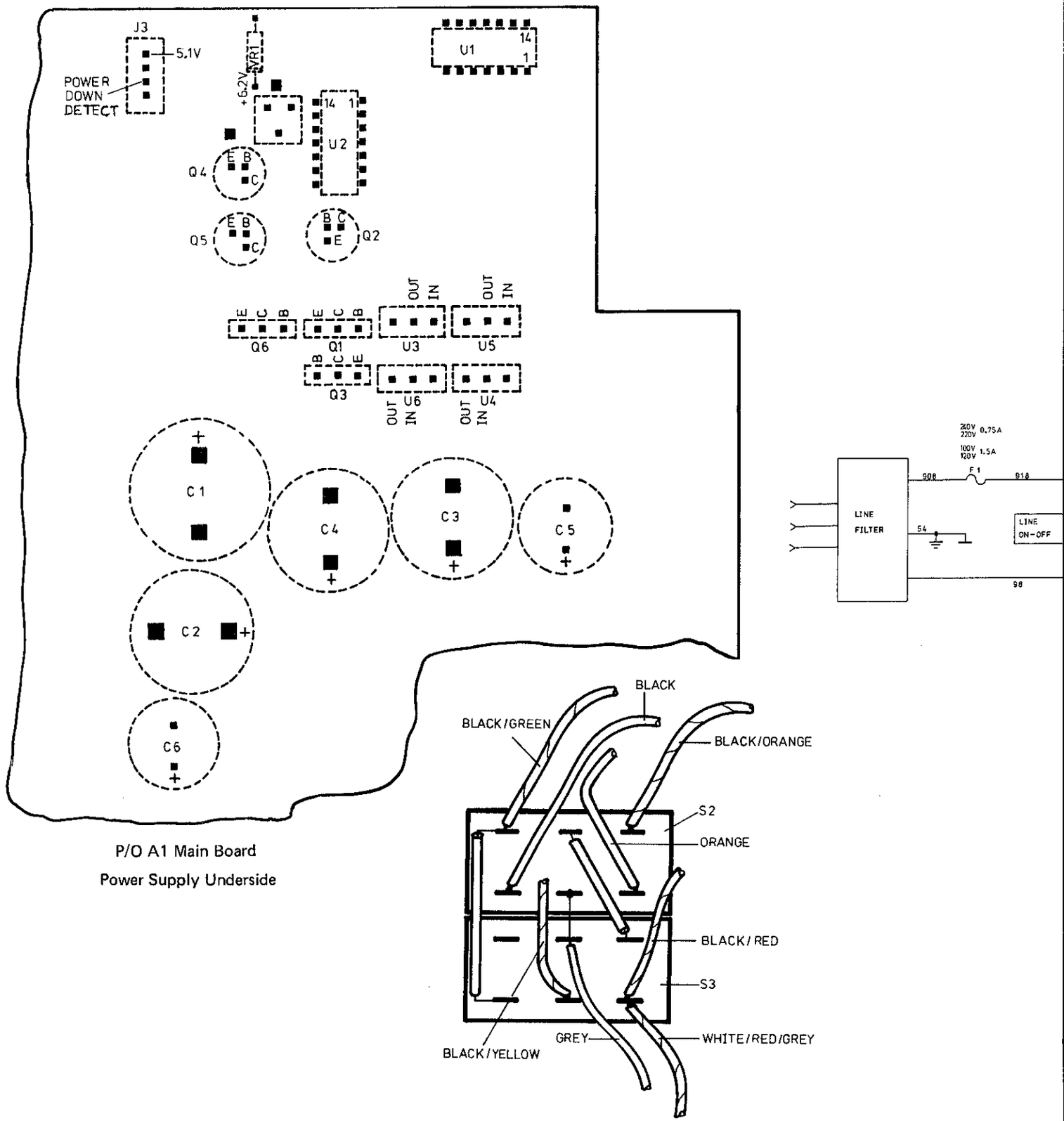


Figure 8–2–2. Line Voltage Selector S2, S3

Fig. 8-2-2, Sht 2 of 4

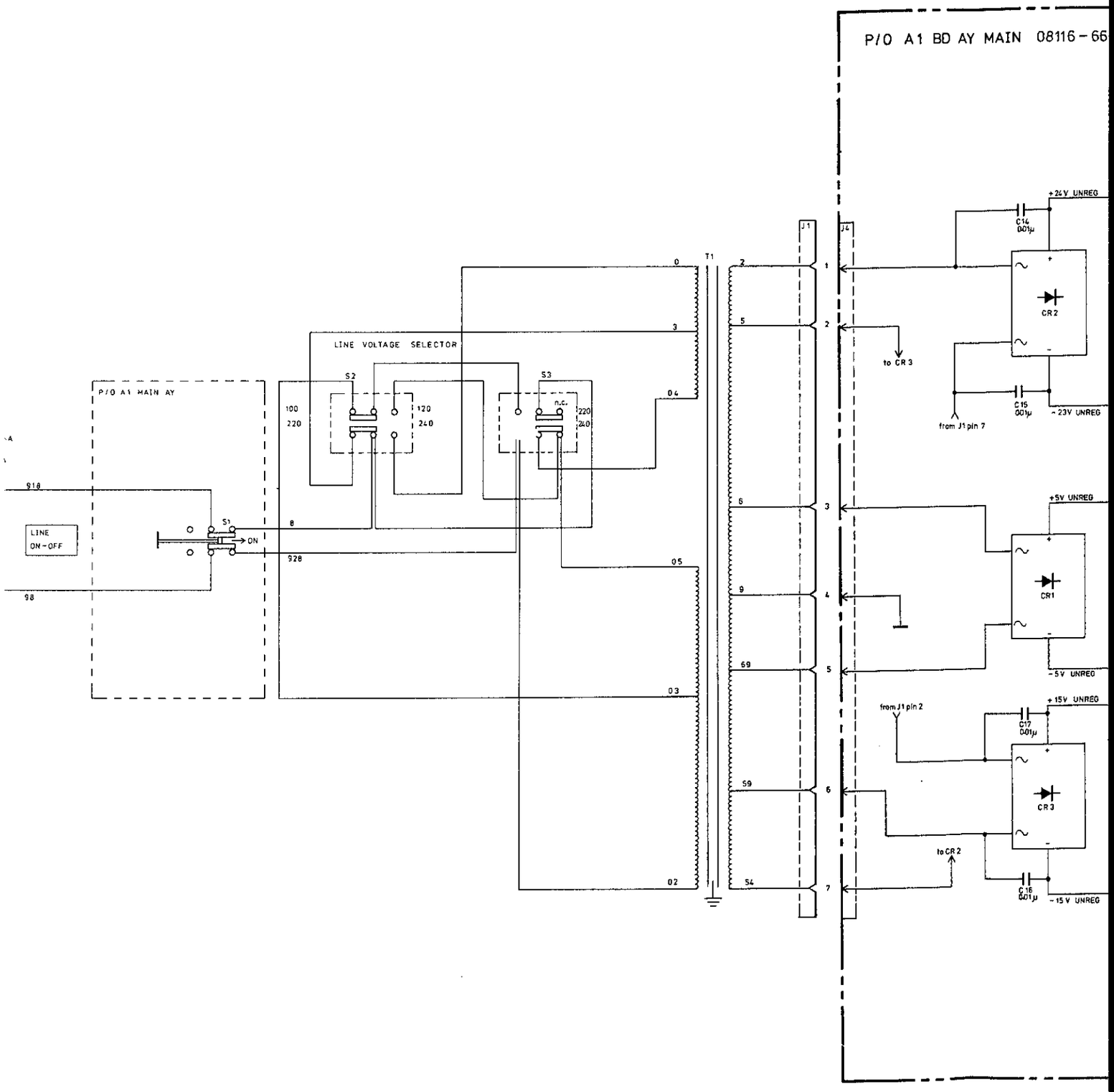


Fig 8-2-2, Sht 3 of 4

MAIN 08116-66511

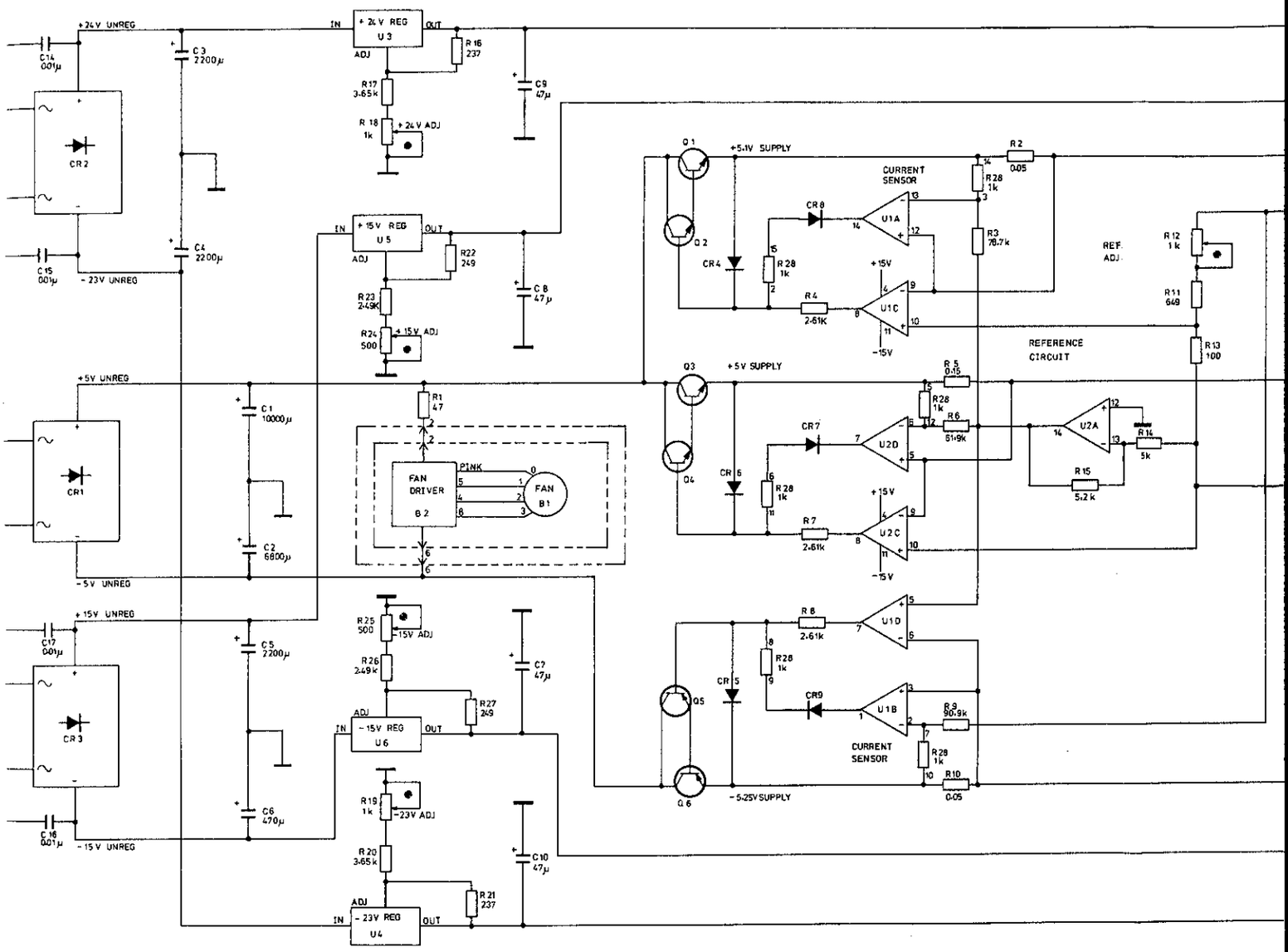
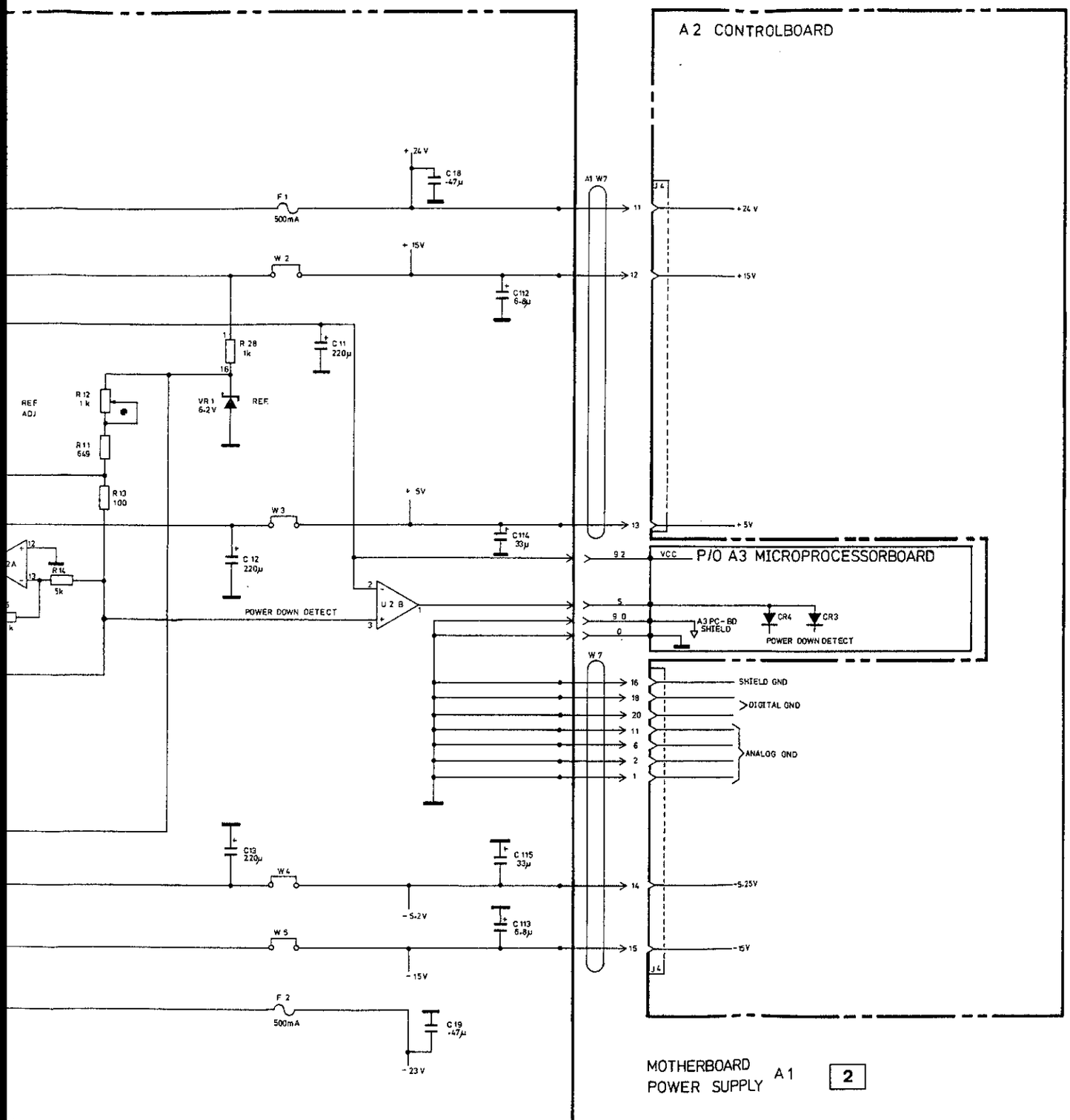


Fig. 8-2-2 Sht 4 of 4



8-7a

SERVICE BLOCK 2 TROUBLESHOOTING GUIDE

NOTE: If an error code is shown in the display it is necessary to press a key e.g. LCL, to set the u-Processor to normal routine, then troubleshoot the instrument.

To Troubleshoot the power supply, disconnect and remove A3 microprocessor board assy. Remove Power Supply Heat Sink assembly by unscrewing 2 screws (A).

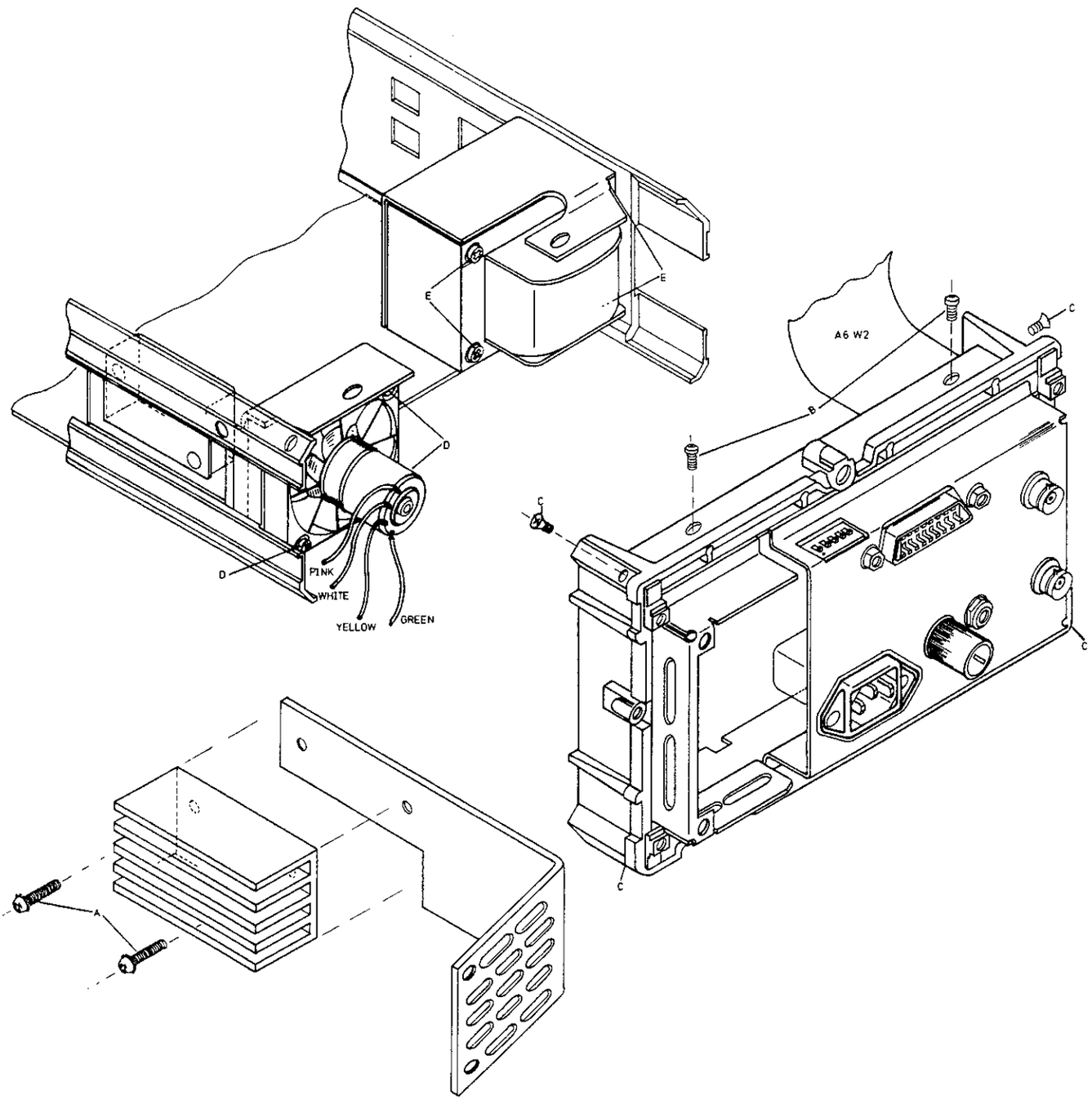


Figure 8–2–3. Exploded View (screws A, B, C, D, E, & F)

Fan and Transformer Removal Procedure

1. Turn instrument off and remove power cord
2. Remove A6W2 HP-IB Ribbon Cable
3. Remove 2 screws A mounting Heat Sink Assembly
4. Remove 4 screws B mounting Rear Frame to brackets
5. Remove 2 screws C mounting Rear Frame to brackets
6. Pull Rear Frame away and lay it on top of the instrument

After disconnecting the respective wires, unscrew the fan and remove the transformer.

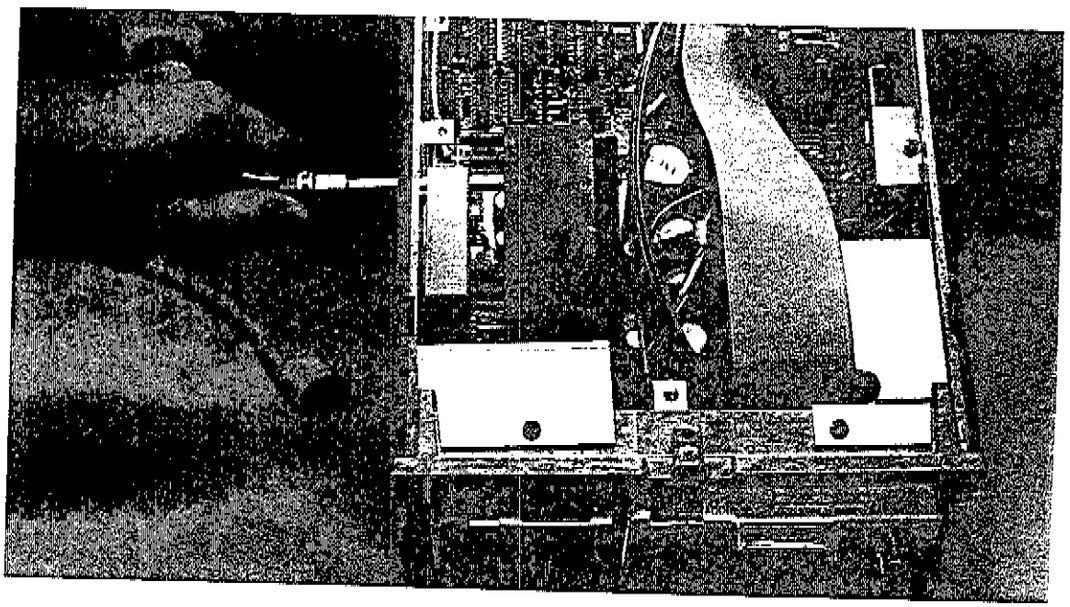


Figure 8–2–4. Power Supply Heat Sink Removal

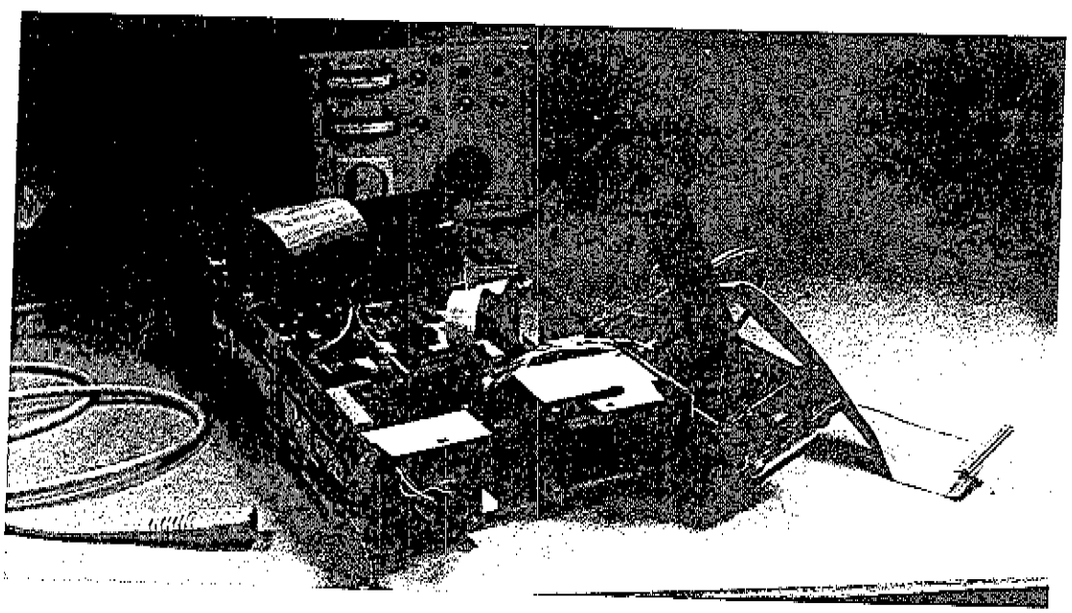
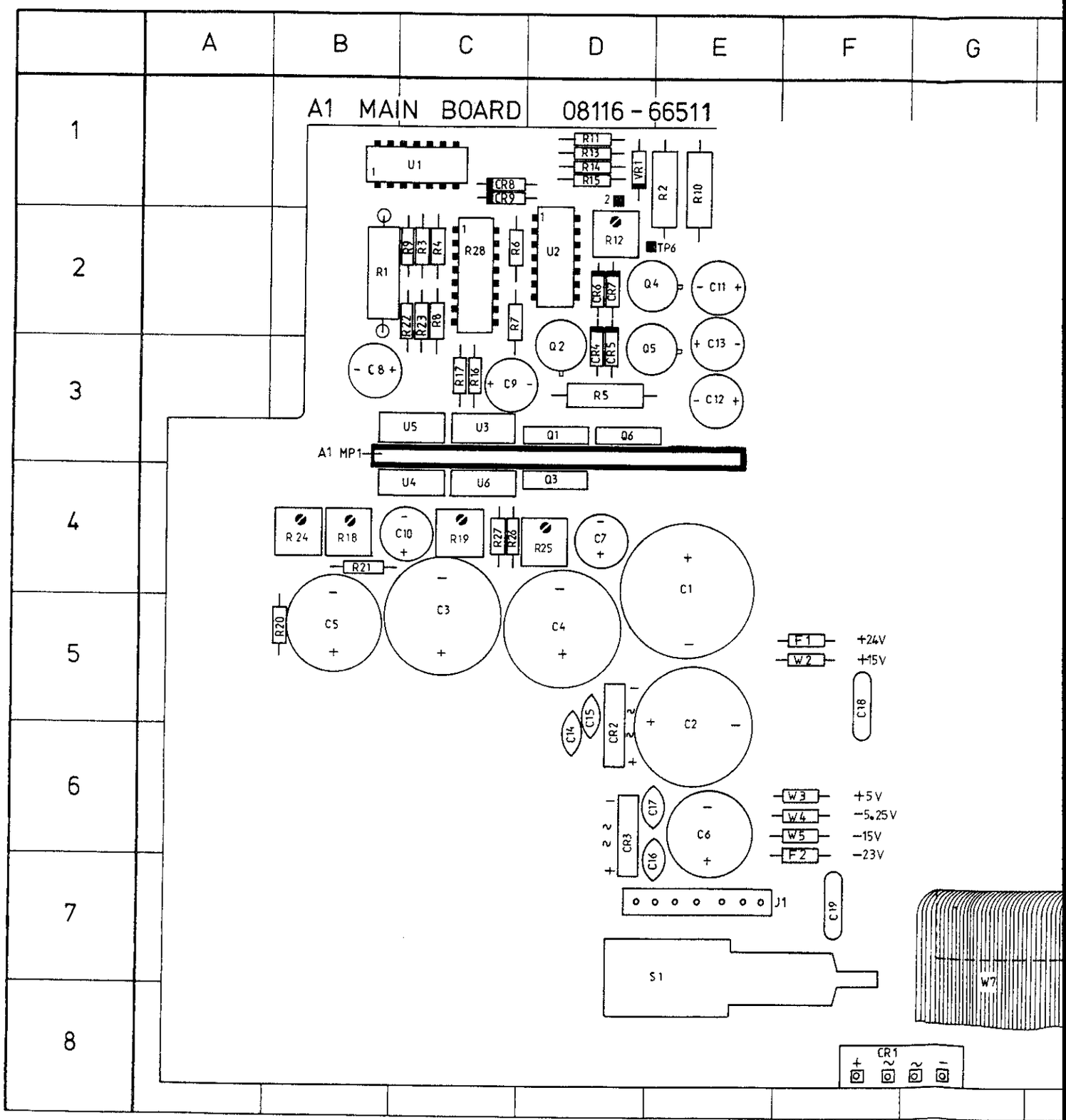


Figure 8–2–5. Removed Rear Frame

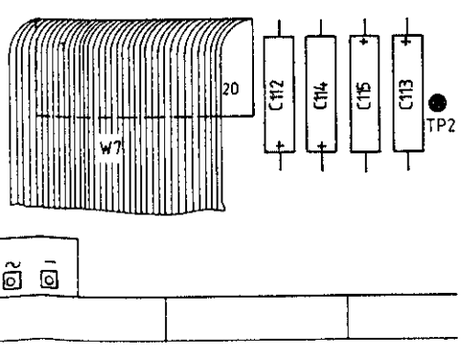
Power Supply, Sht 1 of 2



Power Supply, Sht 2 of 2

G	H	I

COMP	REF	COMP	REF
C1	E4	R1	B2
C2	E6	R2	E1
C3	C5	R3	C2
C4	D5	R4	C2
C5	B5	R5	D3
C6	E6	R6	C2
C7	D4	R7	C2
C8	B3	R8	C2
C9	C3	R9	C2
C10	C4	R10	E1
C11	E2	R11	D1
C12	E3	R12	D2
C13	E3	R13	D1
C14	D6	R14	D1
C15	D6	R15	D1
C16	E7	R16	C3
C17	E6	R17	C3
C18	F5	R18	B4
C19	F7	R19	C4
C112	H7	R20	B5
C113	I7	R21	B4
C114	H7	R22	C2
C115	I7	R23	C2
CR1	F8	R24	B4
CR2	D6	R25	D4
CR3	D6	R26	C4
CR4	D3	R27	C4
CR5	D3	R28	C2
CR6	D2	S1	E7
CR7	D2	U1	C1
CR8	C1	U2	D2
CR9	C1	U3	C3
F1	F5	U4	C4
F2	F7	U5	C3
J1	E7	U6	C3
Q1	D3	VR1	D1
Q2	D3	W2	F5
Q3	D4	W3	F6
Q4	D2	W4	F6
Q5	D3	W5	F6
Q6	D3	W7	G7



SERVICE BLOCK 3

MICROPROCESSOR BOARD THEORY OF OPERATION

Controller

The controller is the data processing and information center of the 8116A Programmable Pulse/Function Generator. The control information required by the instrument is generated here, depending on inputs from one of two sources.

a) Frontpanel inputs when under manual control.
b) HP-IB inputs when under remote control.

During operation, inputs from one of these sources program the desired output parameters.

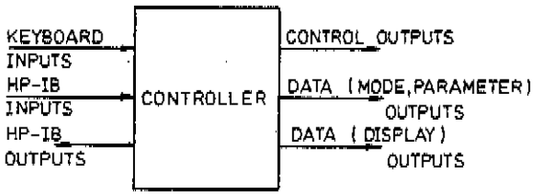


Figure 8–3–1. CPU input and output signals

These parameters are:

Frequency, Duty Cycle, Width, Amplitude, Offset, High Level, Low Level, Operating and control modes, Output and its associated functions such as Auto Vernier, Complement and Limit.

Additional parameters of the 8116A option 001 version are Start-, Stop-, Marker-Frequency, Sweep Time, Repetition Rate and Burst Number. When the instrument is in the remote control mode, all frontpanel keys with the exception of LCL are disabled (unless the Local Lockout command has been sent along the HP-IB-in which case, LCL is disabled too), and parameters can only be entered via the HP-IB.

The controller is comprised of the following major segments:

1. Microprocessor Unit (MPU)
2. Read Only Memory (ROM)
3. Random Access Memory (RAM)
4. HP-IB Interface (GPIA)
5. Address Decoder
6. $\overline{\text{RESET}}$-Circuit
7. RAM Battery Supply

The purpose of the MPU is to execute the functions (routines) programmed into the ROM array. Figure 8–3–1 indicates the input and output signal of the MPU. The MPU has an internal clock oscillator whose timing is controlled by an external quartz crystal. It contains two buses, an eight bit bidirectional data bus and a sixteen bit address bus. The function of the address bus is to address a particular memory location, either ROM, RAM or the GPIA (General Purpose Interface Adapter). The address decoder, also connected to the address bus, enables one of these elements. In the case of a RAM or the GPIA, the MPU also controls read and write modes. Data can then be transmitted over the bidirectional data bus connected to the MPU. Figure 8–3–2 illustrates the microprocessor bus configurations.

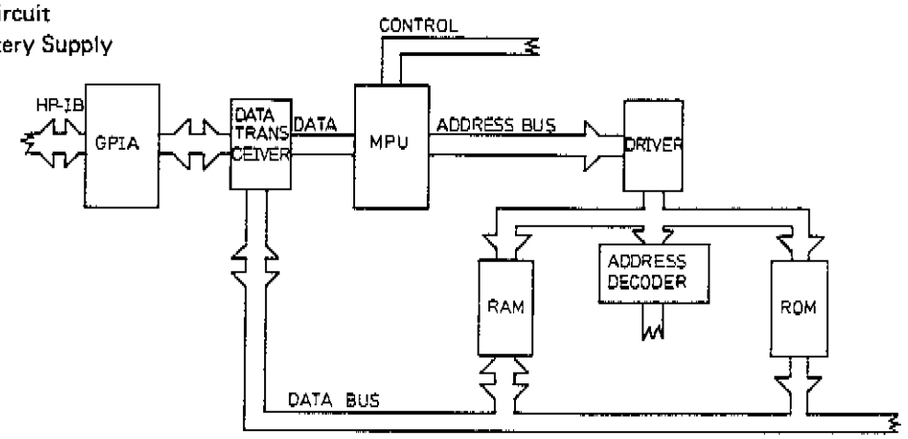


Figure 8–3–2. Bus configuration

2. Read Only Memory

The Read Only Memory is a device in which operational data is stored at manufacture. It can be read from but not written into. Data in a particular ROM location may be accessed by addressing that memory location and enabling the ROM. Addressing and reading data takes place on the address bus and data bus respectively. The 8116A uses ROM's requiring a twelve bit address, giving each device 4096 individual memory locations.

When enabled, the ROM outputs data from the addressed location to the data bus, so for practical purposes, the ROM may be considered as a decoder which transforms input addresses into specific output instructions. To perform a routine (set of specified instructions), the MPU addresses the first memory location of routine data and responds to the instruction it reads. When the instruction has been executed, the MPU addresses the next location, reads the instruction and responds. This cycle is continued until the complete routine has been executed. Some instructions may branch the controller to a sub-routine, while others are directed to the instrument based upon information stored in the ROM's.

3. Random Access Memory (RAM)

The Random Access Memory is the "scratchpad" element of the controller. Data in a memory location is destroyed each time new data is written in. Because Data is written in, read out at a later time and finally destroyed by new data, the contents of the RAM are never considered to be permanent, thus the term "scratchpad". Data stored in a RAM is also normally destroyed when power to the device is withdrawn. However, the 8116A has a 1K byte RAM which stores all current operating data when the instrument is switched off, due to a battery back-up.

RAM's contain two buses — an address bus (10 bits in this case) for the addressing of a particular memory location, and a bi-directional data bus for transmitting data in the read mode and receiving data in the write mode. Both RAM buses are connected to the respective MPU buses. The address decoder is also connected to lines of the address bus and controls the enabling/disabling of each RAM. Read and write functions are controlled by a single line from the MPU. Thus the MPU can enable and address a RAM for a read or write function.

4. HP-IB General Purpose Interface Adapter (GPIA)

The GPIA is part of the HP-IB section of the instrument and is merely an interface device between the MPU (and associated circuitry) and any other equipment operating on the HP-IB. Figure 8–3–3 shows the GPIA – MC 68488 – pinout configuration, while Table 8–3–1 describes the pinout functions. The pinouts can be divided into three groups:

a. MPU Interface
b. Interface between 8116A and other equipment on the HP-IB via bus drivers
c. Control Signal group.

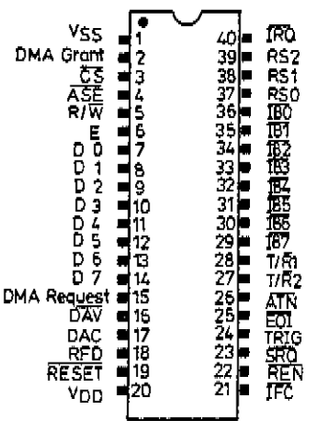


Figure 8–3–3. GPIA pinouts

Table 8–3–1. GPIA pinout functions

a. MPU Interface
Bidirectional data lines (D0 ..... D7) — allows the transfer of data between MPU and GPIA. The output drivers are tri-state devices. Chip Select ($\overline{CS}$) — used to select the GPIA via subdecoder. A negative-going edge selects the GPIA. READ/$\overline{WRITE}$ line (R/$\overline{W}$) — connected to the MPU's R/$\overline{W}$ signal and controls register access and direction of data transfer on the bus. This signal is used in conjunction with the Register Select lines. Register Select lines (RS0, RS1, RS2) — connected to the three lowest address lines A0, A1, A2 to provide selection of the different GPIA registers.

Interrupt Request ($\overline{IRQ}$) – connected to the common interrupt bus line for the MPU.

$\overline{RESET}$ Input used to initialize the GPIA during power-up. The $\overline{RESET}$ signal is generated in the same manner as for the MPU. (See Service Block 2 – Power Supply).

E (Enable Clock, 0) – activates the address inputs, R/W inputs and enables data transfer to the MPU data bus. Also used internally as a state counter, allowing the device to change interface states. E is connected to the MPU clock output.

b. Interface with the HP-IB

Signal lines IB0 ..... IB7 allow the flow of ASCII interface messages and device dependent messages.

Byte transfer lines (DAC, RFD, $\overline{DAV}$) – provide the three-line handshake between source and acceptor. Positive-going RFD indiates that all acceptors are "Ready For Data". A source will indicate that data is valid by pulling DAV low. Upon reception of valid data, DAC will go high, indicating that an acceptor has accepted data.
Bus management lines ($\overline{ATN}$, $\overline{IFC}$, $\overline{SRQ}$, $\overline{EOI}$, $\overline{REN}$) are used to manage the flow of information over the interface lines.

c. Control Signal group

Address Switch Enable ($\overline{ASE}$) is used to enable the tri-state buffer that connects the instrument address switch to the MPU data bus. TRIG, DMA Grant and DMA Request are not used.

GPIA Internal Register.
The MPU has access to the GPIA internal registers via the register select lines and the R/$\overline{W}$ line.

5. Address Decoder

The Address Decoder is the ROM and RAM enabling device. Decoding is performed at two levels (see Figure 8–3–4). Firstly at the Main Decoder (U12) which is dependent upon the status of address lines A12, A13 and A15, and secondly at sub-decoder U13, which is enabled by the main decoder and responds to address lines A8, A9 and A10. The main decoder (U12) enables ROM's 1 to 6, with signals $\overline{ROM1}$ to $\overline{ROM6}$, and both sub-decoders. Sub-decoder U13 Select provides RAM's U10 and U11 Select signals, Keyboard scanner signals and the GPIA Select signal.

Subdecoder U14 is dependent upon address lines A0, A1 and A2. Output signals from this device enable the HP-IB Status Latch, Keyboard Display Latches, Device Bus Feedback driver and the Bus driver (see Service Block 4). Thus, the address performs two functions; not only does it indicate the memory location within the ROM or RAM specified when applied through the address decoder, it also identifies the element to be enabled.

6. Reset

When the instrument is switched on, the MPU requires a period of time for the power supply to become established before the $\overline{RESET}$ signal goes false (high). This period is achieved by the CR network R12 (3 x 10k) and C4. U27D output goes high when C4 has charged to approximately 420 mV, and the $\overline{RESET}$ signal to the MPU and GPIA is therefore withdrawn, allowing the two devices to become operational. The time taken for $\overline{RESET}$ to go false after switch-on is in the order of 2.5 ms.

When the instrument is switched off, transistor U29C is turned on via U27B, and provides a current path for C4 to discharge. U27D output then goes low and the $\overline{RESET}$ signal is established before the MPU and GPIA rails are totally withdrawn.

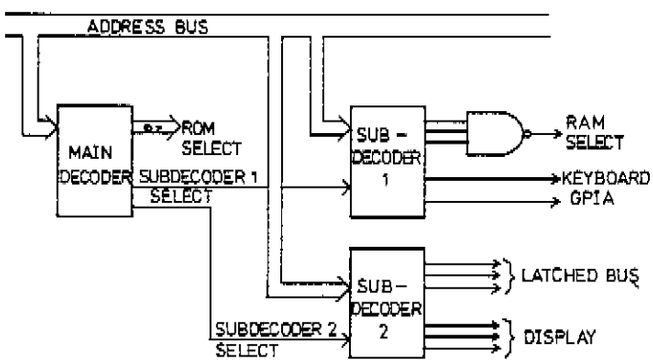


Figure 8–3–4. Address decoding

7. RAM Battery Supply

RAM's U10 and U11 draw their power, under normal conditions, from the +5 V rail via transistor Q1. The battery at this time is charging through R7. At switch-off, the RAM $\overline{CS}$ signal goes false (high) and Q1 is switched off as a result of the Power Fail signal being sent. As soon as Q1 collector potential begins to fall, power from the battery is made available to the RAM's via U28. Thus the Vcc input to both RAM's is never allowed to deteriorate sufficiently for the contents to become corrupted or lost.

8-8d

NOTE: If an error code is shown in the display it is necessary to press a key, eg LCL, to set the u-Processor to normal routine, then troubleshoot the instrument.

Free Run Signature Analysis

For Signature Analysis purposes the u-Processor is set to a free run routine which makes it increment through all addresses continuously. This is achieved by giving some hardware programmed command to the u-Processor which increments the address register by one continuously via CR1 and CR2, when jumper P1 is set to "Free Run" position.

The NMI input has to be held at high potential, so disconnect wire A2W2.

Before the u-Processor accepts the hardware programmed command it has to be reset by shorting RES to ground for a short time.

Address Bus Drivers, Main Decoder and Subdecoders

The Address Bus Drivers/Decoders can be checked by signature Analysis. Set u-Processor to "Free Run" by setting jumper P1 to position "P1" on board A3, disconnecting wire A2W2 and resetting the u-Processor. Set and connect the Signature Analyzer as given in table 8–3–2.

Signature Analyzer	A3 u-Processor Board Assy
Start ⌐	TP "SA"
Stop ⌐	TP "SP"
Clock ⌐	TP "E"
⊥	⊥

Table 8–3–2. Signature Analyzer setting and connection to A3 u-Processor Board Assy for Address-Driver/Decoder Test

NOTE: Verify that reading at +5 V is 0003. If not, the u-Processor is not free-running.

Check the signatures for U3, U4, U10, U11, U12, U13, U14 and U36 against the signatures given in the signature analysis layout. Set u-Processor to "free run" as described above.

ROM TESTING

Signature Analyzer	A3 u-Processor Board Assy
Start ⌐ }	TP1 for U38, TP2 for U9,
Stop ⌐ }	TP3 for U8 etc.
Clock ⌐	TP "E"
⊥	⊥

Table 8–3–3. Signature Analyzer setting and connection to A3 u-Processor Board Assy for ROM-Test

NOTE: Verify that reading at +5 V is P254. If not, the u-Processor is not free running.

EXCHANGING ROM's

When exchanging ROM's, the data saved in the RAM during periods of power-off has to be made compatible with the new ROM data. This can be achieved by setting the 8116A to an error condition, e.g. "E.WID" and "SINE", then turning the instrument OFF and ON again.

Should a processor "hang-up" occur, rendering the instrument inoperable, switch the instrument OFF and disconnect the RAM back-up battery for 30 seconds. This will have the effect of destroying stored data. Reconnect the battery, and switch the instrument ON. The standard Parameter Set will now be loaded into the RAM.

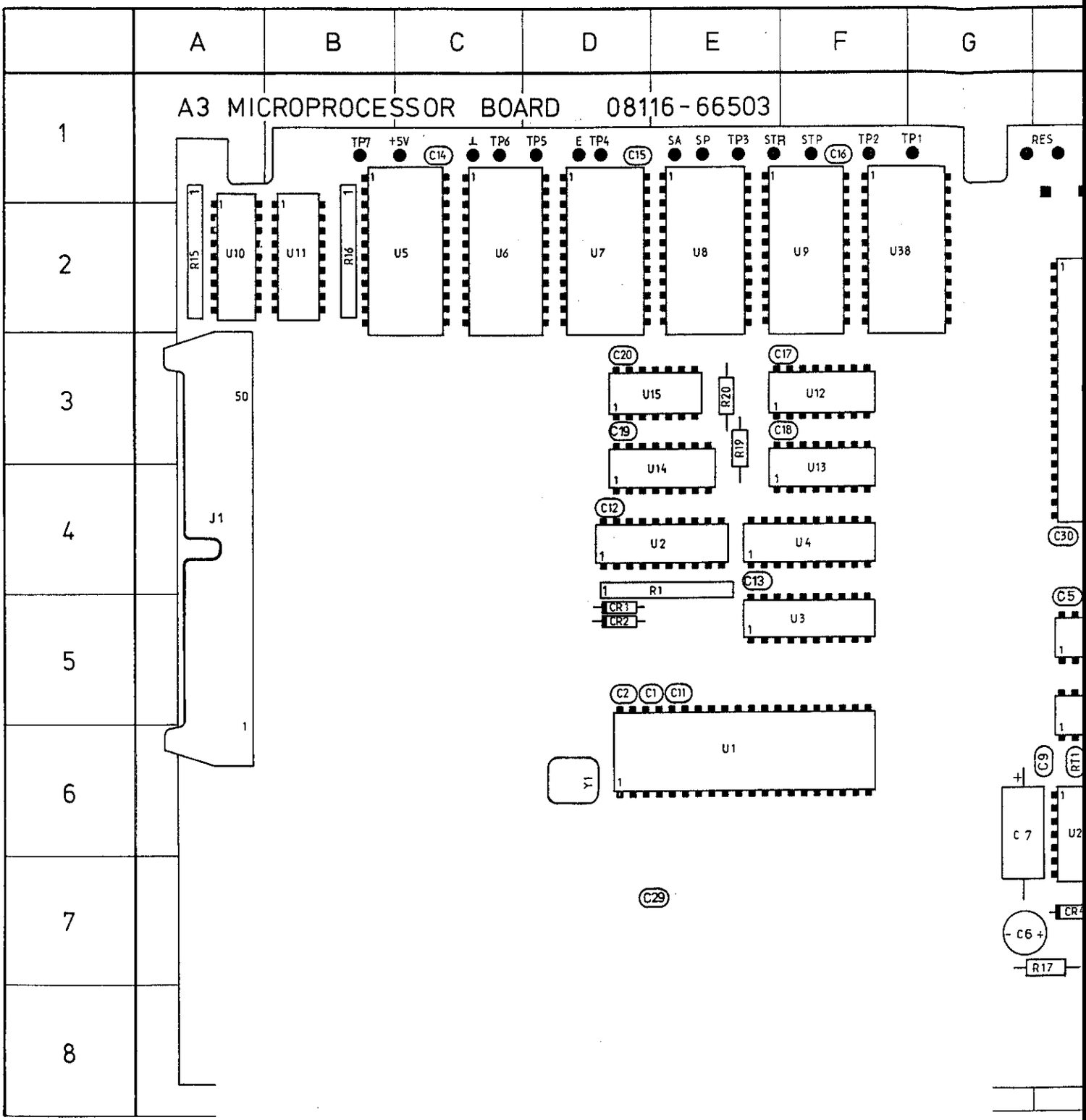
Pin No.	U3	U4	U12	U13	U14
1					
2					
3	6F9A	0002			
4					
5	U759	9UPI			
6					
7	0356	4868	4IP4	748C	PHCC
8					
9	IU5P	4FCA	3IAC	8069	C6PI
10			36F8	U638	HC8A
11			4685	9CPH	6P25
12	P763	6U28	2OUO	359H	C89C
13			I8H7	H883	P26P
14	8484	37C5	IC66	OA8U	89C7
15			2340	5HP5	26HI
16	FFFF	6321			
17					
18	UUUU	7791			

Pin No.	U10	U11	U36
1			667C
8	8UP9	8UP9	

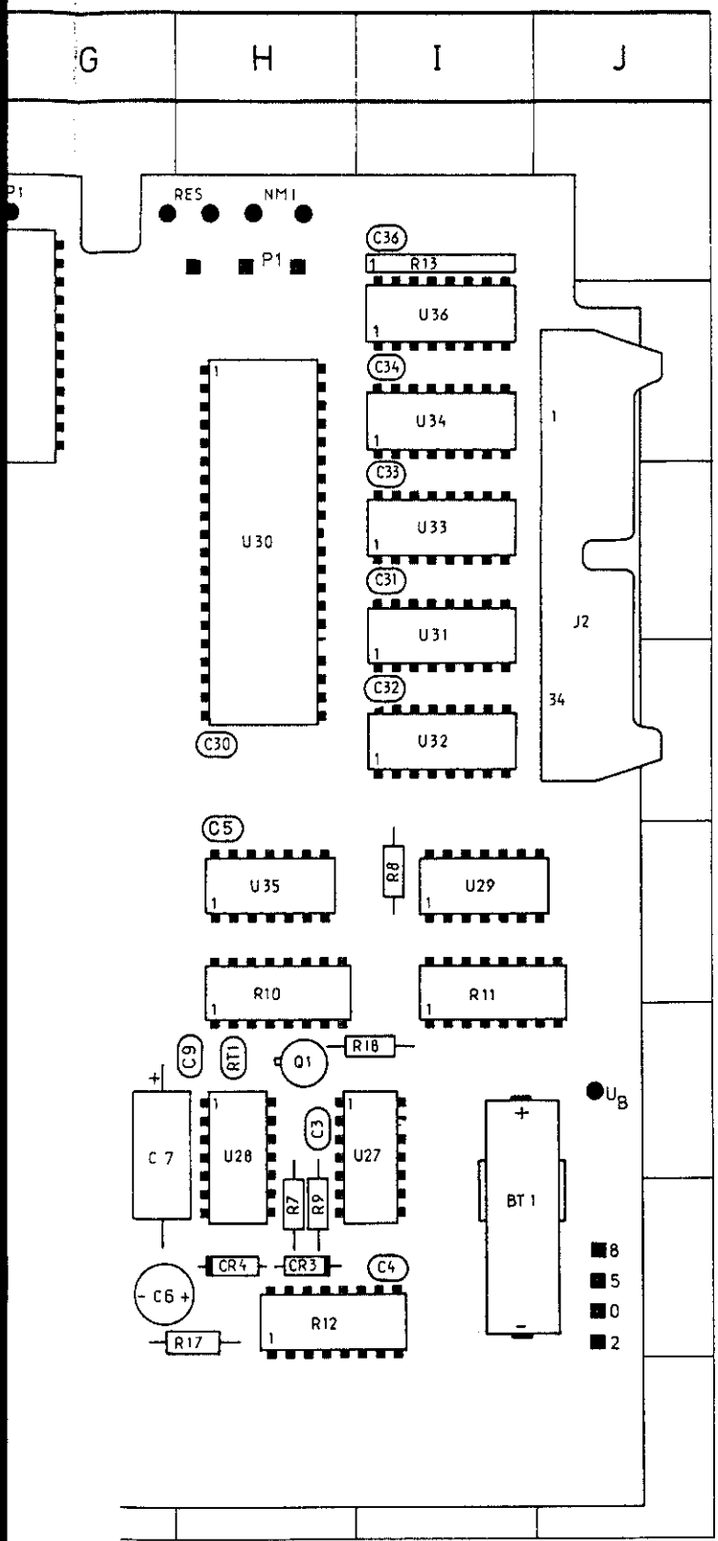
ROMS

Pin No.	U5	U6	U7	U8	U9	U38
9	278A	P726	873U	A4P3	HHU5	55FU
10	6A4H	PPAC	4H66	AC35	001P	384F
11	4731	U658	H178	7H9P	FA3H	H52H
13	U9H8	H7A7	3OA9	9H7O	936H	PHI6
14	6344	CP5F	459U	61U7	64PA	6517
15	PCC0	9P52	2F1A	3061	A738	01FC
16	8PII	A3OC	9C95	FH3C	PC47	P77H
17	9A08	H5UU	3719	COC9	C5CF	HCH4
24	P254	P254	P254	P254	P254	P254

Microprocessor, Sht 1 of 2

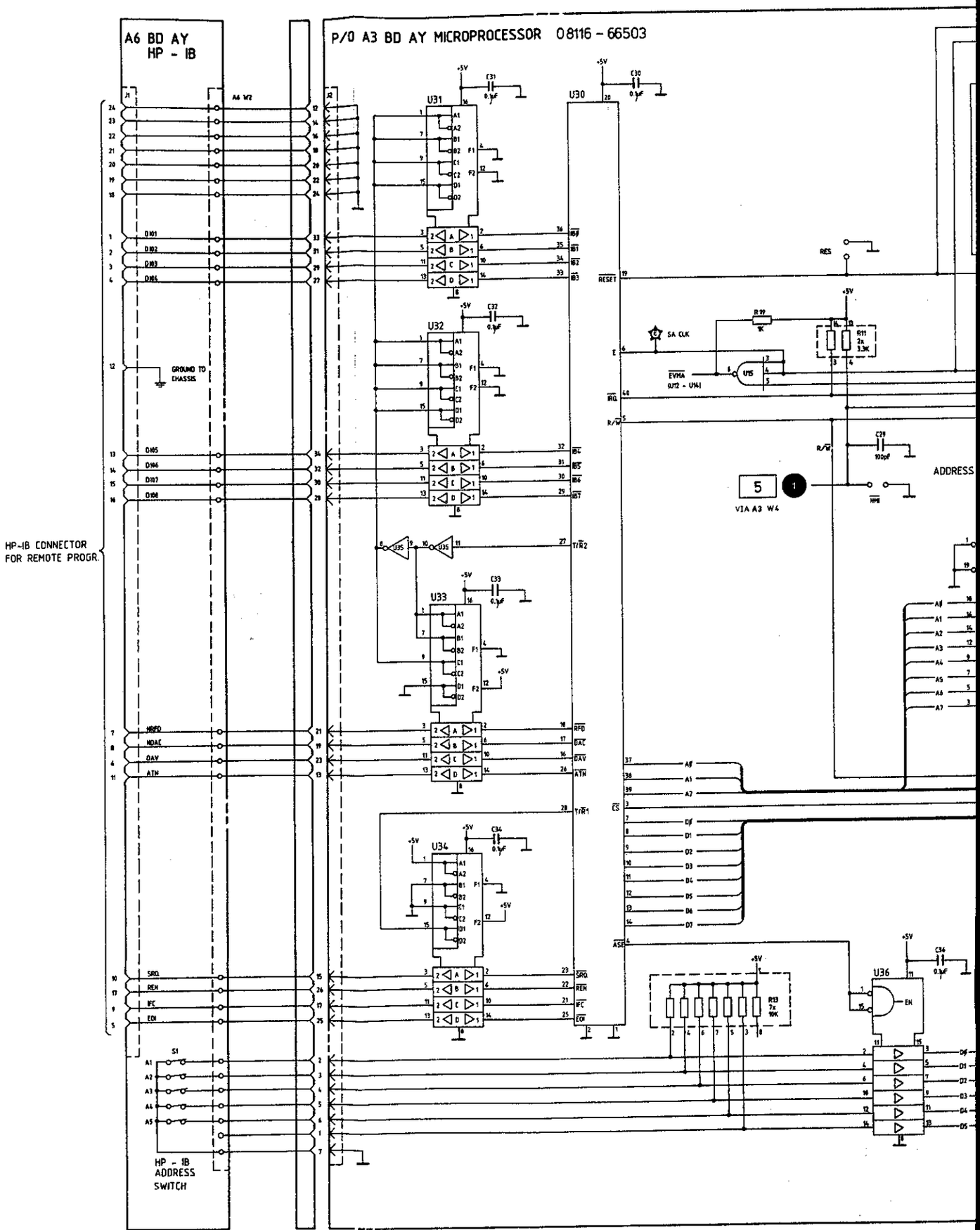


Microprocessor, Sht 2 of 2

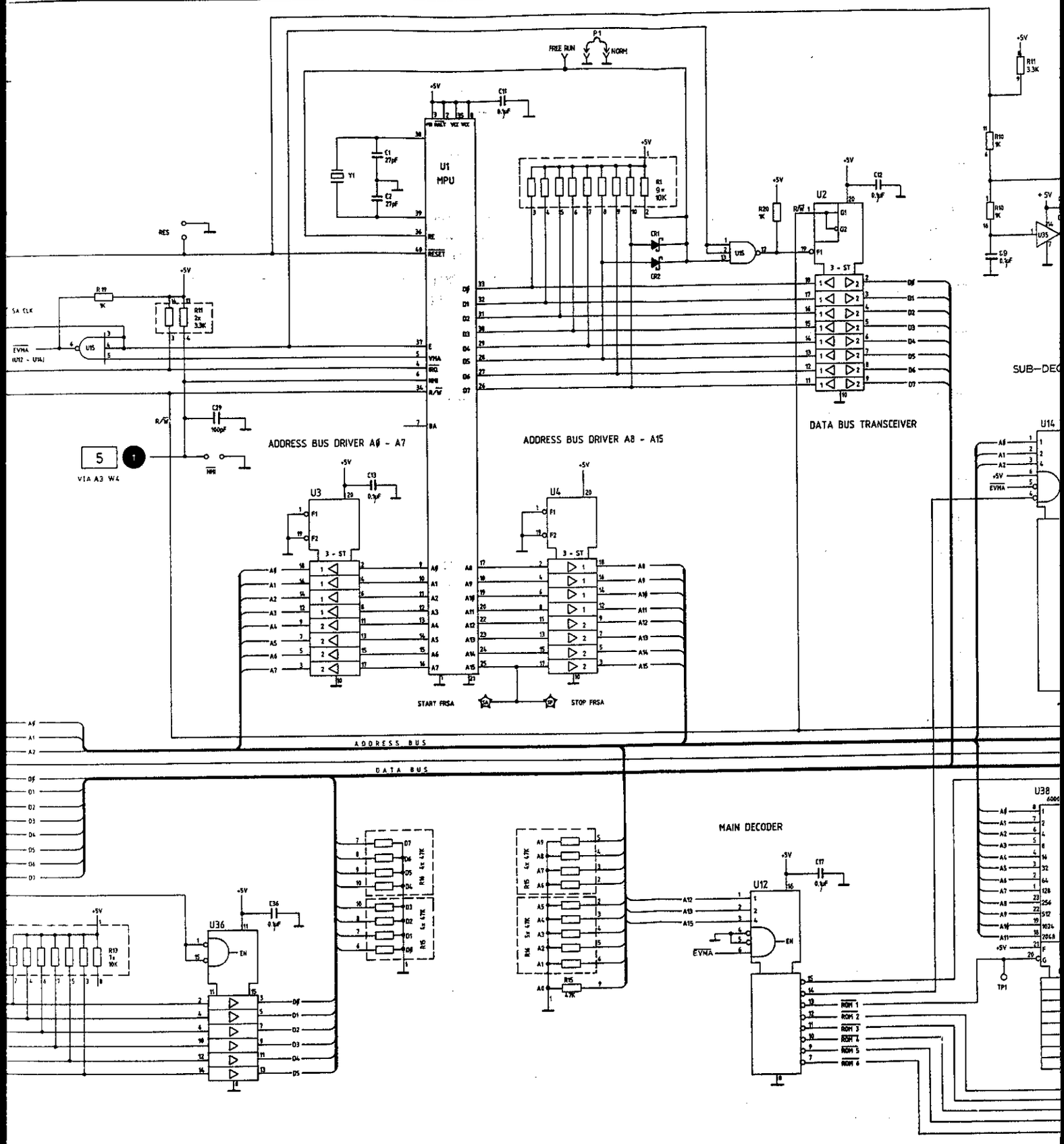


COMP	REF	COMP	REF
C1	E5	R12	H7
C2	D5	R13	I2
C3	H6	R15	A2
C4	I7	R16	B2
C5	H5	R17	H7
C6	G7	R18	I6
C7	G6	R19	E3
C9	H6	R20	E3
C11	E5	RT1	H6
C12	D4	U1	E6
C13	F4	U2	E4
C14	C1	U3	F5
C15	D1	U4	F4
C16	F1	U5	C2
C17	F3	U6	C2
C18	F3	U7	D2
C19	D3	U8	E2
C20	D3	U9	F2
C29	D7	U10	A2
C30	H4	U11	B2
C31	I3	U12	F3
C32	I4	U13	F4
C33	I3	U14	E4
C34	I2	U15	E3
C36	I1	U27	H6
CR1	D5	U28	H6
CR2	D5	U29	I5
CR3	H7	U30	H3
CR4	H7	U31	I4
P1	H1	U32	I4
Q1	H6	U33	I3
R1	E5	U34	I2
R7	H7	U35	H5
R8	I5	U36	I2
R9	H7	U38	F2
R10	H6	Y1	D6
R11	I6	BT1	I7

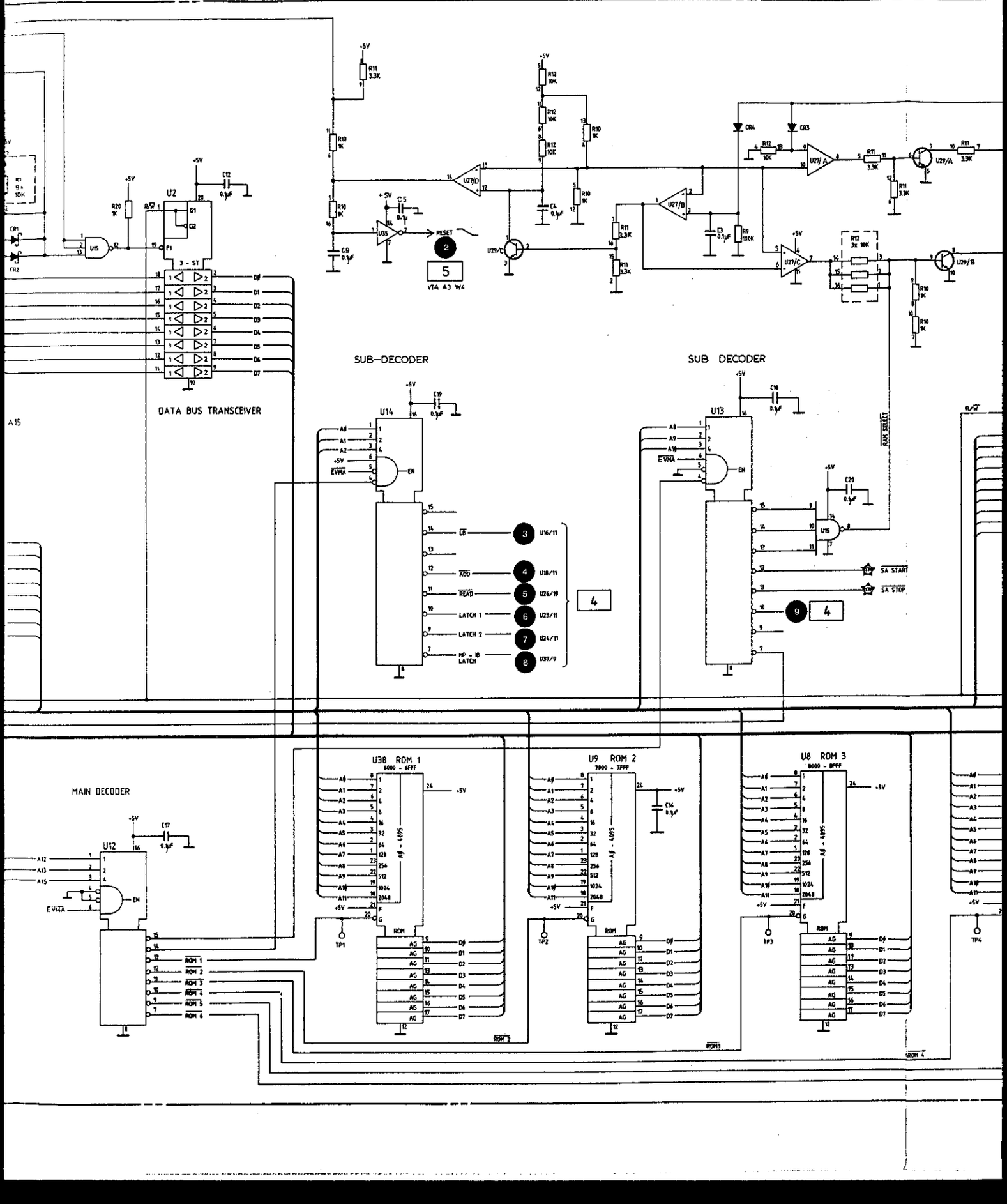
Microprocessor, Schematic
Sht 1 of 4



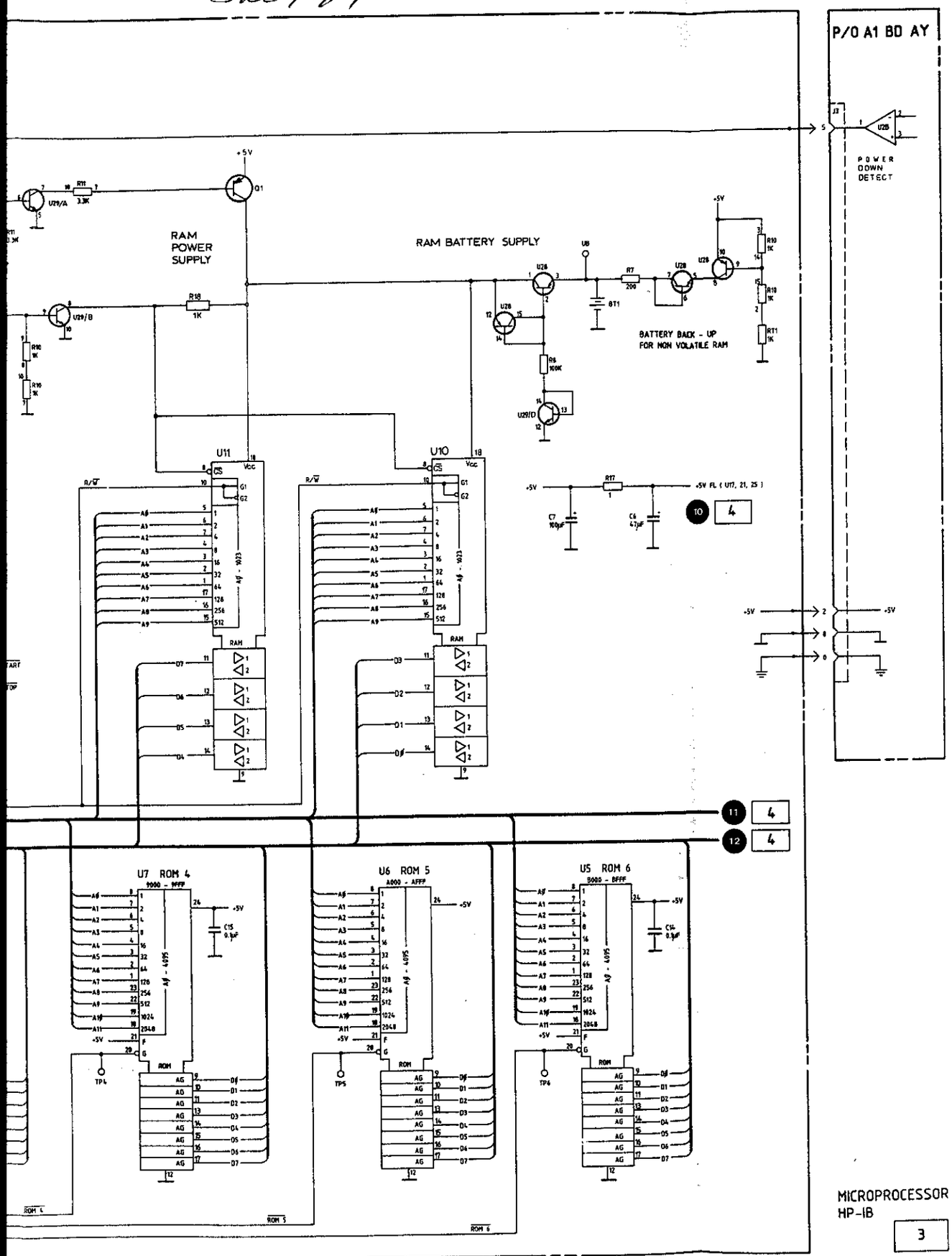
Microprocessor Schematic
Sht 2 of 4



Microprocessor, Schematic
Sht 3 of 4



Microprocessor, Schematic
Sht 4 of 4



SERVICE BLOCK 4

DEVICE BUS CONTROL, KEYBOARD, DISPLAY BOARD THEORY OF OPERATION

General Description

The Device Bus Control section is part of MPU bd assy, and provides necessary interfacing between 2 general instrument areas:

MPU/ROM's and Keyboard/Frontpanel displays.
MPU/ROM's and Control Board data bus.

In addition, all Address decoding between MPU and Control Board is performed in this section.

The circuits of the Device Bus Control section can be divided into the following sections:

1. Control Board Address Decoding.
2. Key Scanner Bus.
3. Latched data bus and associated devices.
4. Display Driver.
5. Keyboard Assembly.
6. Display Board Assembly.

1. Control Board Address Decoding

Address decoding for the Control Board functions is primarily undertaken on the MPU board. Secondary decoding is performed on the Control board assembly itself. Address bits A3 to A9 and A14 are passed through Latch U18 (under control of U14 on the MPU board) to Bus Driver U21, with the exception of A14 which becomes the MODE control for the display driver (described later). Decoder U17 provides Write Select signals $\overline{WS1}$ to $\overline{WS6}$ and the $\overline{WRITE}$ signal to the display driver.

2. Key Scanner Bus

The Key Scanner Bus merely examines the status of the Keyboard assembly to sense which of the frontpanel pushbutton or vernier keys have been selected. U20 is a BCD to decimal converter. Address lines A3, A5 and A4 (binary inputs) are incremented from one to six continuously. The decimal outputs are configured to form the vertical signal paths of the frontpanel key matrix (pushbutton and vernier), such that only one line is set low at any given time.

Meanwhile U17 (8 line to 1 line selector) selects each of its inputs individually, under control of address lines A0, A1 and A2. The eight inputs to U19 form the horizontal signal paths of the keyboard matrix, and are all individually examined each time the address to U20 is incremented. In this way, the status of data line D7 (U19 output) is always representative of the part of the keyboard matrix which has been selected for scrutiny by the address lines A0, A1 and A2 in combination with A3, A4 and A5. Therefore the MPU is always aware of which frontpanel pushbutton or vernier key (if any) has been selected.

3. Latched Data Bus and associated devices
(see Figure 8-4-1)

The latched Data bus performs three distinct functions — the devices on the bus being enabled by sub-decoder U14 (described in Service Block 3). The functions are as follows:

i) Distribution of data on the main bus to Parameter Backlighting, Control, Mode and Unit LED's, and HP-IB Status LED's via the Keyboard Display Latches and HP-IB Latch.

ii) Feed data from the main bus to the device bus for use by DAC's on the Control Board via the Device Bus Latch and Device Bus Transceiver.

iii) Provide data to the numerical displays and Key LED's via the display driver (U22).

4. Display Driver

The Display Driver switches the Key, Control, Mode and Unit LED's and Digital Display in a matrix fashion, similar to the Keyscanner technique. The outputs DIG0 to DIG7 for the vertical signal paths of the matrix and the outputs a to g and DP form the horizontal signal paths as well as being routed to the individual display segments. Built into the driver is an 8 x 8 static RAM, permitting the storage of eight sets of display data at any given time.

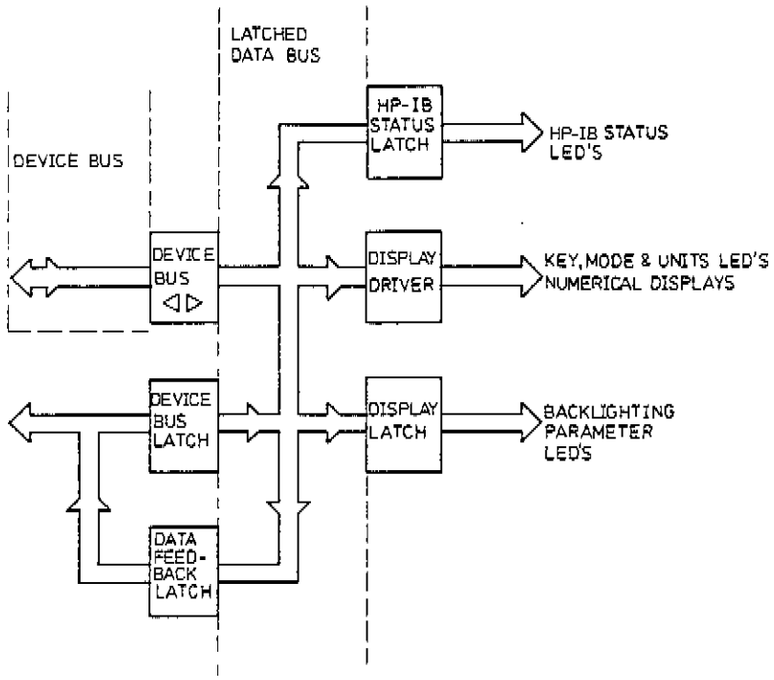


Figure 8–4–1. Latched data distribution

The control instructions are read from the bus lines if MODE is high and $\overline{\text{WRITE}}$ is low. After control instructions have been read, display data can then be written into memory with each following negative going pulse of $\overline{\text{WRITE}}$, -MODE being low. After all eight words or digit memory locations have been written into, additional transitions of $\overline{\text{WRITE}}$ are ignored. Table 8–4–1 shows control instruction definitions while figure 8–4–2 illustrates switching waveforms.

CONTROL INPUT	PIN	STATUS	FUNCTION
$\overline{\text{WRITE}}$	8	HIGH	Data not loaded into RAM
		LOW	Data loaded into RAM
MODE	9	HIGH	Load control word on WRITE pulse.
		LOW	Load data on WRITE pulse.

Table 8–4–1. Display driver control instructions

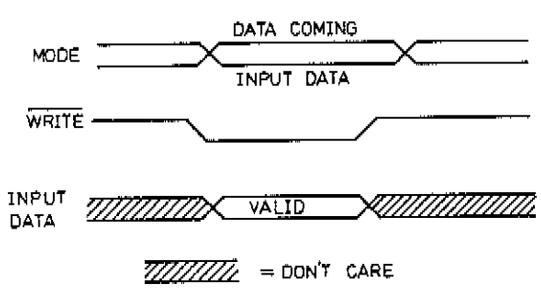


Figure 8–4–2. Display driver waveforms

5. Keyboard Assembly

The Keyboard assembly (A4 board) is a switch panel on which all Mode, Control, Parameter, Waveform selection, Output and Trigger control pushbuttons are located. In addition, those status LED's which are housed in pushbuttons are present on this board.

As previously stated, the pushbutton key connections are matrixed with the key scanner bus, while the pushbutton status LED's are matrixed with the Display Driver bus.

6. Display Board Assembly

The Display Board Assembly (A5 board) is the panel on which the three Vernier switches and the Range switch are located. All backlighting (mnemonic) parameter LED's, Control, Mode and Unit LEDs and Alpha-numeric displays are present on this panel.

The backlighting parameter LED's are under the control of the data bus via the display latch, with the Vernier (and Range) and remaining indicators being matrixed with the key scanner bus and Display Driver respectively.

SERVICE BLOCK 4 TROUBLESHOOTING GUIDE

NOTE: If an error code is shown in the display it is necessary to press a key, e.g. LCL, to set the u-Processor to normal routine, then troubleshoot the instrument.

Keyboard

The keyboard can be checked with help of signature analysis at A3 TP7 when the u-Processor is in free run mode. To set the u-Processor to free run mode set jumper P1 into position P1 on board A3. Disconnect jumper W2 on Control Board A2. Connect RES to gnd. for a short time to reset the u-Processor.

Signature Analyzer	A3 u-Processor Board Assy
Start	TP "SA"
Stop	TP "SP"
Clock	TP "E"
⊥	⊥

Table 8–4–2. Signature Analyzer setting and connection to A3 u-Processor Board Assy

NOTE: Verify that reading at +5 V is 0003. If not, the u-Processor is not free running. Press one key after another and check the signature for each key at TP7 against table 8–4–3.

Bus Driver/Decoder Control Signature Analysis

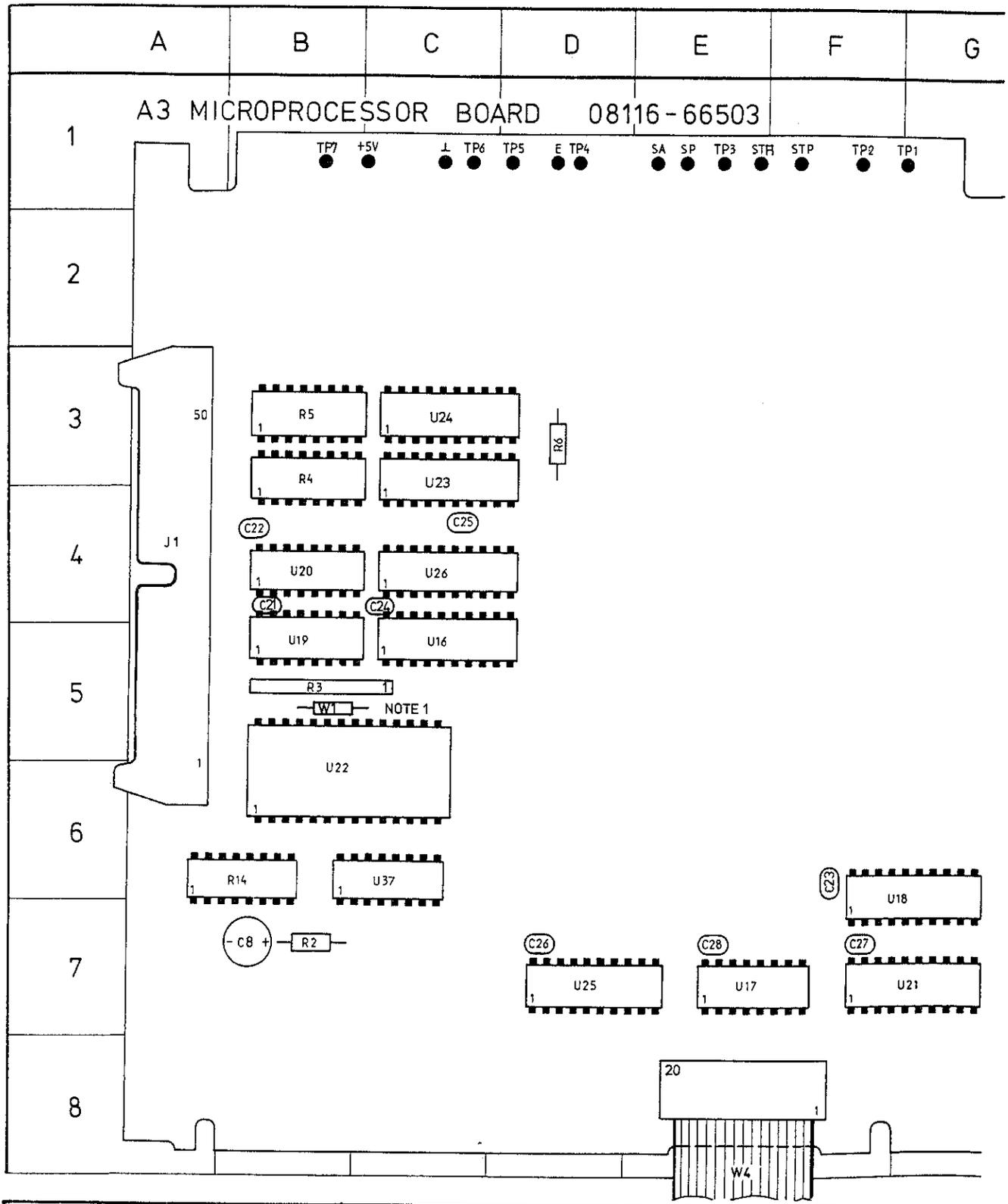
Set u-Processor to free run mode as described above. Set and connect Signature Analyzer as given in table 8–4–2.

Pin No.	U17	U18	U21
2		P50H	
3			P50H
5		CH9U	3P76
6		8759	
7	5U3F		9HIH
9	IFH6	3P76	9HIP
10	8U95		
11	55F4	C898	9HIP
12	79HU	65A5	65A5
13	PU99		
14	IP50		FF4H
15		FF4H	
16		9HIH	8759
18		HPAU	CH9U

Key	TP7 Reading	
	Option	Standard
no key pressed	6F80	0003
LCL	U165	9HP6
MODE 1 (Norm,Trig etc)	8P09	P28A
MODE 2 (Sweep, Burst)	9422	
CTRL (AM, FM, etc)	52A8	3P2C
STA	630A	
STP, RPT	PU62	
SWT, BUR	4F78	
FRQ, MRK	1778	7CUC
DTY, WID	327P	5PUH
HIL, AMP	A503	F980
LOL, OFS	5PPO	3263
–90°	OCU9	677A
Slope	U55P	99HH
Slope	4AU7	2674
MAN	P51H	899P
1 Cycle	FPP7	
∿	U96U	95PF
∿	89UC	P578
⊓	15HP	795H
⊔	8UA6	P325
Auto Vernier	P018	8F9C
Limit	8363	PUP0
Complement	92C2	UP31
Disable	H30F	CU8U
Vernier MSD UP	62HH	0P5P
Vernier MSD DOWN	UCHU	975F
Vernier SSD UP	PU17	8394
Vernier SSD DOWN	8957	P5H4
Vernier LSD Up	OF65	60P6
Vernier LSD DOWN	55U5	3976
Range UP	U4C9	983A
Range DOWN	4A8P	26OH

Table 8–4–3. Keyboard Signatures

HP-IB Latch	PHCC
$\overline{\text{READ}}$	6P25
$\overline{\text{LB}}$	89C7
Latch 1	HC8A
Latch 2	C6PI

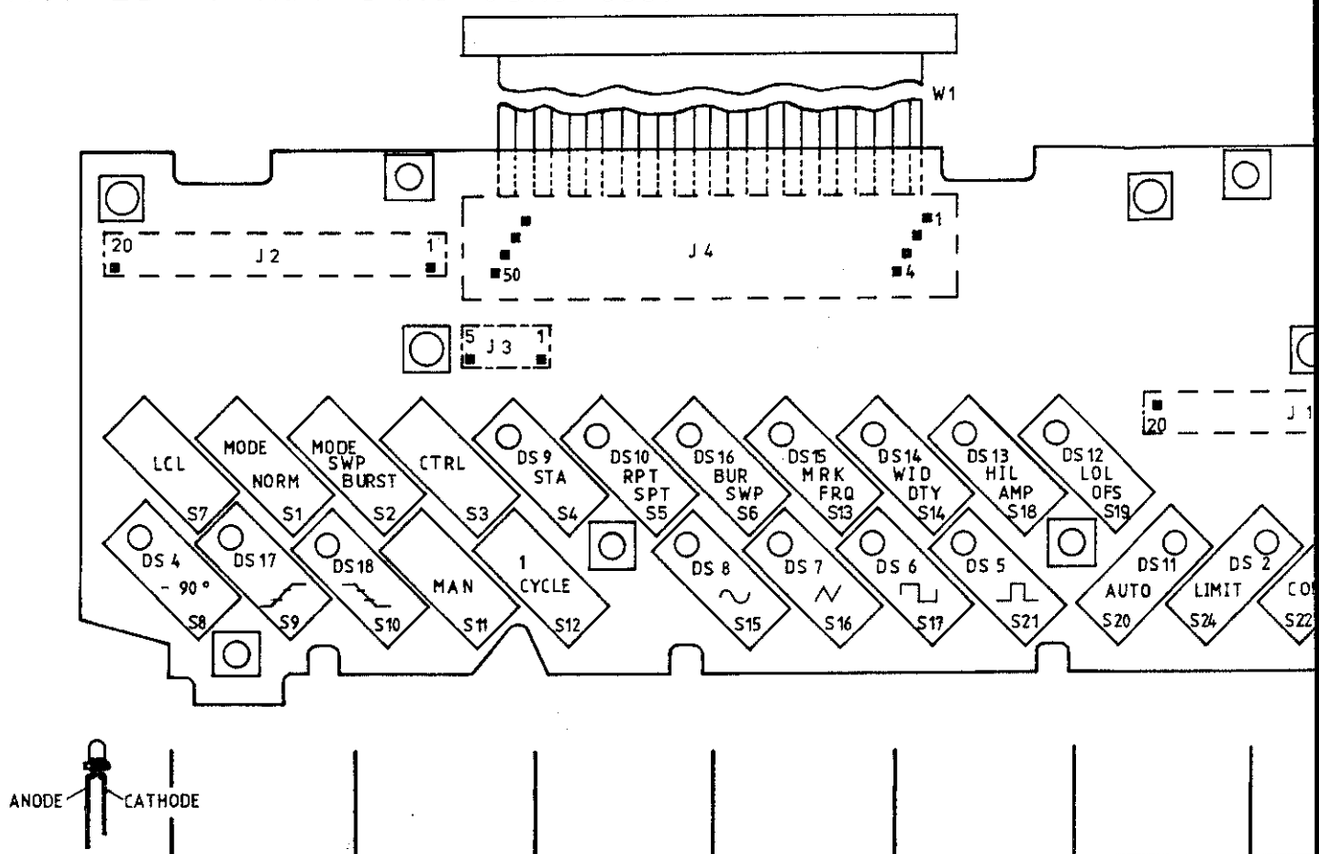


COMP	REF			COMP	REF			COMP	REF
C8	B7	C26	D7	R5	B3	U19	B5	U25	D7
C21	B4	C27	F7	R6	D3	U20	B4	U26	C4
C22	B4	C28	E7	R14	B6	U21	G7	U37	C6
C23	F7	R2	B7	U16	C5	U22	B6	W4	F8
C24	C4	R3	B5	U17	E7	U23	C3	J1	A4
C25	C4	R4	B3	U18	G6	U24	C3		

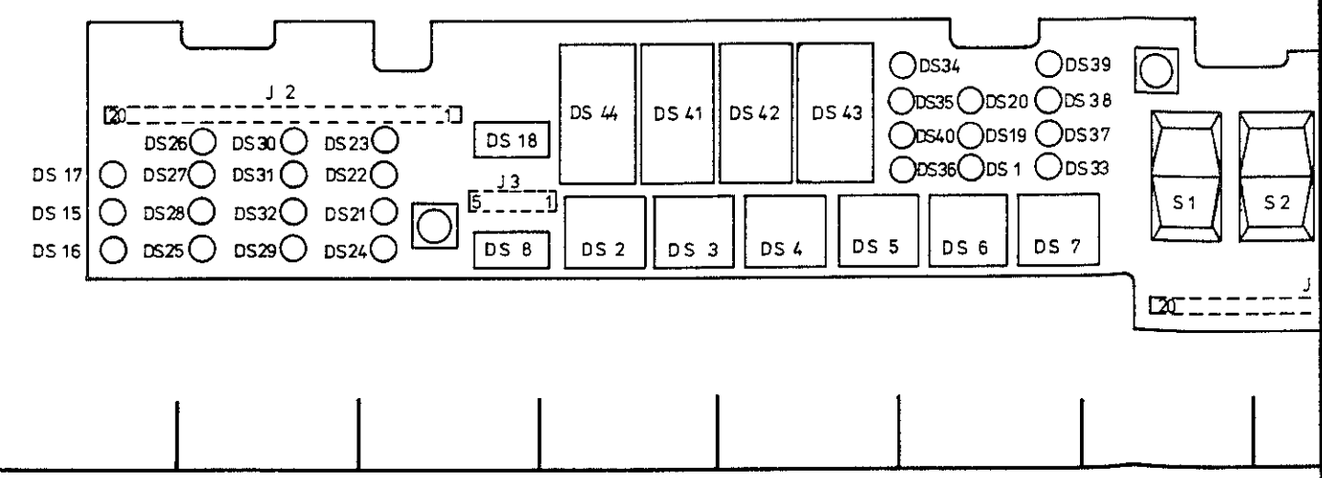
8-11b

Device Bus Control
Sht 1 of 2

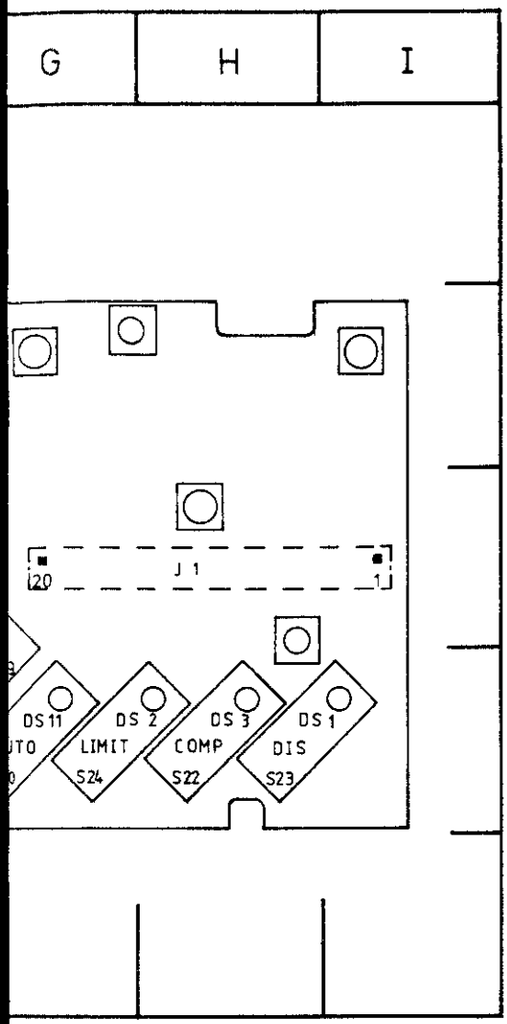
A14 BD AY KEYBOARD 08116-66514



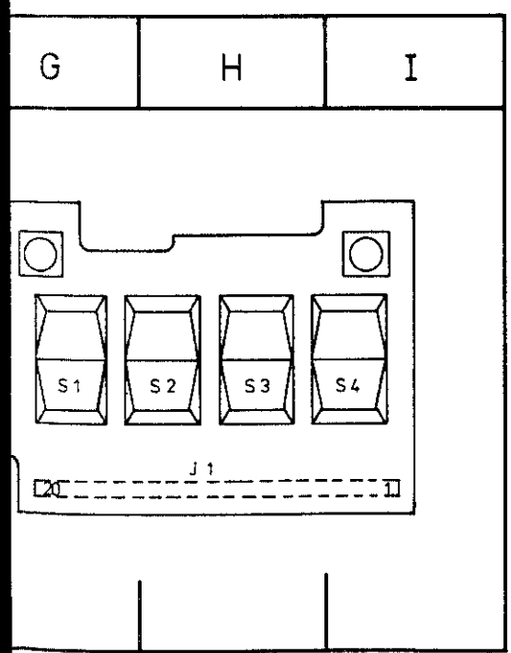
A15 AY BD DISPLAY 08116-66515



Device Bus Control
Sht 2 of 2

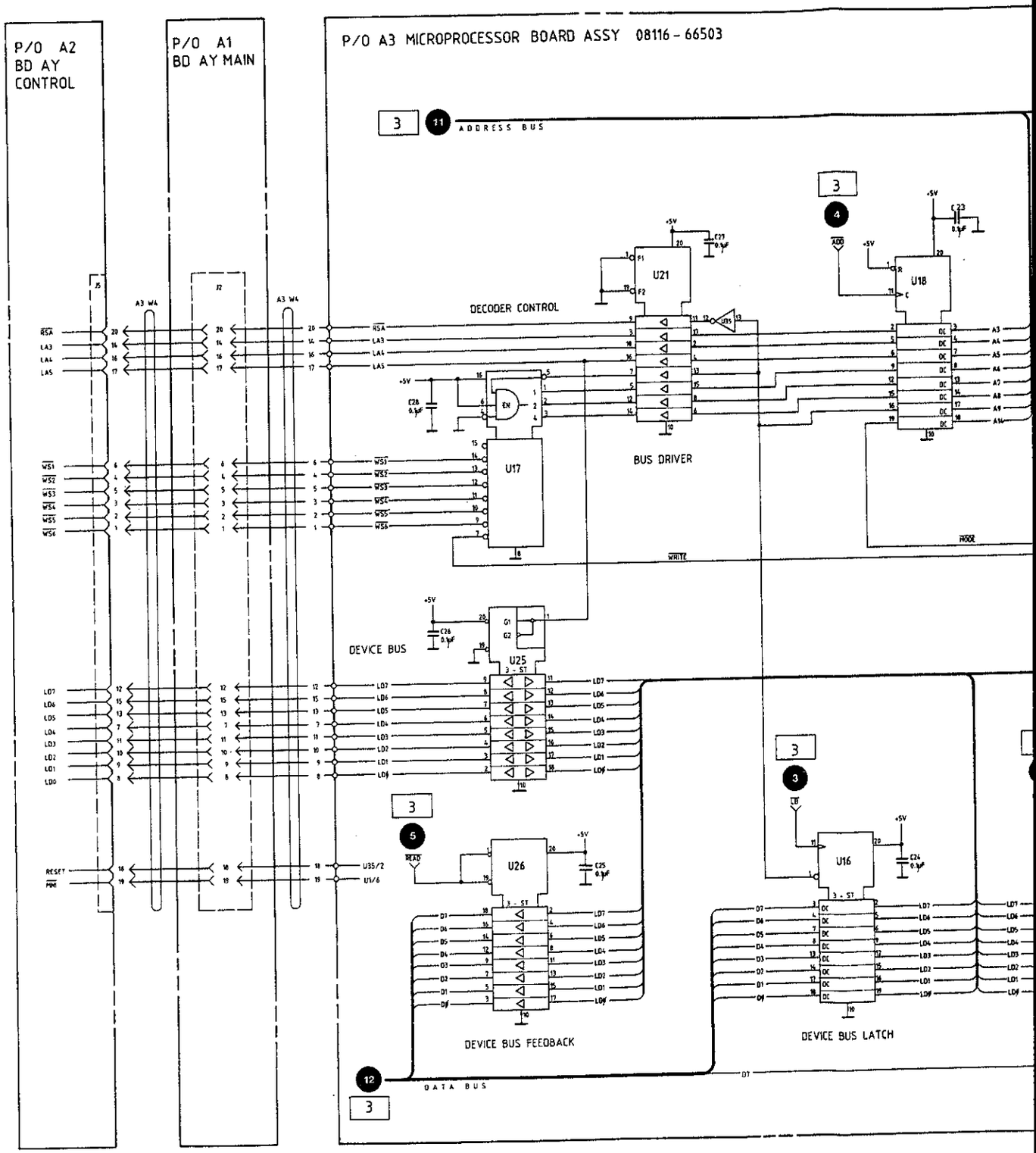


COMP	REF	COMP	REF
DS1	I4	S4	C3
DS2	H4	S5	D3
DS3	H4	S6	D3
DS4	A4	S7	A3
DS5	F4	S8	A4
DS6	E4	S9	B4
DS7	E4	S10	B4
DS8	D4	S11	C4
DS9	C3	S12	C4
DS10	D3	S13	E3
DS11	G4	S14	E3
DS12	G3	S15	D4
DS13	F3	S16	E4
DS14	E3	S17	E4
DS15	E3	S18	F3
DS16	D3	S19	F3
DS17	B4	S20	G4
DS18	B4	S21	F4
J1	H3	S22	H4
J2	B2	S23	I4
S1	B3	S24	G4
S2	B3	W1	D/E1
S3	C3		

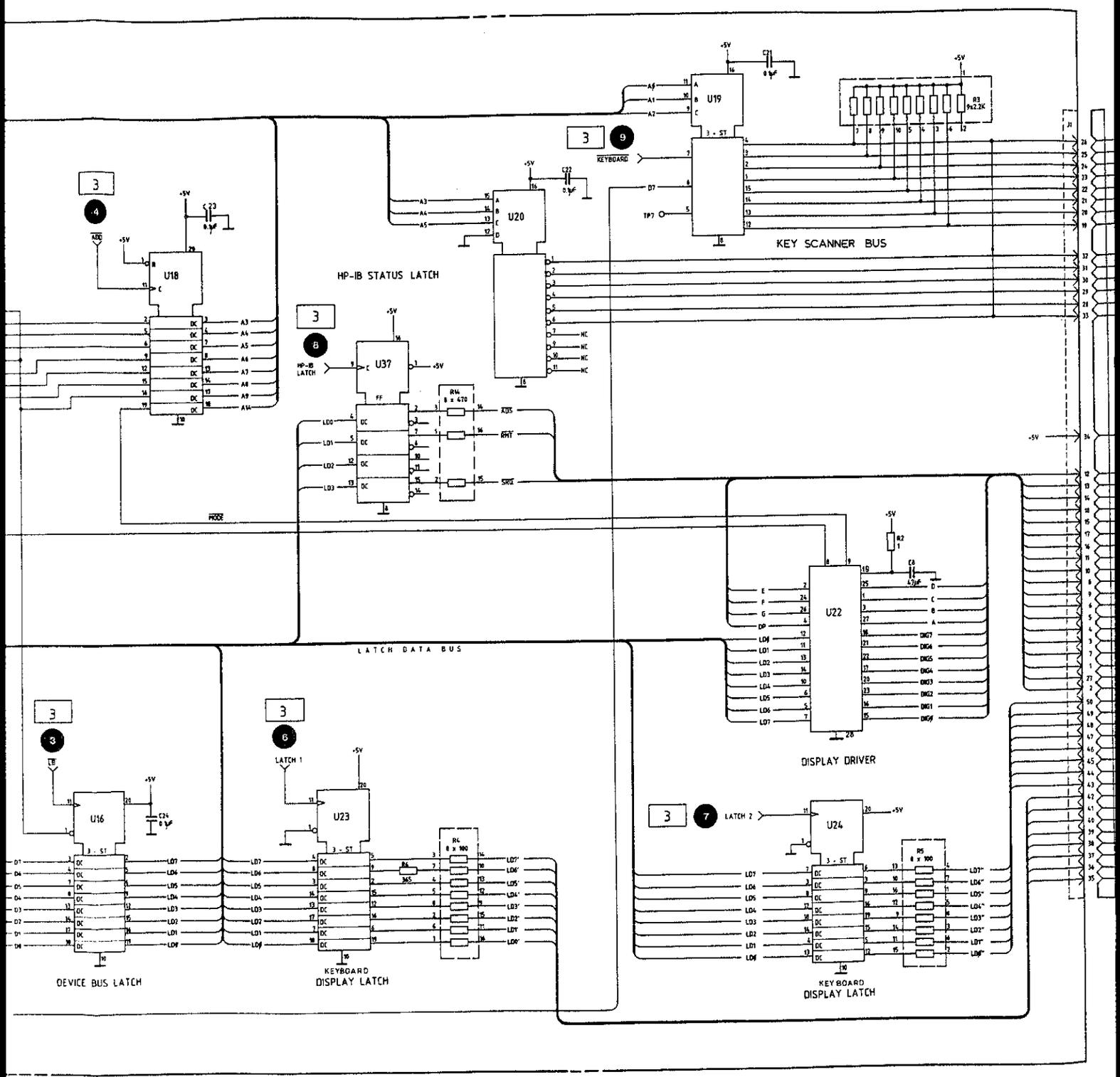


COMP	REF	COMP	REF	COMP	REF
DS1	F2	DS22	C2	DS37	F2
DS2	D2	DS23	C2	DS38	F2
DS3	D2	DS24	C2	DS39	F1
DS4	E2	DS25	A2	DS40	F2
DS5	E2	DS26	A2	DS41	D2
DS6	F2	DS27	A2	DS42	E2
DS7	F2	DS28	A2	DS43	E2
DS8	C2	DS29	B2	DS44	D2
DS15	A2	DS30	B2	J1	H3
DS16	A2	DS31	B2	J2	B2
DS17	A2	DS32	B2	J3	C2
DS18	C2	DS33	F2	S1	G2
DS19	F2	DS34	F1	S2	H2
DS20	F2	DS35	F2	S3	H2
DS21	C2	DS36	F2	S4	I2

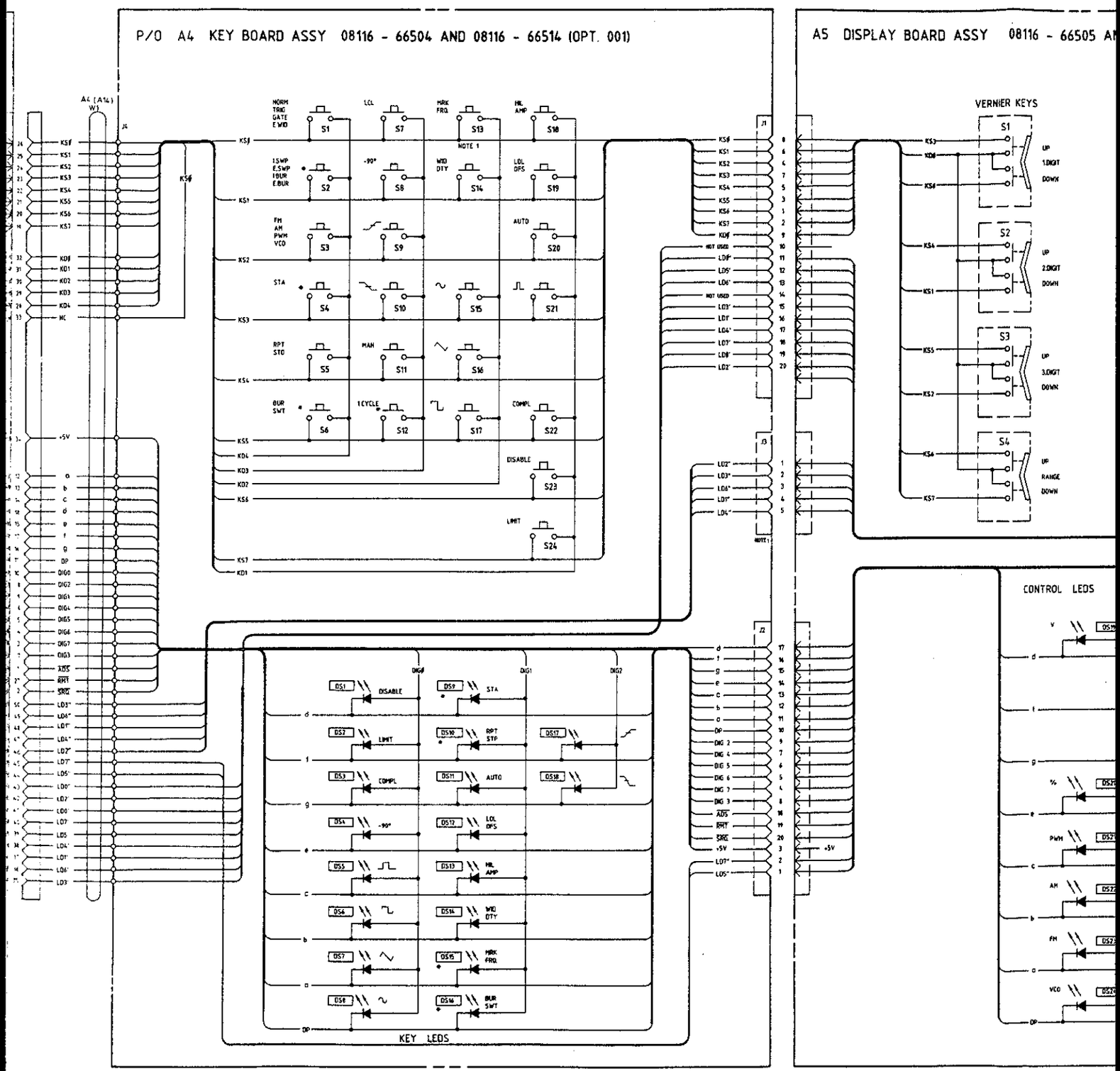
Device Bus Control Schematic
Sht 1 of 4



Device Bus Control Schematic
Sht 2 of 4

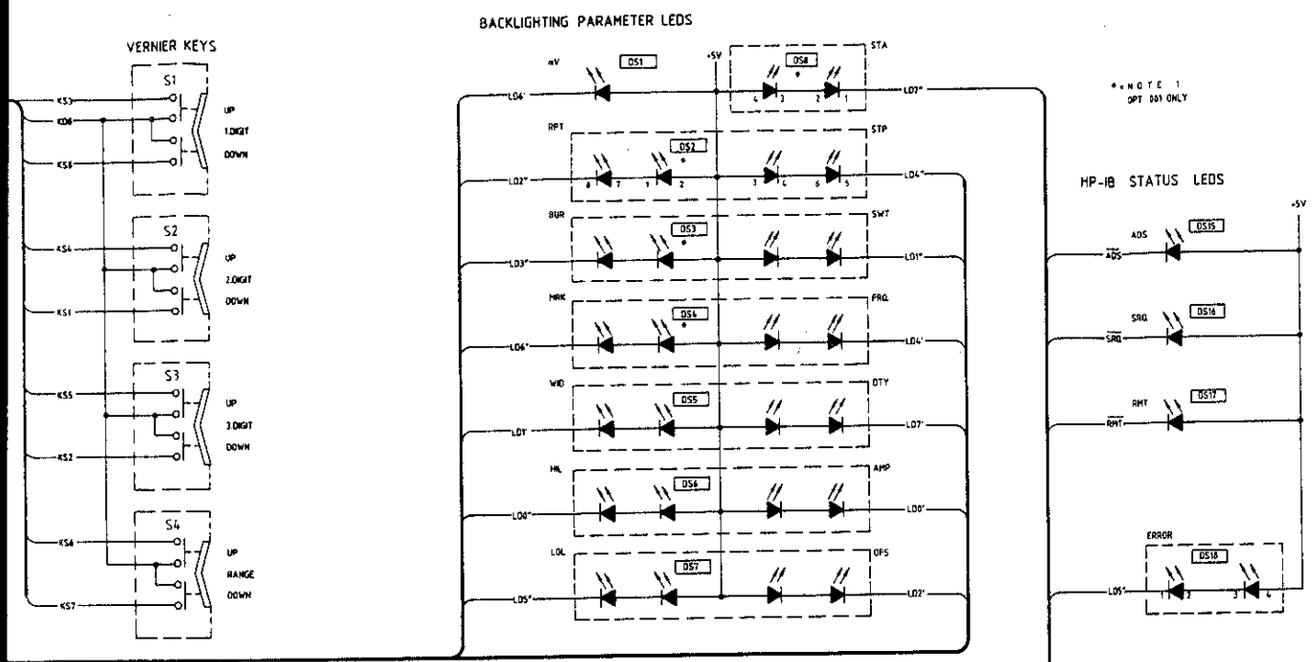


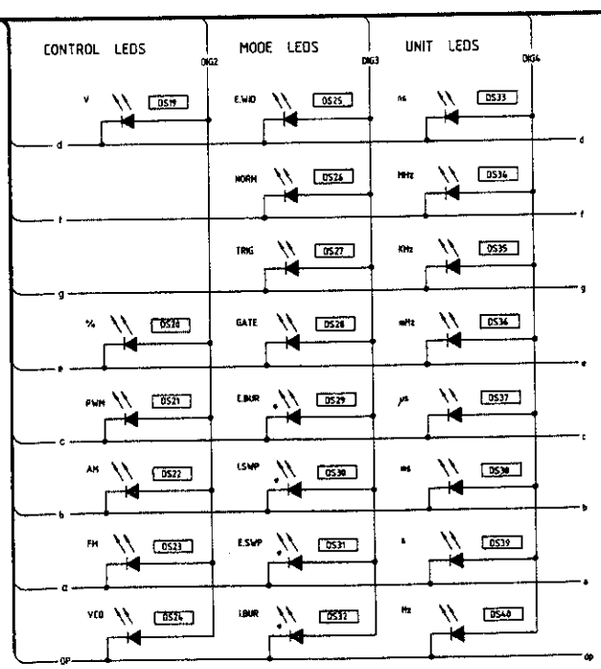
Device Bus Control Schematic
Sht 3 of 4

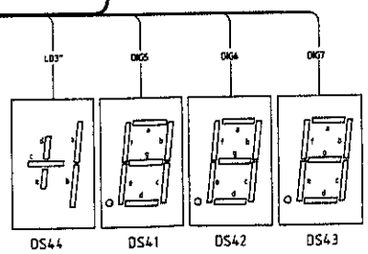


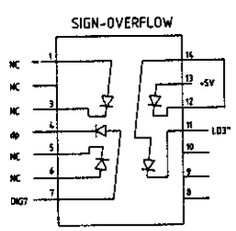
Device Bus Control Schematic
Sht 4 of 4

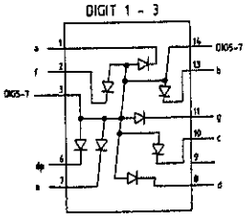
BOARD ASSY 08116 - 66505 AND 08116 - 66515 (OPT. 001)











DEVICE BUS CONTROL A3
KEY BOARD A4 , A14
DISPLAY BOARD A5 , A15

4

8-11d

SERVICE BLOCK 5

CONTROL THEORY OF OPERATION

Introduction

The 8116A Control section is located on A2 Control Board assembly. Power supplies to the board are via A1 Main board assembly and data and control signals are supplied from A3 MPU board assembly.

The Control section can be divided into specific areas and are discussed as follows:

Byte Offset latches and Offset DAC Timer.
Address Decoding.
Reference circuit.
D to A Converters.
Width Vernier Current Source.
Up and Down Current Source.
Capacitance Amplifier.

Byte Offset Latches and Offset DAC

Because it is necessary for the analog Amplitude and offset values to be available simultaneously, and because the Offset DAC has no internal latches, the high and low Byte Offset latches have been designed into the circuit discretely.

Data from the Latched Data Bus on the MPU Board A3 (see Schematic 4) arriving at U21 and U23 is latched through the devices on receipt of the negative going edge of $\overline{HBO}$ from decoder U14, and presented to latches U22 and U43. The data is further latched to the inputs of DAC U24 on receipt of the negative transition of SCA. The time difference between SCA (enabling the amplitude DAC) and $\overline{SCA}$ is merely the propagation delay through buffer U19.

The Offset DAC itself is a 12-bit multiplying device, providing two current outputs. Iout1 (pin 1) is active when any combination of the twelve digital inputs are high, and the summed currents derived from the reference voltage via selected R/2R networks are available at this point. Iout2 (pin 2) provides current from the remainder of the reference voltage via those R/2R networks which have not been selected (data inputs low). Thus, the algebraic sum of current derived from the reference voltage is equal to the sum of Iout 1 and Iout 2, where Iout 1 represents data inputs selected and Iout 2 represents data inputs not selected.

When Offset is selected by the operator at the instrument frontpanel, the resulting digital signal, derived from LD7 is used to enable the output of the Offset DAC via switch U17.

Note:
U17 on when ofs = 999 mV (for ampl. of = 100 mV)
= 99.9 mV (for ampl. of < 100 mV)

Timer

The IC which is responsible for this task is a standard type 555, and is configured to behave as an Astable multivibrator — dependent upon two different signals for free-run operation.

The logic signal arriving at pin 4 from NAND gate U40, is required to be high in order for the Astable to run. When this input is low, the timer is effectively inhibited. The other signal required is RESET, which also needs to be high.

The Timer output is at pin 3 ($\overline{NMI}$) — a signal required by the MPU to produce the flashing error display.

Address Decoding

Address Decoding is performed by U14 and U20. Address lines LA3, LA4 and LA5 from the MPU board comprise the input address to both decoders — the output line selected being dependent upon binary value of the input.

Reference Circuit

The −9 V reference voltage provides a constant current and is derived from a unity-gain inverting amplifier. The −9 V supply is used as a reference by the Amplitude, Offset and Width Vernier Current Source DAC's on the Control Board.

Digital to Analog Converters

Figure 8–5–1 shows three channels of a basic DAC. Switches A, B and C correspond to digital inputs – A being most significant, B the second significant and C third most significant. In the diagram the position of the switches is related to a logic high input, i.e. all three bits ON.

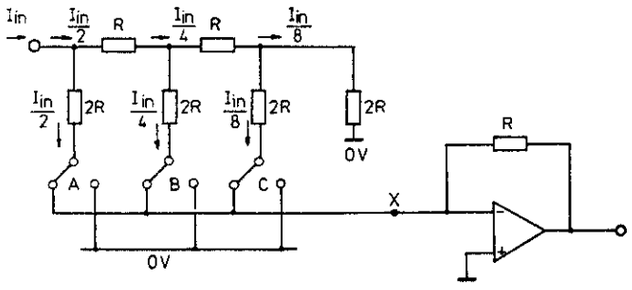


Figure 8–5–1. DAC – principle of operation

The total current Iin, which is derived from the reference voltage, is divided by a factor of two for each resistance path it meets. The currents are then summed at point X such that, in this case, the total current available is:

$$Iin/2 + Iin/4 + Iin/8 = 7/8Iin$$

By selecting any combination of the three digital inputs, output currents between 1/8Iin to 7/8Iin may be output. In practice, DAC's generally have 8, 10 or 12 digital inputs. In this case, the reference current is divisible by up to 256, 1024, and 4096 respectively.

When a logic low level is applied to an input, the current through that particular channel continues to flow, but to ground. The remainder of the current derived from the reference voltage is buffered and inverted before being passed on to the load.

The Control Board Amplitude and Frequency DAC's function in the above fashion.

To describe the operation of the remaining DAC's it is necessary to refer to Figure 8–5–2. As in the previous description, inputs are selected digitally, with each channel dividing the current to half the preceeding channel's value. The difference in the circuits is that in the second example, the output is a reciprocal value of the selected inputs. The currents being summed at the inverting input of the op-amp can be expressed as:

$$VA/2R + VA/4R + VA/8R = -Vref/R$$

therefore, $VA = -8/7Vref$

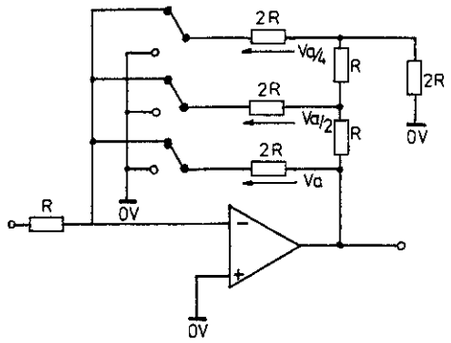


Figure 8–5–2. DAC – reciprocal operation

The Control Board Width Vernier Current Source and Duty Cycle DAC's function in the above manner.

Width Vernier Current Source

The operation of the DAC in this circuit is described above. The reciprocal output current is drawn through one of two resistance paths, selectable logically, and then passed to the Analog Decoder section of the Timing IC on Main Board Assy A1.

Up and Down Current Sources

Both current source outputs are dependent upon the Duty Cycle DAC outputs. The frequency DAC output, after being attenuated, provides the reference inputs for both Duty Cycle DAC's. DAC U8 output is directly proportional to the duty cycle selected, while U10 output is proportional to the difference between Period and Duty Cycle. Therefore, both outputs, if added together, represent the programmed period of the waveform selected.

The outputs of the Up and Down Current Sources obey the same rule. When a Duty Cycle of 50 % is selected both Source outputs will be identical. If, however, a duty cycle of 20 % is selected, the ratio of output currents will be 80 % to 20 % in favour of the Up Current Source. This apparent inversion ratio is due to the reciprocal output of the Duty Cycle DAC's. The requirement of the Slope Generator is such that for a short duty cycle, the ramp capacitor has to charge more quickly than for a long duty cycle. This being the case, more current is made available for a fast charge time than for a slower charge time.

Capacitance Amplifier

The operation of the capacitance Amplifier is best explained with the aid of Figure 8–5–3 and 8–5–4.

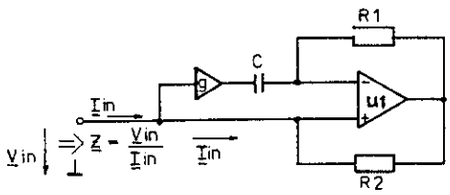


Figure 8–5–3. Simplified capacitance amplifier

Figure 8–5–3, illustrates a simplified capacitance amplifier circuit. U1 serves merely as a voltage amplifier. For the purposes of a basic description however, Figure 8–5–4 is provided.

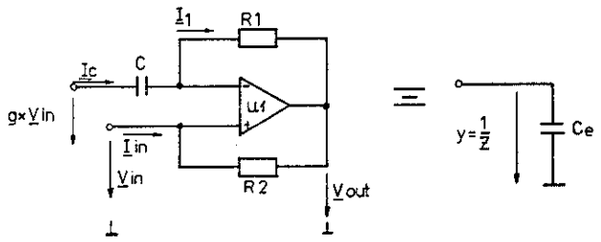


Figure 8–5–4. Formula derivation for capacitance amplifier

The capacitance amplifier is basically a circuit in which a capacitor's value may be increased or decreased in decade ranges. The effective capacitance may be represented by the Formula:

$$Ce = \frac{R1}{R2} (g-1)\ C.\ uF$$

Where R1 is the resistance in the negative feedback path, R2 is the resistance in the positive feedback path, g is the gain of the voltage amplifier and C is the value in microfarads of the circuit capacitor.
By varying the value of R1, the equivalent output capacitance will also vary.

In the instrument, the decade resistors are switched in to the circuit digitally via latch U3 and relays K1 to K4.

The amplifier output is passed to the Range Switching circuit on Main Board Assy A1 (see Service Block 6 for details).

SERVICE BLOCK 5 TROUBLESHOOTING GUIDE

NOTE: If an error code is shown in the display it is necessary to press a key, e.g. LCL, to set the u-Processor to normal routine, then troubleshoot the instrument.

Address Decoders Signature Analysis

The Timing and Output Address Decoders, which provide the logic control signals for all DACs on A2 Control Board Assy can be checked with Signature Analysis.

Set the u-Processor to free run mode by setting the jumper P1 to "P1" position on board A3. Disconnect jumper A2W2. Connect REST (A3) to gnd for a short time to reset the u-Processor.

Signature Analyzer	A3 u-Processor Board Assy
Start ⎍	TP "SA"
Stop ⎍	TP "SP"
Clock ⎎	TP "E"
⊥	⊥

Table 8–5–1. Signature Analyzer setting and connection to A3 u-Processor Board Assy

NOTE: Verify that reading at +5 V is 0003. If not, the u-Processor does not run free.

Check the signatures of U14, U19 and U20 against the readings given in the Table

Frequency Control

Frequency Range	COMP1	COMP0	U16 "ON" Channels
1.00 mHz – 99.9 Hz	H	L	15 –> 1, 4 –> 5
100 Hz – 9.99 MHz	H	H	15 –> 1, 4 –> 3
10.0 MHz – 50.0 MHz	L	L	15 –> 2, 4 –> 5

Table 8–5–3. Frequency Range Corrections

8116A Frequency Setting	Voltage at TP4 ± 10 %
1 kHz	–0.44 V
5 kHz	–2.20 V
9.99 kHz	–4.39 V

Table 8–5–4. Frequency DAC Output Voltages

Duty Cycle Control

Set 8116A:

FRQ . . . . . 9.99 kHz
Output . . . . . sine

8116A Duty Cycle	Voltage at TP5 ± 15 %	Voltage at TP6 ± 15 %
10 %	10.1 V	1.1 V
50 %	2.0 V	2.0 V
90 %	1.1 V	10.1 V

Table 8–5–5. Duty Cycle DACs Output Voltages

Width Control

Set 8116A:

FRQ . . . . . 1 kHz
Output . . . . . pulse

8116A Width Setting	Voltage at TP7 ± 10 %
10.0 us	9.9 V
50.0 us	2.0 V
99.9 us	1.0 V

Table 8–5–6. Width DAC Output Voltage

Width Range	COMP2	U17 "ON" Channel
10.0 ns – 99.9 ns	L	4 –> 5
100 ns – 999 ms	H	4 –> 3

Table 8–5–7. Width Range Correction

Amplitude Range	U17 pin 11	U17 "ON" CHANNEL
		pin pin
100 mV – 9.99 V	H	14 –> 13
10.0 V – 16.0 V	L	14 –> 12

Table 8–5–9. Amplitude DAC Gain Control

Amplitude Control

Set 8116A:

OFS . . . . . 000 mV

Amplitude Setting	Voltage at TP8 ± 10 %
1.00 V	3.96 V
5.00 V	2.20 V
9.99 V	< 15 mV
10.0 V	2.64 V
16.0 V	< 10 mV

Table 8–5–8. Amplitude DAC Output Voltage

Offset Control

Set 8116A:

AMP . . . . . 100 mV

Offset Setting	Voltage at TP9 ± 20 %	Offset DAC Input Data											
		Binary											Decimal
		Q	11	10	9	8	7	6	5	4	3	2	1	0	
+7.95 V	–7.35 V	0	0	0	1	1	1	0	0	1	0	1	0		458
+5.12 V	–4.70 V	0	1	0	0	0	0	0	0	0	0	0	0		1024
+1.00 V	–0.92 V	0	1	1	1	0	0	1	1	1	0	0	0		1848
+999 mV	–9.22 mV	0	0	0	0	0	0	1	1	0	0	1	0		50
+100 mV	–0.92 V	0	1	1	1	0	0	1	1	1	0	0	0		1848
+10 mV	–0.09 V	0	1	1	1	1	1	1	0	1	1	0	0		2028
000 mV	< 20 mV	1	0	0	0	0	0	0	0	0	0	0	0		2048
–10 mV	+0.09 V	1	0	0	0	0	0	0	1	0	1	0	0		2068
–100 mV	+0.92 V	1	0	0	0	1	1	0	0	1	0	0	0		2248
–999 mV	+9.22 mV	1	1	1	1	1	1	0	0	1	1	1	0		4046
–1.00 V	+0.92 V	1	0	0	0	1	1	0	0	1	0	0	0		2248
–5.12 V	+4.70 V	1	1	0	0	0	0	0	0	0	0	0	0		3072
–7.95 V	+7.35 V	1	1	1	0	0	0	1	1	0	1	1	0		3638

Table 8–5–10. Offset DAC Input Data and corresponding output voltages

NOTE: Q0 is only used when the result of $\frac{HIL - LOL}{2}$ is an odd number (0.5 mV correction)

Control
Sht 1 of 2

Offset Range	U17/Pin 10	U17 "ON" Channel
		pin pin
000 mV ± 999 mV	H	15 –> 1
± 1.00 V ± 8.95 V	L	15 –> 1

Table 8–5–11. 20 dB Offset Attenuator Control Signals

Capacitance Amplifier

Frequency Range	U3 pin 6	5	4	3	
1.00 mHz – 9.99 mHz	L	H	H	H	K4 on
10.0 mHz – 99.9 mHz	H	L	H	H	K3 on
100 mHz – 999 mHz	H	H	L	H	K2 on
1.00 mHz – 9.99 mHz	H	H	H	L	K1 on

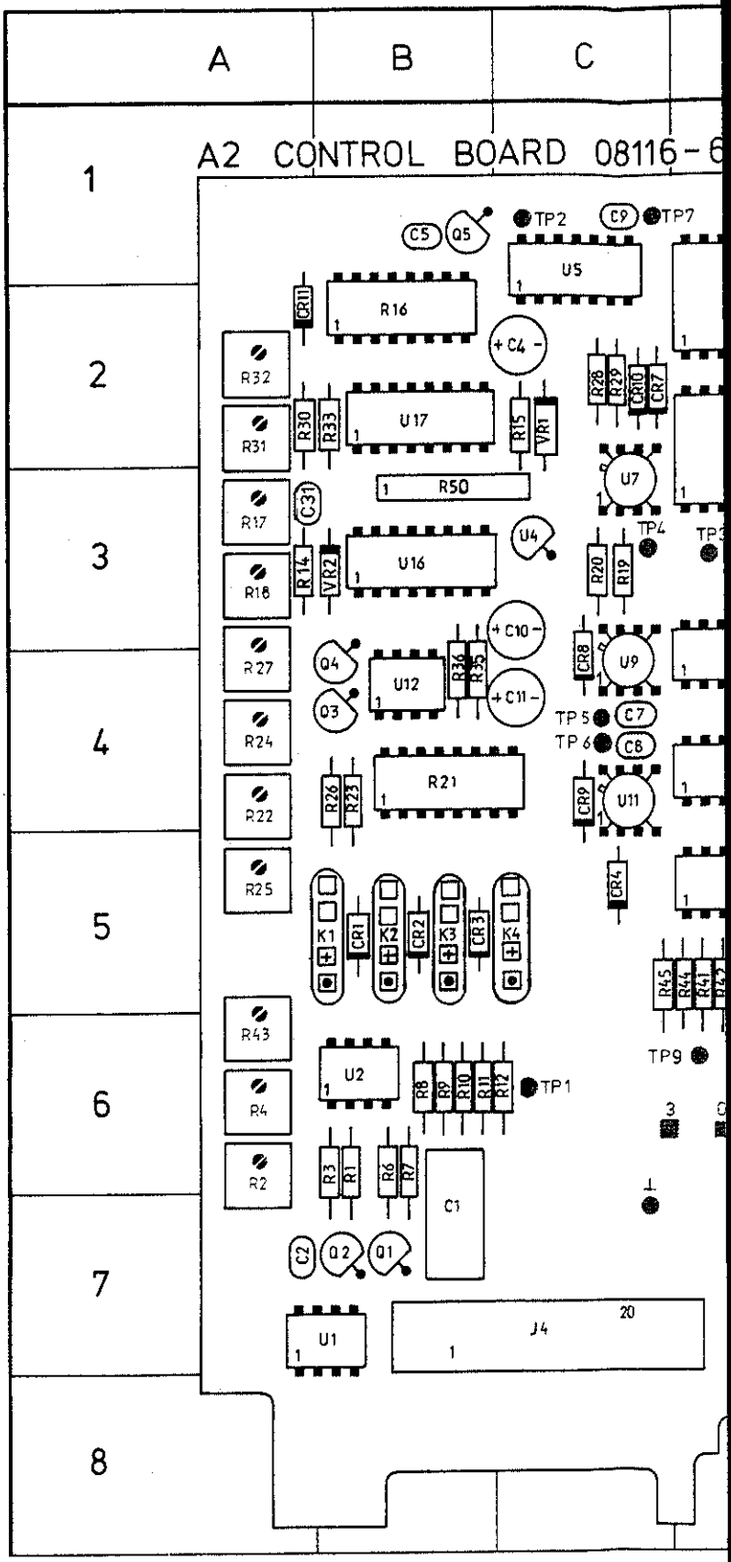
Table 8–5–12. Low Frequency Range Switching Truth Table

Timer

At any time an erroneous setting is made to the 8116A timer, input pin 4 goes high which causes the timer to generate an output signal of approx. 100 Hz.

This output signal interrupts the u-Processor and makes it jump to an error subroutine where the right error display is illuminated (flashing or constant).

Verify correct operation of U31 by setting 8116A to "E.WID" and "Sine". U31 pin 3 must deliver a signal with a frequency of approx. 100 Hz.

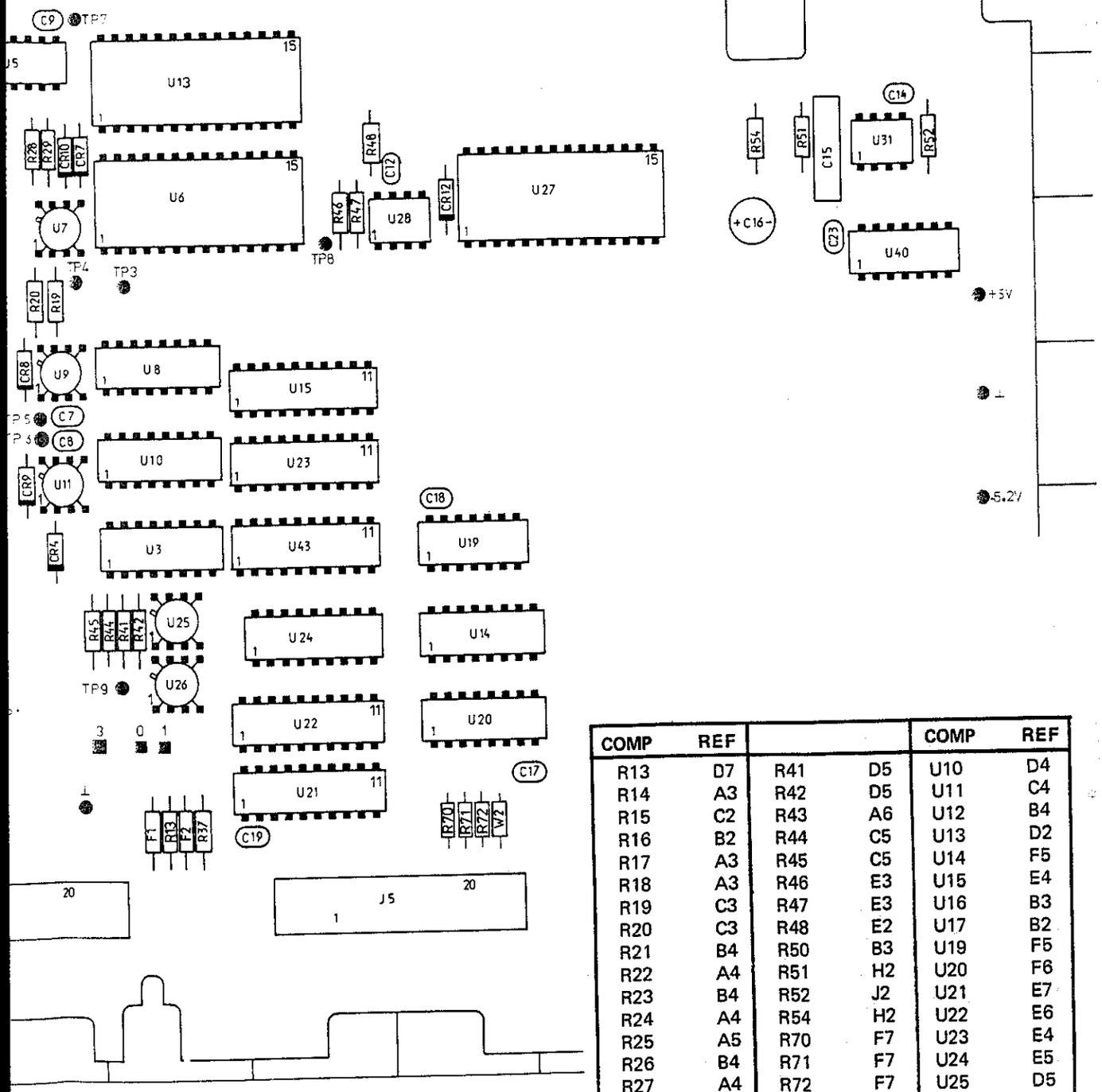


COMP	REF			COMP	REF			COI
C1	B7	C10	C3	C18	F5	CR7	C2	J5
C2	A7	C11	C4	C19	E7	CR8	C4	K1
C4	C2	C12	F2	C31	A3	CR9	C4	K2
C5	B1	C14	I2	CR1	B5	CR10	C2	K3
C7	C4	C15	I2	CR2	B5	CR11	A2	K4
C8	C4	C16	H3	CR3	B5	CR12	F3	Q1
C9	C1	C17	F6	CR4	C5	J4	C7	Q2

C | D | E | F | G | H | I | J

08116-66512

Control Sht 2 of 2



COMP	REF			COMP	REF
R13	D7	R41	D5	U10	D4
R14	A3	R42	D5	U11	C4
R15	C2	R43	A6	U12	B4
R16	B2	R44	C5	U13	D2
R17	A3	R45	C5	U14	F5
R18	A3	R46	E3	U15	E4
R19	C3	R47	E3	U16	B3
R20	C3	R48	E2	U17	B2
R21	B4	R50	B3	U19	F5
R22	A4	R51	H2	U20	F6
R23	B4	R52	J2	U21	E7
R24	A4	R54	H2	U22	E6
R25	A5	R70	F7	U23	E4
R26	B4	R71	F7	U24	E5
R27	A4	R72	F7	U25	D5
R28	C2	U1	B7	U26	D6
R29	C2	U2	B6	U27	G3
R30	A2	U3	D5	U28	F3
R31	A2	U4	C3	U31	I2
R32	A2	U5	C1	U40	I3
R33	B2	U6	D2	U43	E5
R35	B4	U7	C3	VR1	C2
R36	B4	U8	D4	VR2	A3
R37	D7	U9	C4	W2	F7

	COMP	REF			COMP	REF
	C2	J5	F7	Q3	B4	R6	B6
	C4	K1	B5	Q4	B4	R7	B6
	C4	K2	B5	Q5	B1	R8	B6
0	C2	K3	B5	R1	B6	R9	B6
1	A2	K4	C5	R2	A6	R10	B6
2	F3	Q1	B7	R3	B6	R11	B6
	C7	Q2	B7	R4	A6	R12	C6

8-13C

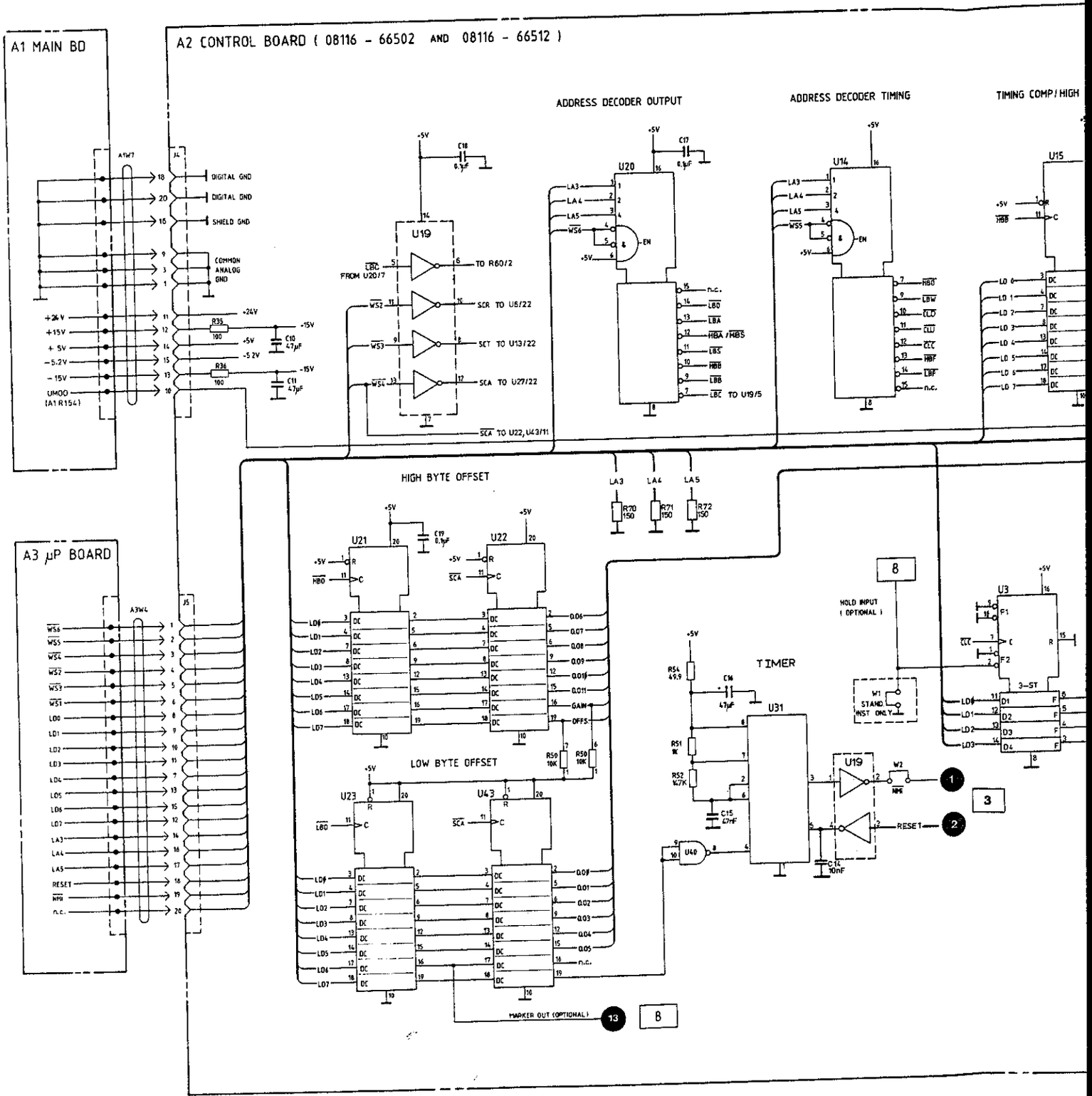
Logic Signals – Mnemonics – Description – Signatures

Area	Mnemonic	Description	Free Run Signatures
Frequency DAC U6	$\overline{SCR}$ $\overline{LBF}$ $\overline{HBF}$ LD0–LD7	Freq. Data Load signal Low Byte Frequency High Byte Frequency Frequency Data	PU9A PIOH F49I
Duty Cycle DAC U8	$\overline{CLU}$ LD0 – LD7	Iup – Data Load Signal Iup – Data	58F8
Duty Cycle DAC U10	$\overline{CLD}$ LD0 – LD7	Idown – Data Load Signal Idown-Data	7IPO
Width DAC U13	$\overline{SCT}$ $\overline{LBW}$ $\overline{HBF}$ LD0 – LD7	Width Data Load Signal Low Byte Width High Byte Width Width – Data	79HF OF4F F49I
Capacitance Ampl. Control U3	$\overline{CLC}$ LD0 – LD7	Low Frequency Range Data Load Signal Low Frequency Range Data	27A6
Amplitude DAC U27	$\overline{SCA}$ $\overline{LBA}$ $\overline{HBA}$ LD0 – LD7	Amplitude Data Load Signal Low Byte Amplitude High Byte Amplitude Amplitude Data	55F7 O4H5 5O8P
Offset Latches U21, U22, U23, U43	$\overline{SCA}$ $\overline{LBO}$ $\overline{HBO}$ LD0 – LD7	Offset Data Load Signal Low Byte Offset High Byte Offset Offset Data	55F4 8UP5 F2F2

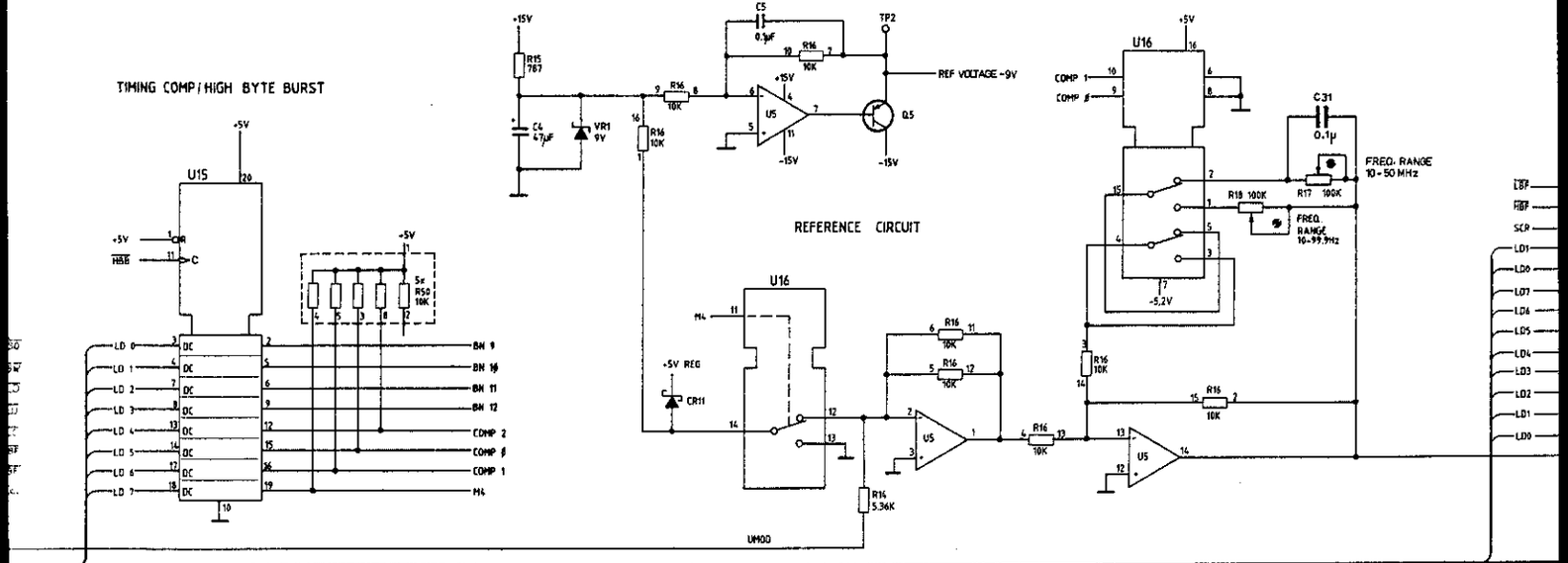
Table 8–5–2

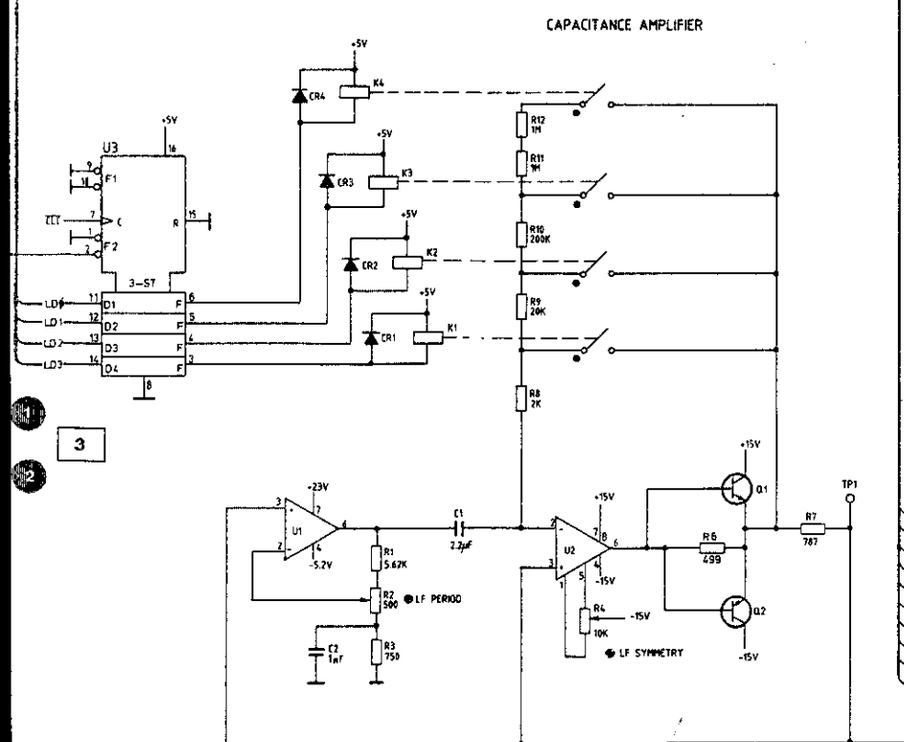
Pin No.	U14	U19	U20
1	P50H		P50H
2	CH9U		CH9U
3	8759		8759
4	8U95		IFH6
5	8U95	FU39	IFH6
6		FU3A	
7	F2F2		FU39
8		79HF	
9	0F4F	79HU	H456
10	7IP0	PU9A	IIAF
11	58F8	PU99	8392
12	2786	55F7	508P
13	F49I	55F4	04A5
14	PIOH		8UP5

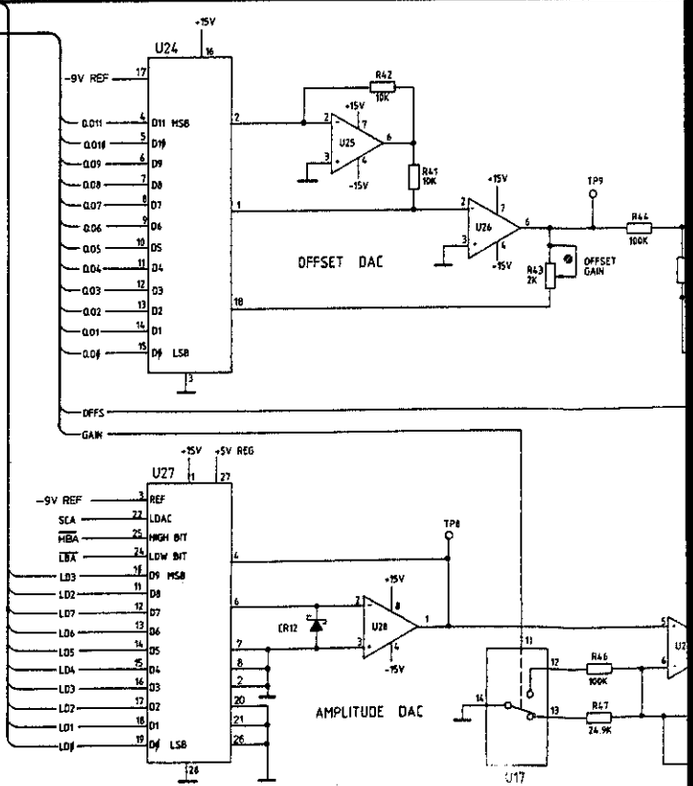
Control Schematic
Sht 1 of 4



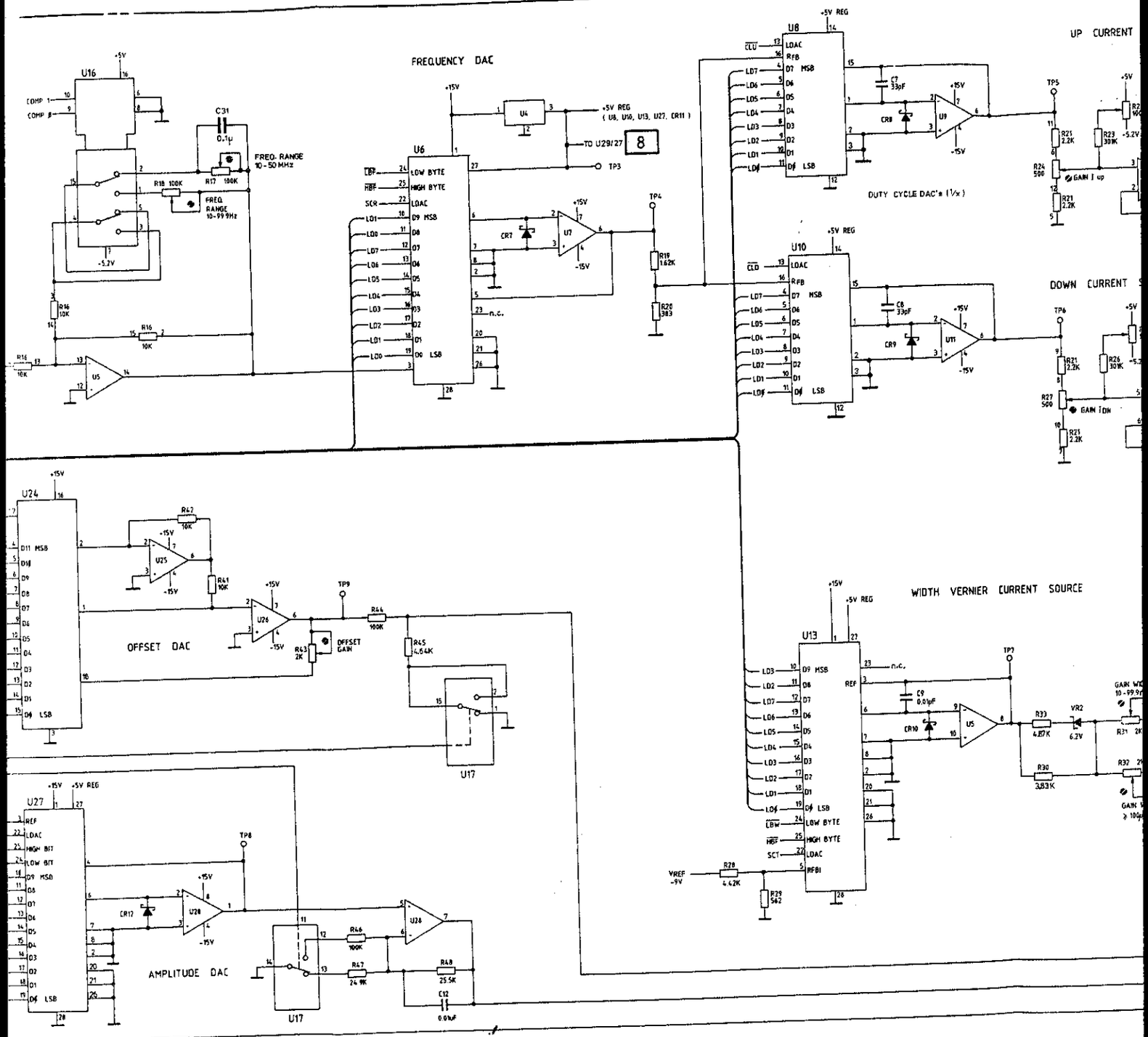
Control Schematic
Sht 2 of 4



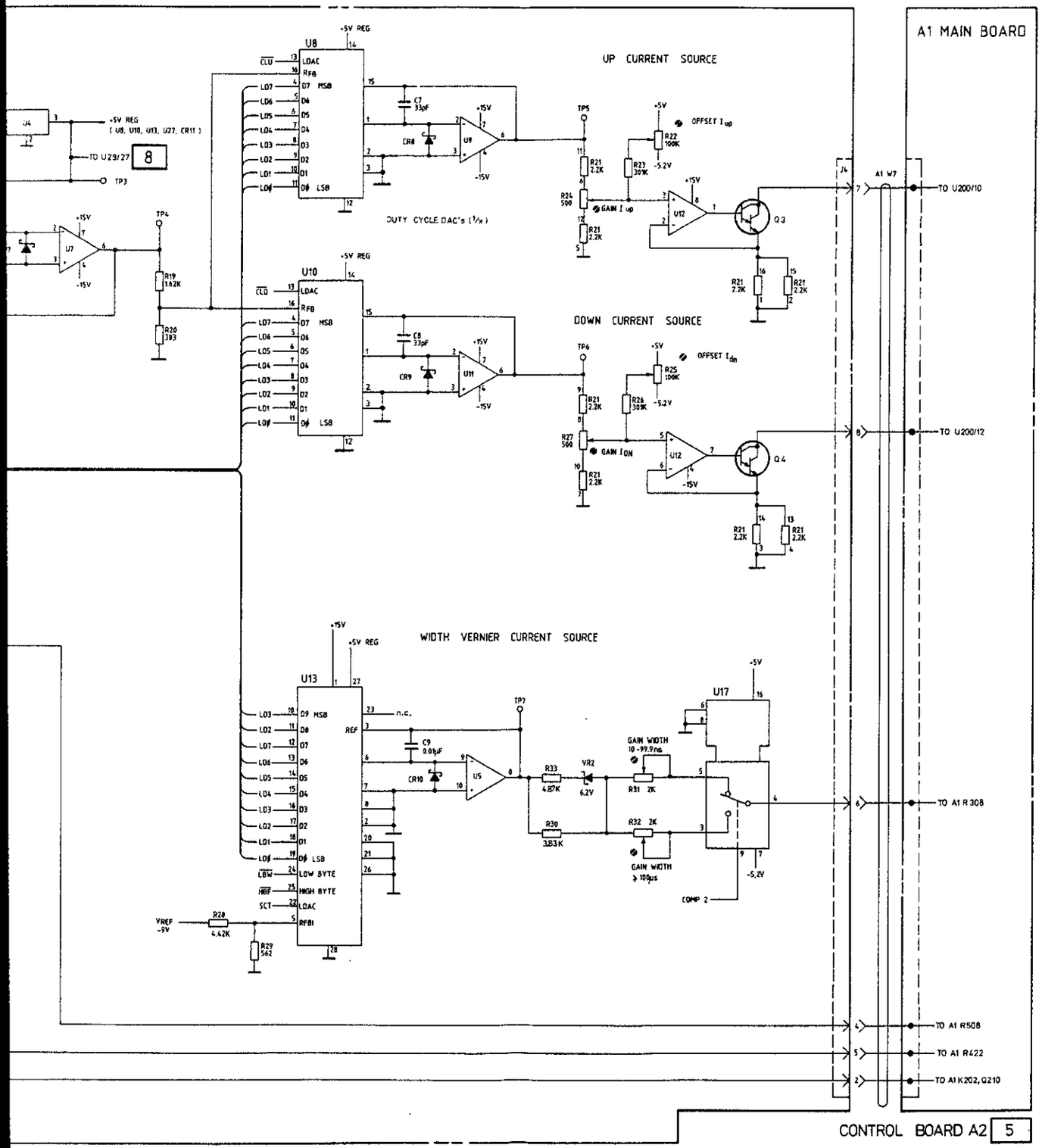




Control Schematic
Sht 3 of 4



Control Schematic
Sht 4 of 4



8-13e

SERVICE BLOCK 6

VCO, WIDTH GENERATOR THEORY OF OPERATION

General

The bulk of the Slope Generation and Timing circuitry is to be found on the Main Board A1 Assy. A small part is also located on Control Board A2 Assy.

The Overall operation may be generally divided into the following functions:

1. Trigger Input Circuits
2. Control Input Circuits
3. Slope Generator IC
4. Timing IC
5. Error Feedback and Vernier Feedback

1. Trigger Input Functions

There are three distinct trigger input functions.

The first stage (Trigger Level Circuit) receives both the trigger input and trigger level adjust directly from the instrument frontpanel, and is designed to provide the required trigger level to the second stage without imposing it on the trigger input signal (thereby not disrupting the trigger source). Figure 8–6–1 shows the principle of operation of the circuit. Op-Amp U101A is configured to provide a fixed voltage source of –1.25V, and U101B is an inverting amplifier of unity gain used to provide a voltage of equal magnitude but opposite polarity to the level selected.

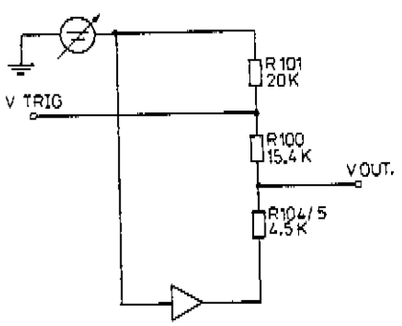


Figure 8–6–1. Trigger input circuit simplified

By varying the voltage across the divider chain, the DC component (or DC shift) of Vout will change accordingly. Vout is now passed through high-to-low impedance converter Q100/Q101 and on to the second trigger output function. The trigger input amplifier is a three-stage ECL circuit with Schmitt trigger characteristics. Each operational amplifier stage has a main and complementary output – both of which are pulled down to –5.2 V via a 470 Ohm resistor. The circuit feedback resistor (R113) provides a hysteresis path to the input in order to overcome any noise which may be present. The threshold of this Schmitt Trigger circuit is fixed at –1.3 V. The third trigger input function is a wired-OR configuration for trigger slope/MAN selection. INT BURST or MAN selection at the frontpanel results in the Trigger Mode Latch U103 outputting a TTL high to one of four ECL NOR gates via the TTL/ECL converter R116/R117/R118. In the wired-OR configuration, a logic high prevails (logic low is, in fact, a high impedance output stage). Auto Vernier FF U203 is clocked by this high-going signal, eventually providing an Auto Vernier Feedback signal, after having been reset as a result of Auto Vernier selection at the frontpanel.

2. Control Input Circuits

The control input signal from the instrument frontpanel is routed to the Main Board A1 Assy. The circuit input has voltage protection diodes CR151 and CR152 to clamp incoming levels outside the ± 15 V window. Operational amplifier U151 is configured as a unity-gain, non-inverting buffer – the output being limited within a –5.2 V to +5 V window – which provides the input to the Control Mode Selector U152. Frequency and Amplitude Modulation, Pulse Width Modulation and Voltage controlled oscillator modes are selected via logic signals M1 and M2 at U152. For FM mode, the control signal is output from U152 pin 14. VCO mode control signal is output at pin 12, and PWM control signal at pin 4 (via pin 11). When AM has been selected, U152 pin 13 becomes earthed via pin 15, and U151 output is processed by the Amplitude modulator. See Service Block 7.

The PWM control signal is passed from the selector directly to the Timing IC (U300), which is used as a width generator. Further information about this IC appears in this Service Block.

The VCO and FM control signals are discussed further in Service Block 5.

3. Slope Generator IC (U201)

The Slope Generator here functions as triangle waveform generator up to 50 MHz. The signal generation may be free-running, gated or triggered. A special burst control input – Burst control – (pin 2) permits a counted number of pulses to be generated on receipt of a trigger signal derived from the Burst Counter on A2 Control Bd Assy. Figure 8–6–2 shows a block diagram of the Slope Generator IC.

Generation of the triangular waveform is achieved by charging and discharging a ramp capacitor with constant current. External current sources are used for this task.

Current sources

For repetition rate generation, the Slope Generator I.C. relies upon the Ramp Current Source for charging a range capacitor (internally or externally), and Idn REF for discharging.

The ramp current source is derived from Iup REF, and passed through complementary transistors Q203 and Q204. While charging, current is drawn through Q203 – under control of the internal buffer. When the capacitor charge threshold has been attained Q203 is switched off, ramp current is dumped to ground via Q204 and the capacitor discharged through I dn REF. This principle applies to variable Duty cycles. Iup REF is utilised when variable start phase has been selected in TRIG, GATE or BURST mode. The level at which the capacitor begins to charge is fixed by two clamping diodes acting upon a voltage at pin 11.

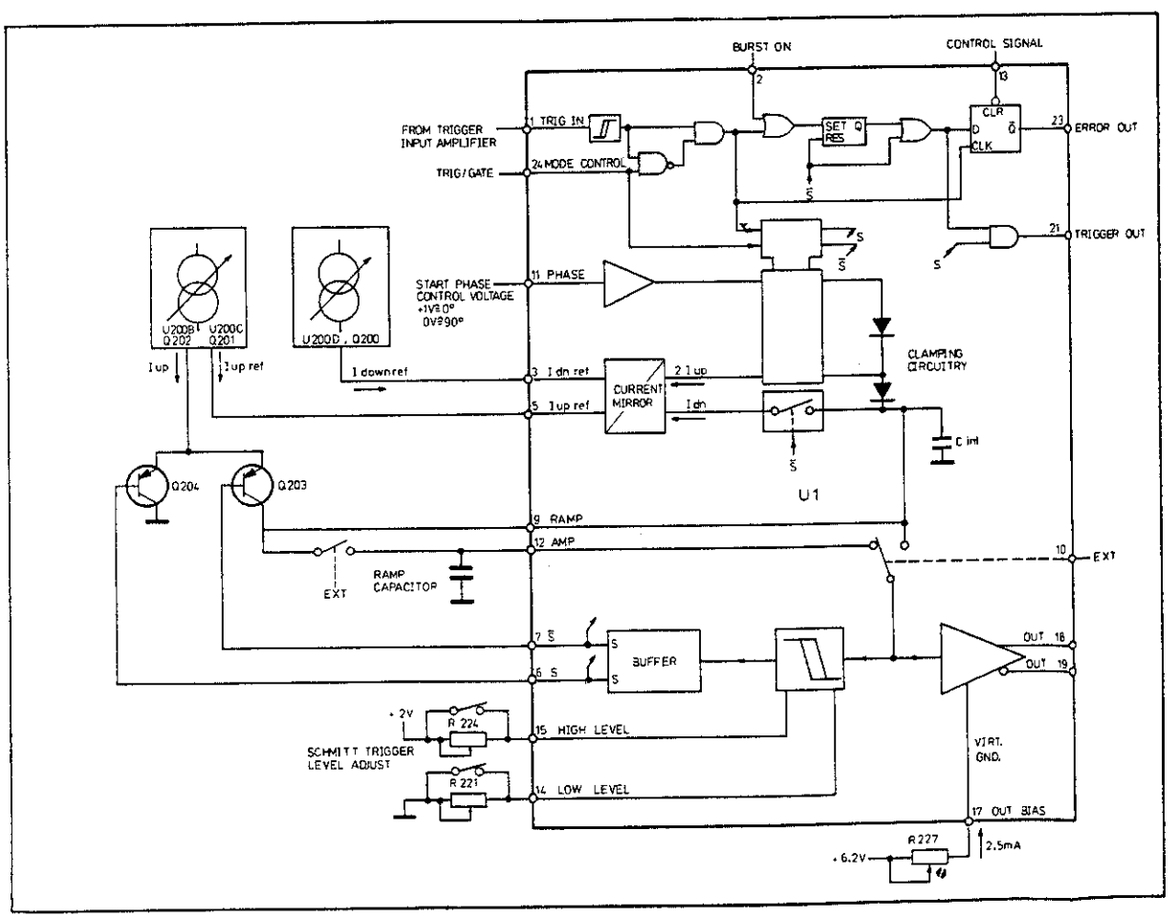


Figure 8–6–2. Slope Generator block diagram

This voltage is derived from the Reference circuit and has a different value for each start phase. Iup REF has no effect when the instrument is in Normal mode. Table 8–6–1 shows the relationship between clamped voltage and start phase.

Pin 11	start phase
0 V	–90°
1 V	0°

Table 8–6–1.

The current source is required to sink 2xIup (Phase voltage source pin 11, and Iup REF) in order to balance the two clamping diodes during the time when the oscillator is not running e.g. between gate signals.

In the external range switching circuit, current values are variable by up to a factor of 100, and the capacitors arranged in parallel decade multiples (digitally controlled from Range Latch U210). Frequencies from 1 mHz to 1 MHz with variable duty cycles from 10 % to 90 % are possible. For frequencies less than 10 Hz a special capacitance amplifier is necessary to provide the high capacitance values which are needed for very low frequency generation. The function of this capacitance amplifier is described in Service Block 5.

Schmitt Trigger

The Slope Generator IC has a Schmitt Trigger which controls the switching of analog circuitry within the device.

The upper and lower switching thresholds for the Schmitt Trigger are defined externally in the High and Low level adjust circuits. The actual threshold voltage will depend upon the state of switches U205.

A reference voltage of 6.2 V is divided down to approximately 1.9 V, then passed to U202A. Switch U205 is digitally controlled from Range Latch U210, its wiper position being dependent upon the frequency range selected. Table 8–6–2 shows the relationship between frequency ranges and Range Latch data to U205.

EXT	R3	Range
1	0	1 mHz – 999 kHz
1	1	1 MHz – 9.99 MHz
0	1	10 MHz – 50 MHz

Table 8–6–2. Relationship between frequency and latch data

The resulting voltage is passed to the Schmitt Trigger as the high level threshold. The low level threshold is derived in the same way as above with the exception of the reference voltage being 0 V in this case.

The values of the currents drawn by the Schmitt Trigger are always proportional to the Iup REF value in order to compensate for propagation delays encountered in the Schmitt trigger and current switching circuits.

In Burst mode, a selectable number of triangles or square-waves are generated at the I.C. output, the selected number being loaded into a counter (see Service Block 8 for details). The counter consists of 11 stages to enable selection of any number between 1 and 1999. Upon the burst start trigger, the counter, having been pre-loaded, counts down to 1. The value "1" is used to detect burst completion to generate a disable signal, which together with the last oscillator output pulse disables the gate input and reloads the burst number into the counter. The next burst cycle is then triggerable almost immediately.

Figure 8–6–3 shows the relationship between external triggering and start phase.

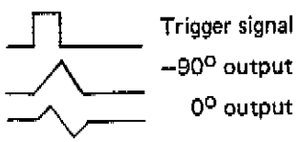


Figure 8–6–3a

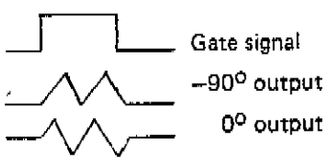


Figure 8–6–3b

Error output

The Error output of the Slope Generator I.C. is used only for instrument self-test purposes.

4. Timing IC

The Timing IC performs three distinct functions:

a. Triggerable pulse width generator.
b. Pulse Width Modulation as a result of an external control input (at the instrument frontpanel).
c. A trigger source for the Internal Burst mode.

The various operating modes for the IC are designated TIME, $\overline{\text{RATE}}$ and PWM.

In TIME mode the width of the output pulse is variable over 8 decades between 10 ns and 999 ms (see Table 8–6–3). Analog control within each decade is achieved by varying the FREQ IN current at pin 4. Control current is derived from the Width DAC on bd A2. In $\overline{\text{RATE}}$ mode the output frequency is variable over 8 decades from 1 Hz to 100 MHz. However, the fastest range is not fully utilised. To understand the method of frequency division in the IC it is necessary to refer to the block diagram. It will be seen that, in addition to a 6 decade counter, there is an analog divide-by-5 current attenuator and a flip-flop (divide-by-2). The control current from the Width Vernier Current DAC on bd A2 is varied at the FRQ IN port at pin 4.

Because FRQ IN and TIME IN are virtual ground inputs, a voltage source and series resistor provide the external current.

The approximate value of current taken in each of the input modes is shown in table 8–6–3.

	REF CURRENT	FRQ IN	TIME IN
$\overline{\text{RATE}}$ mode	~ 80 uA	2 mA – 0.2 mA	0.2 mA const
TIME mode	~ 80 uA	2 mA – 0.2 mA	0.2 mA const
PWM	~ 80 uA	2 mA const	2 mA – 0.2 mA

Table 8–6–3. Mode/Current relationship

Note that the first input stage performs an IFRQ/ITIME function.

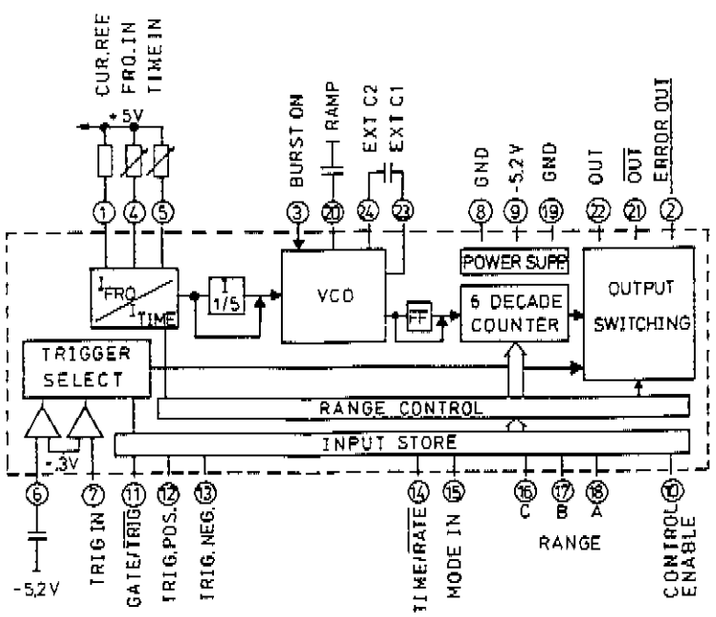


Figure 8–6–4. Timing I.C. block diagram

8-14d

The VCO operates in 2 ranges. In TIME mode the ranges are 10 ns to 99.9 ns and 50 ns to 500 ns.

In $\overline{\text{RATE}}$ mode the ranges are 100 MHz to 10 MHz and 20 MHz to 2 MHz. For all lower ranges in each mode, the 6-decade counter is used.
Table 8–6–5 illustrates frequency range selection.

The Timing IC has a built-in input store which is fed digitally by 8 Mode and Range select lines from the A3 uP board.

Taking these inputs in numerical pin sequence, their functions are as follows:

Pin No.	Signal	Function
10	$\overline{\text{WS3}}$	Control Enable. A TTL positive-going edge on this pin latches all digital information into the input store.
11	LD7	These three inputs determine the Timing IC trigger modes.
12	LD6	
13	LD5	
14	LD4	Mode select (TIME, RATE). See Table 8–6–4.
15	LD3	
16	LD2	Range selection, Width in Time mode and Frequency in Rate mode. See table 8–6–5 for details.
17	LD1	
18.	LD0	

TIME	MODE IN	MODES	OUTPUT
0	0	RATE	RATE
0	1	NOT USED	
1	0	TIME	TIME
1	1	NOT USED	

Table 8–6–4. Mode selection truth table

The output switching block of the Timing IC provides three signals, two of which are differential open collector outputs (OUT at pin 22 and $\overline{\text{OUT}}$ at pin 21). The two differential open collector outputs have fixed risetime and current amplitude of 12 mA. The third output signal is the ERROR OUT signal at pin 12, which indicates a timing error if a trigger signal occurs before the previously begun event has been completed (see Figure 8–6–5). Also, the Error Output is used during self-testing. The ERROR OUT port is an open collector configuration with fixed current swing.

5. Error Feedback and Vernier Feedback

These are two sources of error in circuits covered by this service block. The first is the WIDTH ERROR signal from the Timing IC-previously mentioned in (4). The second error is VCO ERROR, which is output from the Slope Generator IC at pin 23 when the circuit is triggered before the previously begun cycle is completed. VCO ERROR is utilised only for instrument Self-Test purposes and is software controlled.

Both error signals, at source, are ECL. Transistors Q302 and Q303, diodes CR301 and CR302 and resistors R118 and R129 make the error signals TTL compatible before they perform a Set function on Flip-Flops U301A and U301B. The Flip-Flop outputs are then gated with $\overline{\text{RSA}}$ before being put on the data bus.

The Auto Vernier feedback signal which accomplishes the Auto Vernier function is derived from the Trigger circuitry and also made TTL compatible before being output to the data bus.

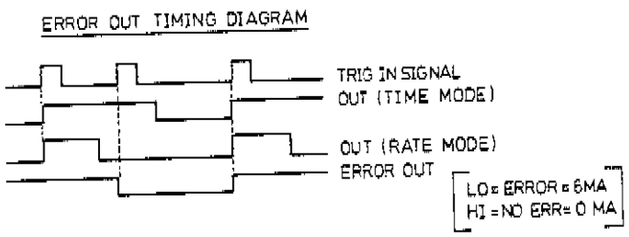


Figure 8–6–5. Error output waveforms

RANGE #	RANGE C	RANGE B	RANGE A	OUT FREQ IN RATE MODE	OUT WIDTH IN TIME MODE
0	0	0	0	$10^{7} - 10^{8}$ Hz	$10^{-8} - 10^{-7}$ sec
1	0	0	1	$10^{6} - 10^{7}$ Hz	$10^{-7} - 10^{-6}$ sec
2	0	1	0	$10^{5} - 10^{6}$ Hz	$10^{-6} - 10^{-5}$ sec
3	0	1	1	$10^{4} - 10^{5}$ Hz	$10^{-5} - 10^{-4}$ sec
4	1	0	0	$10^{3} - 10^{4}$ Hz	$10^{-4} - 10^{-3}$ sec
5	1	0	1	$10^{2} - 10^{3}$ Hz	$10^{-3} - 10^{-2}$ sec
6	1	1	0	$10^{1} - 10^{2}$ Hz	$10^{-2} - 10^{-1}$ sec
7	1	1	1	$10^{0} - 10^{1}$ Hz	$10^{-1} - 10^{0}$ sec

Table 8–6–5. Range selection

Control Mode	M3	M2	M1
off	L	H	L
FM	L	L	H
AM	H	H	L
PWM	L	H	H
VCO	L	L	L

Control mode truth table

Freq. Range	Frequency	EXT	$\overline{EXT}$	R3	R4	R5	R6	R7	LFR
1	10.0 MHz – 50.0 MHz	L	H	H	H	H	H	H	H
2	1.00 MHz – 9.99 MHz	H	L	H	H	H	H	H	H
3	100 kHz – 999 kHz	H	L	L	H	H	H	H	H
4	10.0 kHz – 99.9 kHz	H	L	L	L	H	H	H	H
5	1.00 kHz – 9.99 kHz	H	L	L	L	L	H	H	H
6	100 Hz – 999 Hz	H	L	L	L	L	L	H	H
7	10.0 Hz – 99.9 Hz	H	L	L	L	L	L	L	H
8	1.00 Hz – 9.99 Hz	H	L	L	L	L	L	L	L
9	100 mHz – 999 mHz	H	L	L	L	L	L	L	L
10	10.0 mHz – 99.9 mHz	H	L	L	L	L	L	L	L
11	1.00 mHz – 9.99 mHz	H	L	L	L	L	L	L	L

Table 8–6–5 (A) Range selection

Waveform	Mode	WF2	WF1
∿,⩘,⎍	I, BUR	L	L
∿,⩘	all, except E.WID	L	H
⩘,⎍	all, except E.WID	L	H
⎍	E.WID	H	L
⎍	all, except E.WID	H	H

Table 8–6–6. Logic signals information

VCO TROUBLESHOOTING

8116A Setting:

MODE . . . . . NORM
OUTPUT . . . . . sine
FRQ . . . . . 1.00 kHz
DTY . . . . . 80 %

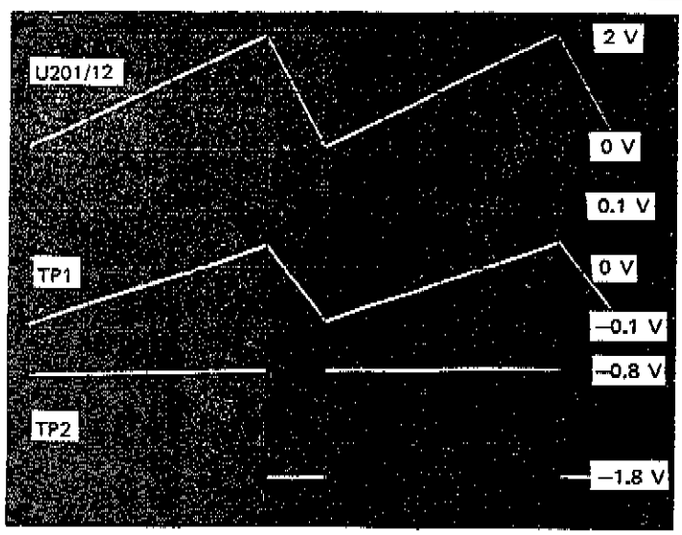


Figure 8–6–6. VCO Input and Output Signals

NOTE: Signal at TP1 may not necesarily be symmetrical.

Schmitt Trigger Low and High Levels

For frequencies to 999 kHz, the Schmitt trigger levels are set at 0 V for the low level (U201 / pin 14) and +2 V for the high level (U201 / pin 15).

If the levels are incorrect, disconnect U201 from its socket and recheck voltages at socket pin 14 and 15.

To disconnect U201 turn instrument off. When instrument is turned on again with disconnected U201, error E21 occurs in the display. Press LCL key to set 8116A to normal operation routine.

Check analog switch U205 against table 8–6–7.

Frequency Range	R3	EXT	"ON" Channels			
			pin	pin	pin	pin
1.00 mHz – 999 kHz	L	H	2 –>	3	15 –>	13
1.00 MHz – 9.99 MHz	H	H	4 –>	3	11 –>	13
10.0 MHz – 50.0 MHz	H	L	5 –>	3	14 –>	13

Table 8–6–7. U205 truth table

Iup Current Source (U200B, Q202)

Set 8116A:

MODE . . . . . NORM
FRQ . . . . . as required
DTY . . . . . 50 %

Connect a current meter between U201 pin 9 and ground Check values against table 8–6–8.

FRQ	Current ± 10 %
1.00 kHz	0.165 mA
5.00 kHz	0.830 mA
9.99 kHz	1.650 mA

Table 8–6–8. Iup-, Iupref- and Idnref currents (50 % Duty Cycle)

Iup ref Current Source (U200C, Q201)

Iup ref current is used to provide the start phase clamping in Trigger, Gate and Burst Modes.

It may only be checked when U201 is disconnected from its socket (same setting as for Iup Current Source).

For disconnection of U201 turn instrument off. When instrument is turned on again with disconnected U201, error E21 occurs in the display. Press LCL key to set 8116A to normal operation routine.

Connect current meter between U201 socket pin 5 and ground. Check current values against table 8–6–8.

Idn ref Current Source (U200D, Q200)

Same procedure as above.
Connect current meter between U201 socket pin 3 and ground.

WIDTH Generator – Troubleshooting

8116A Setting:

MODE . . . . . NORM
OUTPUT . . . . . pulse
FRQ . . . . . 100 kHz
WID . . . . . 6.00 us

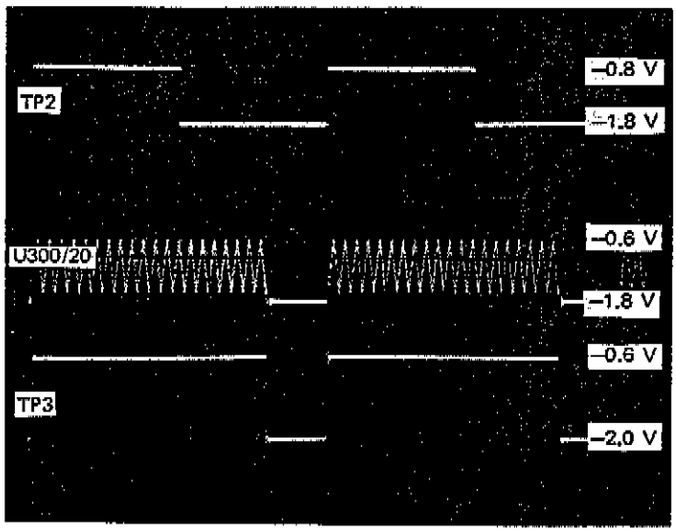


Figure 8–6–7. Width Generator Input and Output Signals

NOTE: When measuring at U301 pin 20, width may change due to the capacitance of the probe.

WIDTH Vernier Current

The width vernier current can be checked by measuring the voltage at R308/C303. (Table 8–6–9).

Set 8116A:

MODE . . . . . NORM
OUTPUT . . . . . pulse
FRQ . . . . . 1.00 kHz
WID . . . . . as required

Width	Voltage at R308/C303 min	max.
10.0 us	80 mV	180 mV
99.9 us	1.16 V	1.80 V

Table 8–6–9.

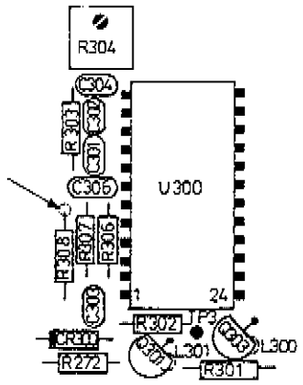


Figure 8–6–8. Width Vernier Control Voltage

Verify that voltage at U301 pin 4 is held at virtual ground (min. –40 mV; max. 0 mV). Verify that also U301 pin 1 and U301 pin 5 are at virtual ground (min. –40 mV; max. 0 mV).

Trigger Level Circuit/Input Amplifier

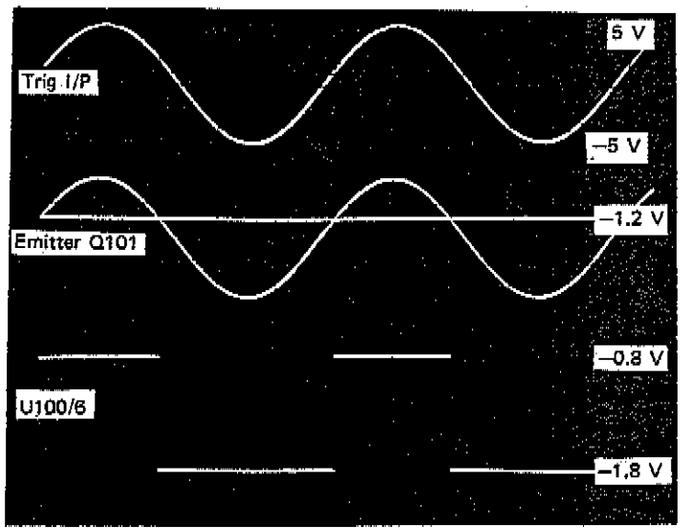


Figure 8–6–9. Trigger Input Amplifier Signals

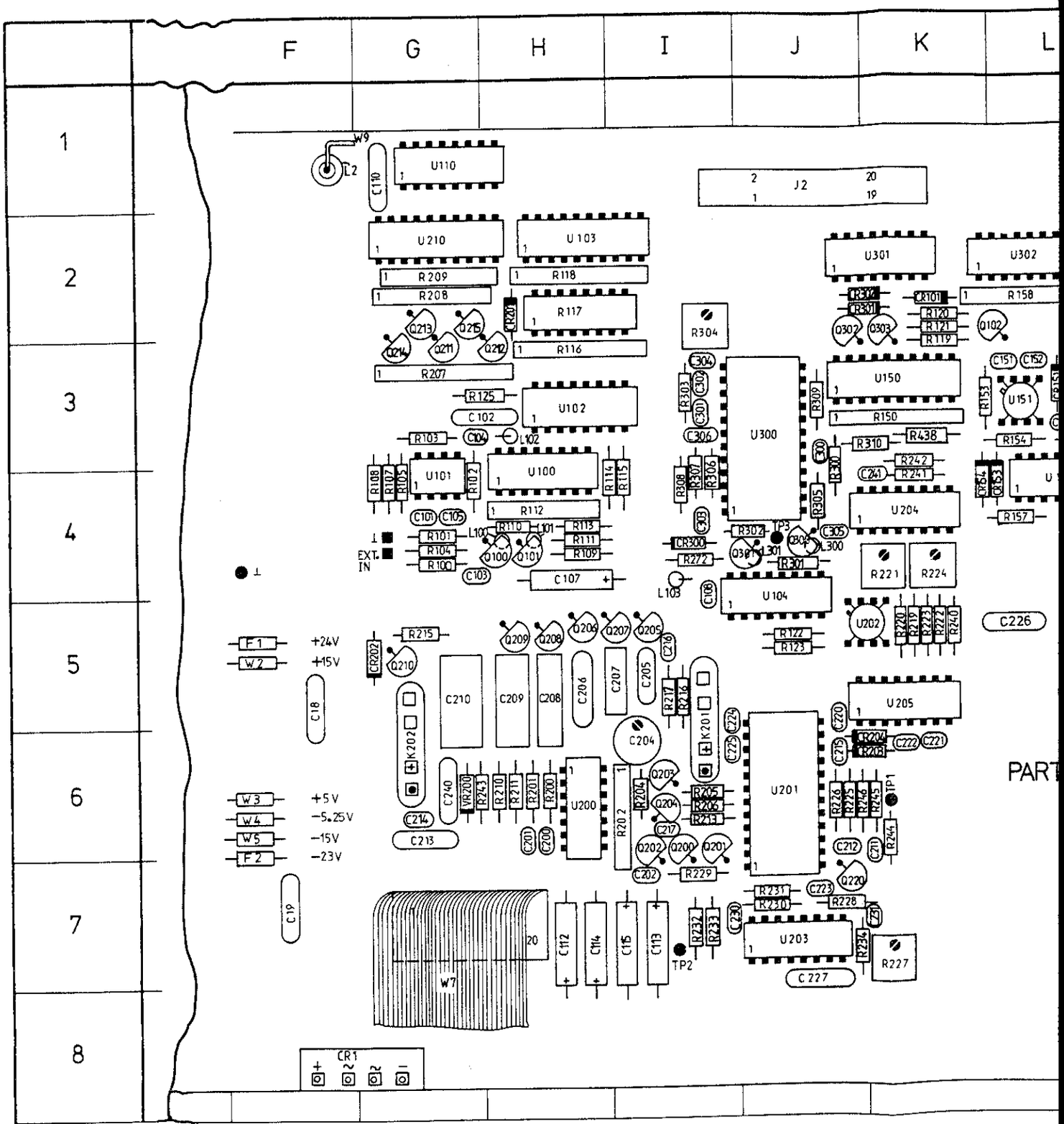
TROUBLESHOOTING GUIDE

NOTE: If an error code is shown in the display it is necessary to press a key, e.g. LCL, to set the u-Processor to normal routine, then troubleshoot the instrument.

Logic Signals – Abbreviations		Description
Address Decoder U110	LA3	subdecoded Addresses
	LA4	
	$\overline{WS1}$	
	$\overline{CLT}$	Control signal for U103
	$\overline{CLR}$	ERROR Feedback Reset
	$\overline{CLM}$	Control signal for U150
Control Latch U150	$\overline{CLM}$	Operating Mode Control Latch select
	F/S	Control signal for U201 H = all modes, except triggered pulse
	PH	Phase control voltage
	LOF	Output Level Check H = normal L = self test
	M1	Control Modes
	M2	
	M3	
	NORM/COMPL	control signal for shaper IC (see SB 7)
	T/G	Trigger/Gate control for U201
Range Latch U210	WS2	Frequency Range Latch select
	$\overline{EXT}$	Frequency control (see table 8–6–5 A)
	$\overline{EXT}$	
	R3	
	R4	
	R5	
	R6	
	R7	
	$\overline{LFR}$	Capacitance Amplifier enable (Low Frequency Range)
Trigger Mode Latch U103	$\overline{CLT}$	Trigger Mode Latch select
	POS	trigger on positive transition
	NEG	trigger on negative transition
	MAN	trigger when MAN pushbutton is operated
	BOS	Burst ON FF set
	AVR	Auto Vernier FF reset
	BOR	Burst ON FF reset
	WF1	Waveform Switching control signals see table 8–6–6
	WF2	
Timing IC U300	$\overline{WS3}$	Timing IC Input Store select
	LD7	Data to be latched into the Input store of U300. see Service Block 4 (Theory of Operation)
	LD6	
	LD5	
	LD4	
	LD3	
	LD2	
	LD1	
	LD0	
Error Feedback U301/U302	$\overline{RSA}$	Error Feedback Gate signal
	$\overline{CLR}$	Error Feedback reset

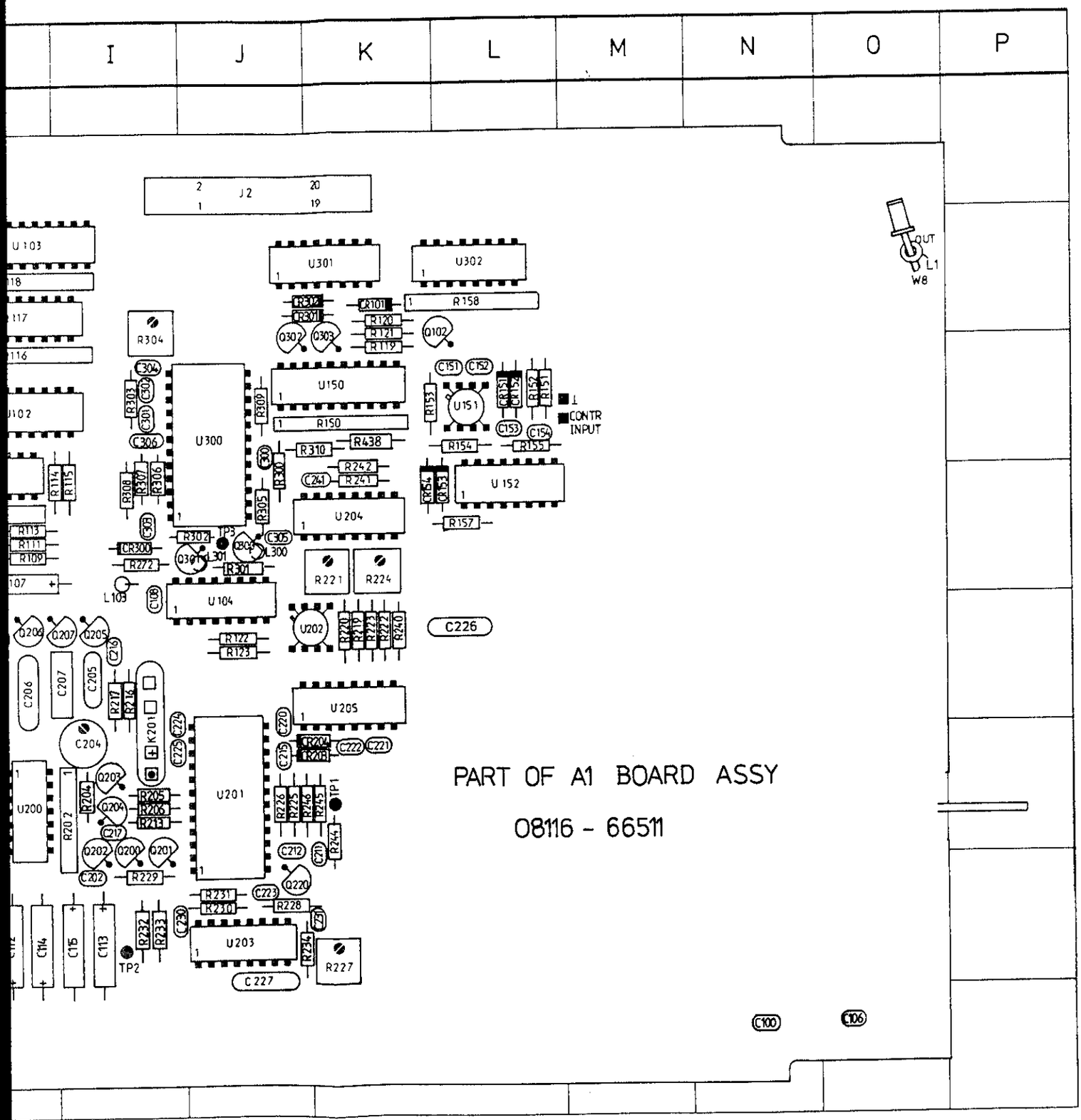
Table 8–6–9.

Oscillator Sht 1 of 2



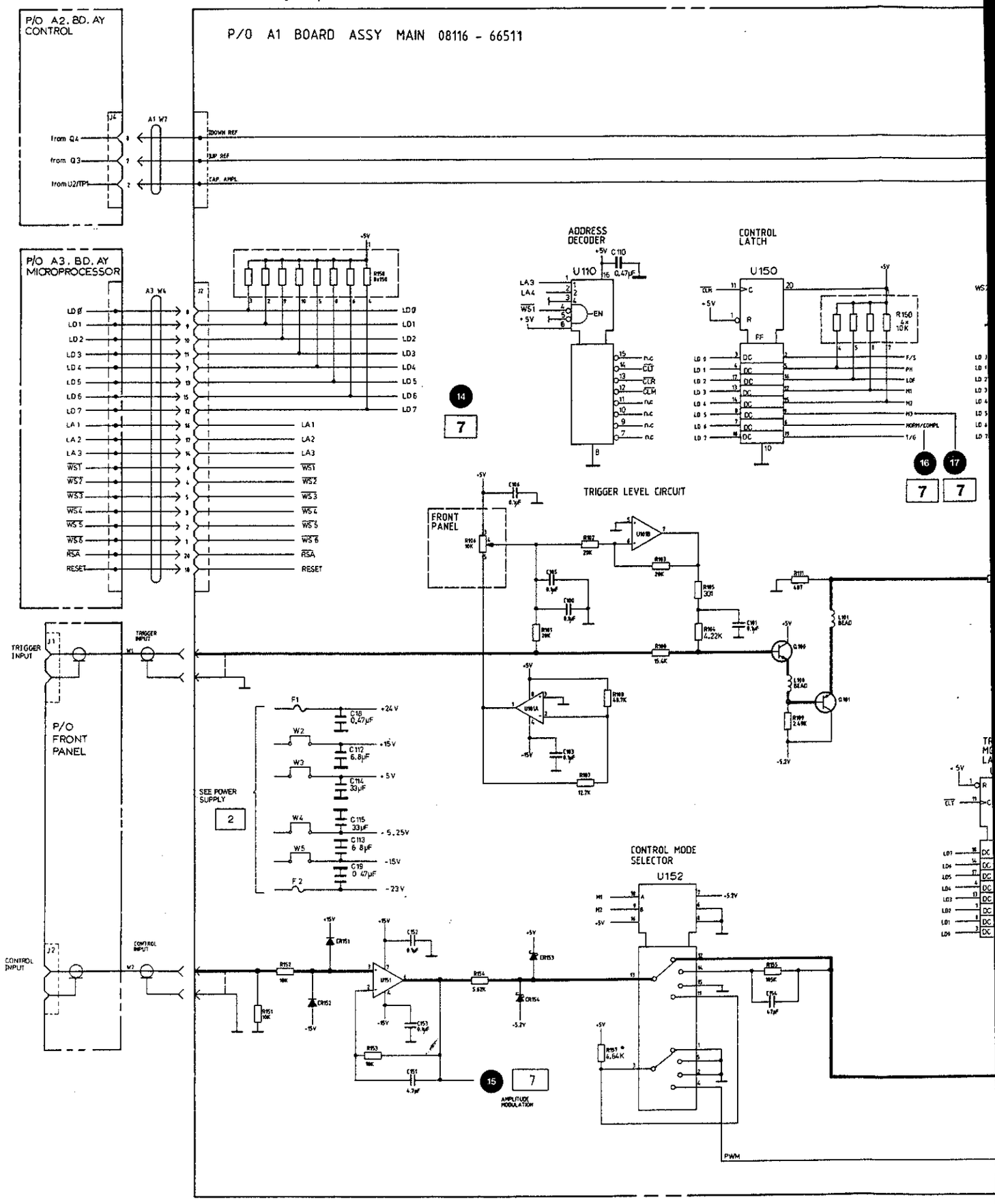
8-16b

Oscillator Sht 2 of 2

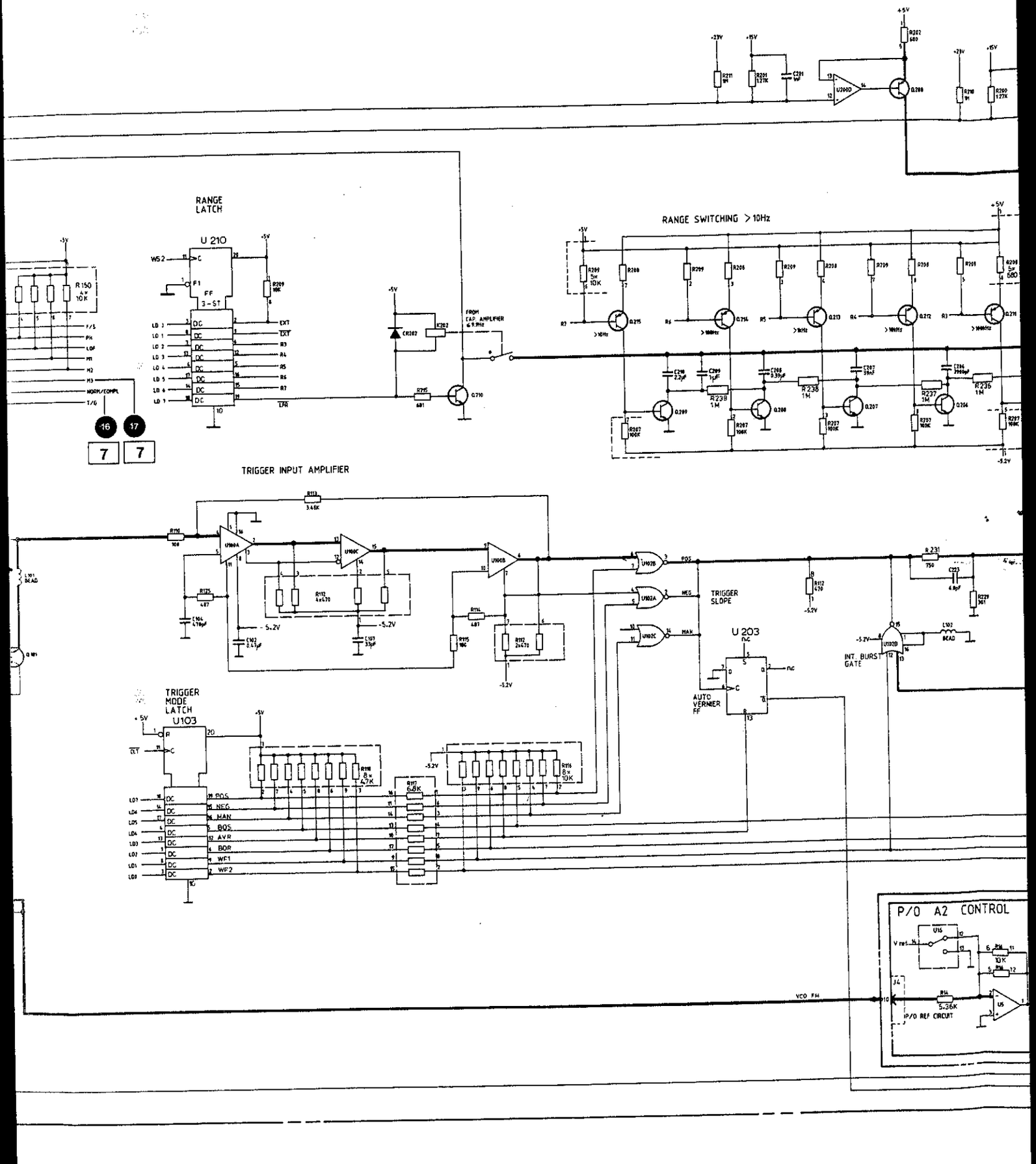


COMP	REF			COMP	REF			COMP	REF
C18	F5	C225	I6	Q204	I6	R150	K3	R243	G6
C19	F7	C226	L5	Q205	I5	R151	L3	R244	K6
C100	N8	C227	J7	Q206	H5	R152	L3	R245	J6
C101	G4	C230	I7	Q207	I5	R153	K3	R246	J6
C102	G3	C231	J7	Q208	H5	R154	L4	R272	I4
C103	G5	C240	G6	Q209	H5	R155	L4	R300	J4
C104	G3	C241	K4	Q210	G5	R157	L4	R301	J4
C105	G4	C300	J4	Q211	G3	R158	L2	R302	J4
C106	O8	C301	I3	Q212	H3	R200	K6	R303	I3
C107	H5	C302	I3	Q213	G3	R201	H6	R304	I3
C108	I5	C303	I4	Q214	G3	R202	I6	R305	J4
C110	G1	C304	I3	Q215	H3	R204	I6	R306	I4
C112	H7	C305	J4	Q220	J7	R205	I6	R307	I4
C113	I7	C306	I3	Q300	J4	R206	I6	R308	I4
C114	H7	CR101	K2	Q301	I4	R207	G3	R309	J3
C115	I7	CR151	L3	Q302	J3	R208	G2	R310	K4
C151	L3	CR152	L3	Q303	K3	R209	G2	RT1	K8
C152	L3	CR153	L4	R100	G4	R210	H6	U100	H4
C153	L4	CR154	K4	R101	G4	R211	H6	U101	G4
C154	L4	CR201	H2	R102	G4	R213	I6	U102	H3
C200	H7	CR202	G5	R103	G3	R215	G5	U103	H2
C201	G7	CR203	J6	R104	G4	R216	I5	U104	J5
C202	I7	CR204	J6	R105	G4	R217	I5	U110	G1
C204	I6	CR300	I4	R106	Front panel	R219	K5	U150	K3
C205	I5	CR301	J2	R107	G4	R220	K5	U151	L3
C206	H5	CR302	J2	R108	G4	R221	K5	U152	L4
C207	I5	J2	J2	R109	H4	R222	K5	U200	H6
C208	H6	K201	I6	R110	H4	R223	K5	U201	J6
C209	H6	K202	G6	R111	H4	R224	K5	U202	J5
C210	G6	L100	H4	R112	H4	R225	J6	U203	J7
C211	K7	L101	H4	R113	H4	R226	J6	U204	K4
C212	J6	L102	H3	R114	H4	R227	K7	U205	K5
C213	G5	L103	I5	R115	I4	R228	J7	U210	G2
C214	G5	L300	J4	R116	H3	R229	I7	U300	J4
C215	J6	L301	J4	R117	H2	R230	J7	U301	K2
C216	I5	Q100	H4	R118	H2	R231	J7	U302	L2
C217	I6	Q101	H4	R119	K3	R232	I7	VR200	E6
C220	J5	Q102	L3	R120	K3	R233	I7	W2	F5
C221	K6	Q200	I7	R121	K3	R234	J7	W3	F6
C222	K6	Q201	I7	R122	J5	R240	K5	W4	F6
C223	J7	Q202	I7	R123	J5	R241	K4	W5	F6
C224	I6	Q203	I6	R125	G3	R242	K4		

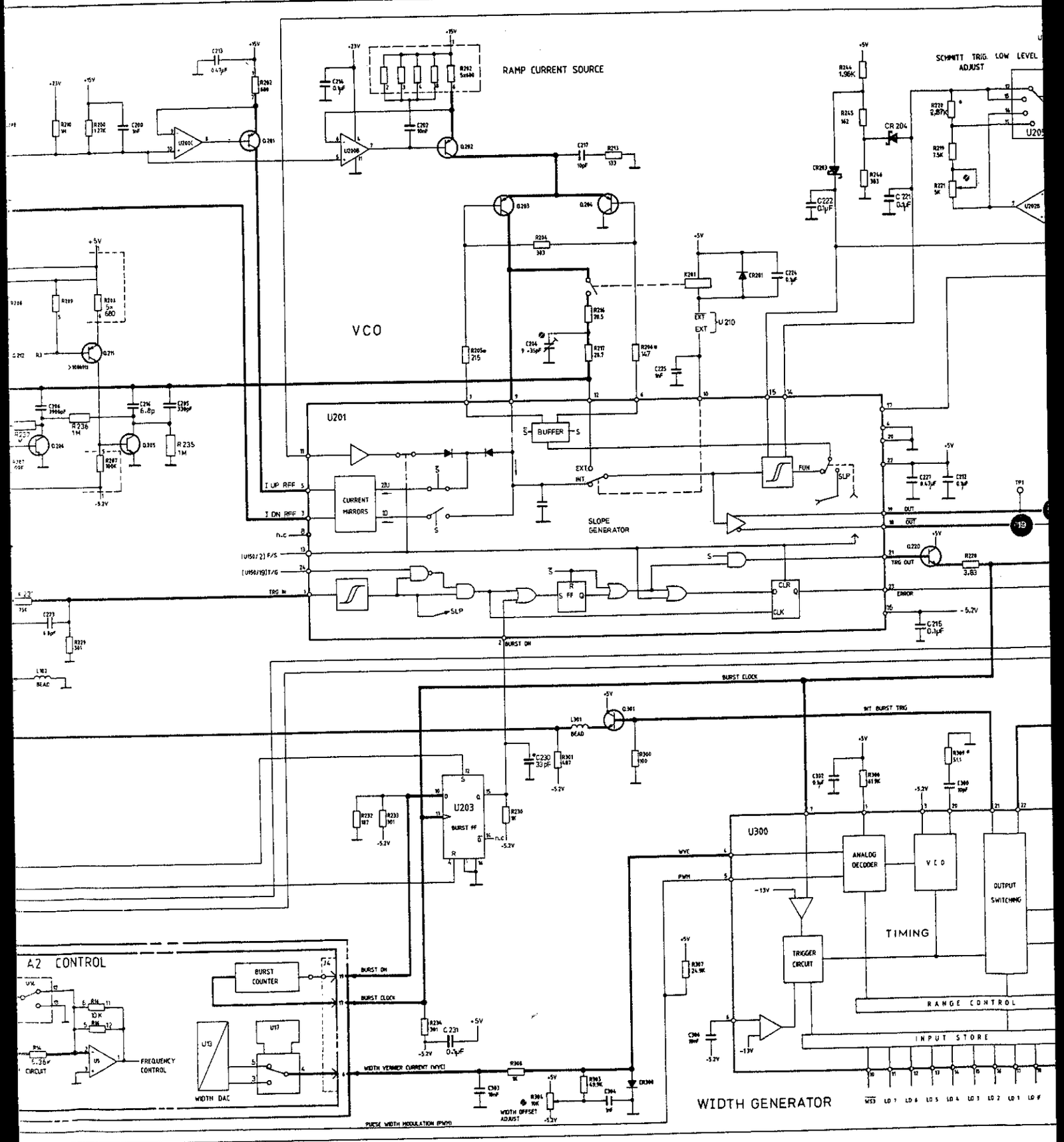
Oscillator Schematic
Sht 1 of 4



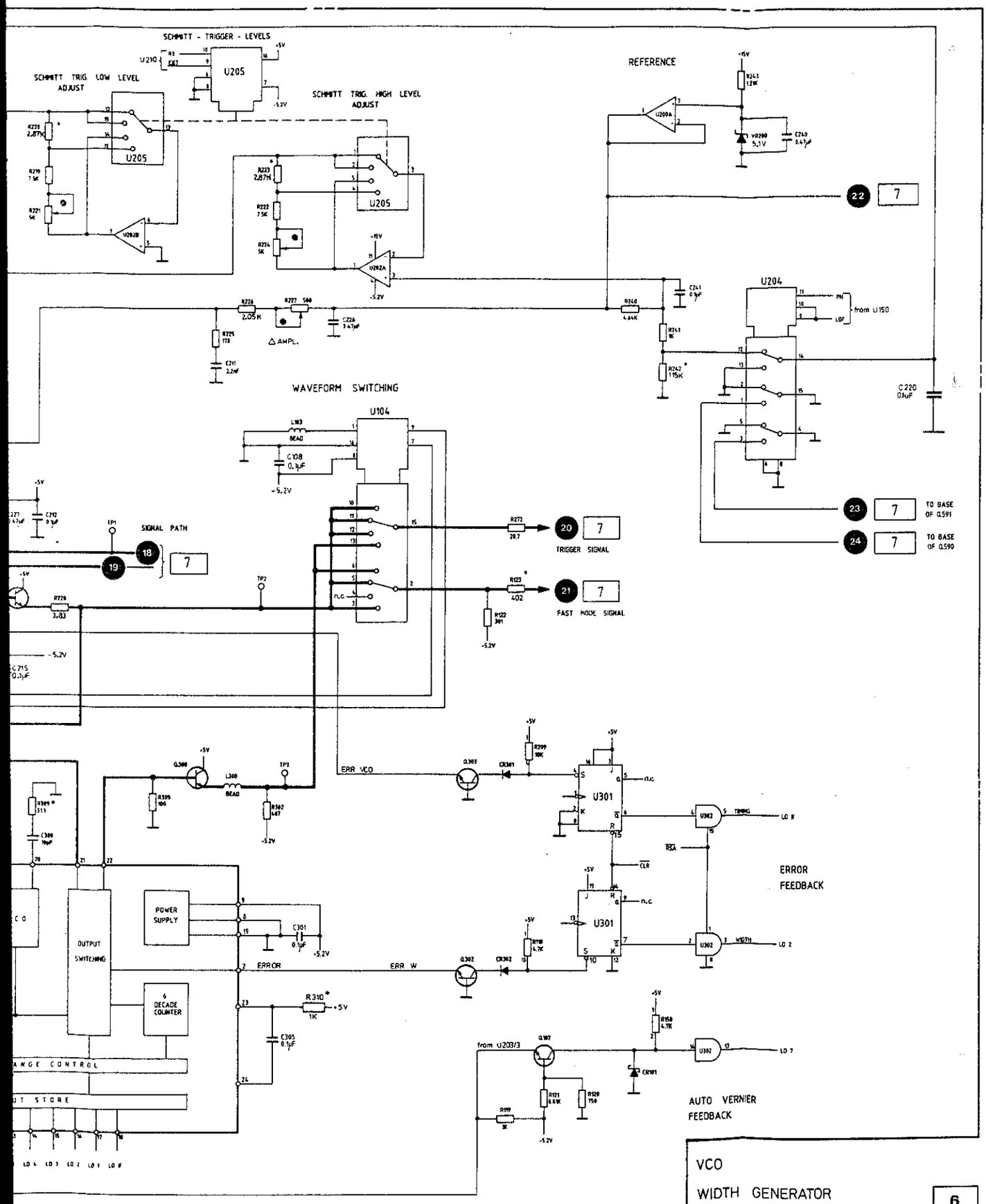
Oscillator Schematic
Sht 2 of 4



Oscillator Schematic
Sht 3 of 4



Oscillator Schematic
Sht 4 of 4



SERIVCE BLOCK 7
SHAPER, OUTPUT AMPLIFIER THEORY OF OPERATION

Introduction

The Shaper and Output Amplifier circuitry is located on A1 Board Assy. These circuits are the last in the signal path, and it is from the Output Amplifiers that the 8116A Output and Trigger Output signals are derived.

The entire circuitry can be broken down into areas under the following headings:

1. Shaper IC
2. Amplitude Modulator
3. Current Mirror
4. Pre-Attenuator
5. Signal Output Amplifier
6. Output Attenuator
7. Trigger Output Amplifier

1. Shaper IC U401

The Shaper IC is a high-performance signal control circuit. It functions as a linear pre-amplifier or a triangle to sine converter. Controlling the EECL input by a pulse width EECL levels (0 V to −0.6 V), the IC also generates a pulse with fast but fixed transition times. While the main inputs are differential current inputs, the EECL input is a single ended voltage input. The output waveform of the differential outputs is selected by the two digital mode inputs.

The low frequency input modulates the amplitude of all waveforms, although the modulating current has to be generated externally (see Amplitude Modulator).

The Shaper IC Vernier stage attenuates each output signal using an externally derived DC current. When the Vernier input pin voltage is held at virtual ground, a voltage source and resistor may be used to attenuate.

For all waveforms, normal and complement phase is selectable via a digital input. In addition, two bias inputs are incorporated to level shift the output signal (Figure 8–7–1 shows a block diagram of the Shaper IC).

2. Amplitude Modulator

The Amplitude Modulator relies on two external stimuli for operation. The first of these stimuli is derived from the signal applied to the Control Input connector. This control signal is passed through a buffer amplifier. The input to the amplifier circuit is protected against voltage excursions outside a +/− 15 V window, while the op-amp output is limited between +5 V and −5.2 V.

The second stimuli to the Amplitude Modulator takes the form of a TTL signal (M3, R430), which when in its false state (low), disables the modulator output.

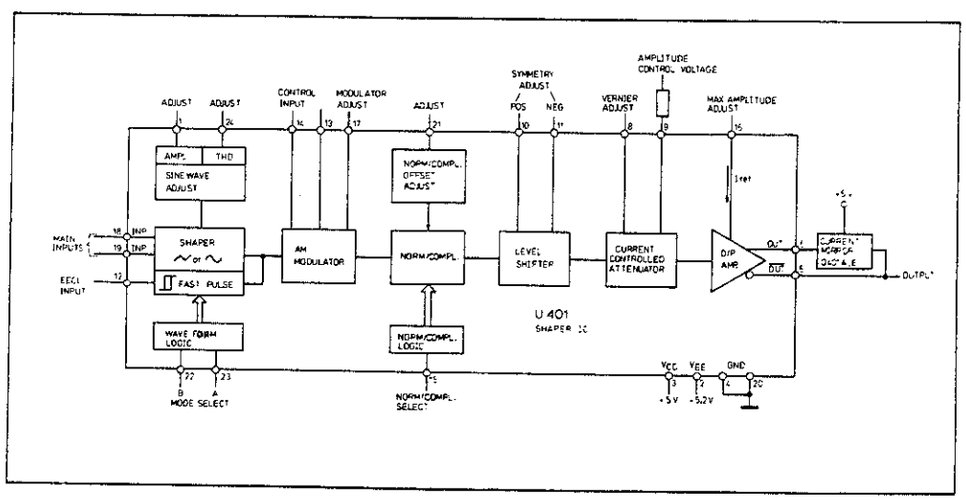


Figure 8–7–1. Shaper I.C. block diagram

When the logic signal M3 is high as a result of AM being selected at the 8116A frontpanel, the principle of circuit operation is as follows:

Transistor Q430 is switched off. Q431 base is biased towards the +5 V supply and follows the operational amplifier output. Q431 emitter tracks the base potential and, therefore Q432 turns on accordingly. Q432 and Q433 form the complementary amplifier stage of the circuit ensuring that the signal applied to the Shaper IC has a current capability and offset proportional to its input amplitude.

3. Current Mirror

The differential output of the Shaper IC requires a special output stage which is designated "current mirror". By summing the differential output currents in such a circuit, the undesirable offset on the output is eliminated and a doubling of the available output signal is achieved.

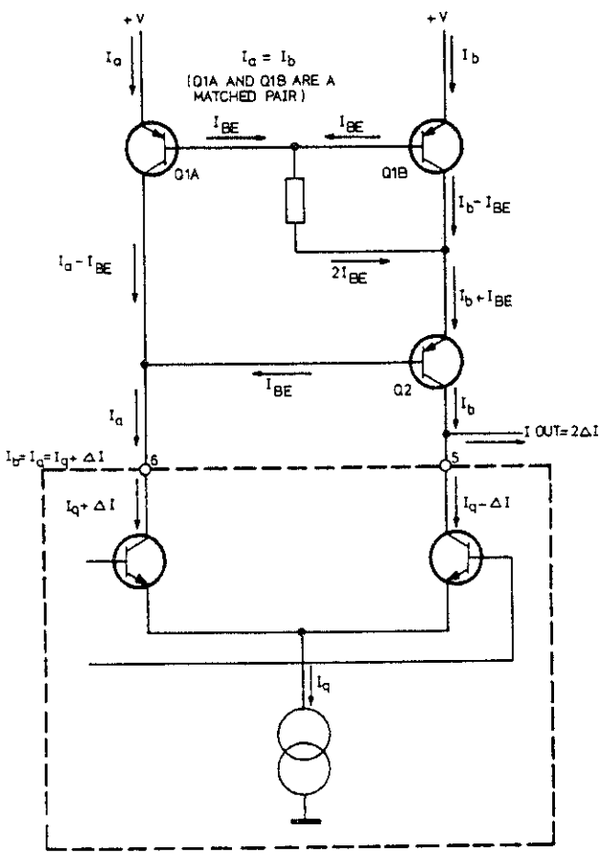


Figure 8–7–2. Current mirror principle

The operating principle is illustrated in Figure 8–7–2. The Current Mirror performs a current inversion and, in effect, produces an output current which is a true reflection of its input, providing that Q1A and Q1B are a matched pair. By summing the differential currents, the quiescent currents Iq and their effect are eliminated.

In triangle and sine mode, a logic low level is applied to Q403 which switches the RC combination R441/C406 to the current mirror to improve the performance of the current mirror.

4. Pre-Attenuator

The pre-attenuator circuit is logically controlled by signals from the bus via latch U503. The logic signals are needed to energise relays K501 to K504 in order to determine the signal path through the pre-attenuator.

With K501 energised, the Shaper IC output is not attenuated, and is passed directly to the output amplifier.
K502 and K504, when energised, provide an attenuation path of 3.7 dB which attenuates the max. shaper output current to give 9.99 V instead of 16 V. K503 and K404 when energised, produce a path giving 23.7 dB attenuation to provide the 0.1 – 0.99 V range.

5. Signal Output Amplifier

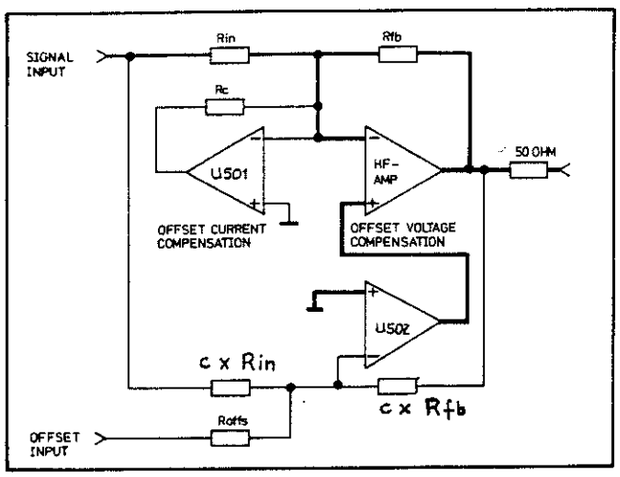
The prime functions of the output amplifier are to amplify the signal from Shaper IC U401, and add the required offset voltage. The amplifier is, in principle, an inverting operational amplifier, with a voltage gain determined by the equation:

$$\text{Gain} = Rfb/Rin$$

The main amplifier is constructed from discrete components (Q501 to Q513 and related circuits on schematic 7), and has offset voltages and currents which have to be compensated for by two additional operational amplifiers. These are: offset current control amplifier (U501) and offset voltage control amplifier (U502). The offset current error of the HF amplifier's inverting input is compensated via the offset current control amplifier, which detects the potential at the virtual ground at the inverting input of the HF amplifier. This potential is then compared to ground, the offset current control amplifier then supplying the necessary current via Rc to maintain zero difference.

U502 detects any undesired offset voltage at HF AMP output via the feedback network c x Rin / c x Rfb, and compensates for it via the non-inverting input of the HF AMP. Note that this feedback network should be adjusted to provide the same dividing factor as the HF AMP feedback network.

The offset input (derived from the Offset Vernier DAC) is added to the HF amplifier output by applying the offset as current via Roffs into the summing point of the offset voltage control amplifier. Therefore it is possible to reduce the necessary offset current by a factor 'c', where 'c' is the constant ratio between corresponding resistors in the HF amplifier and offset voltage control amplifier feedback networks e.g. Rfb and c x Rfb.



Simplified Output Amplifier

The HF amplifier comprises three stages:

- Input
- Voltage Gain
- Output

The signal from the shaper/current mirror arrangement is applied to the inverting input where it is amplified by Q501, Q502 (common base amplifiers), CR501 and CR502 providing the required bias voltages. The offset signal is applied to the non-inverting input at the junction of CR501 and CR502, ensuring a constant reference point.

The output signals of this stage, produced across R524/R527 are applied to the bases of Q503 and Q504 of the voltage gain stage. These transistors operate as emitter followers for driving Q505 and Q506 to provide the actual voltage gain. The output stage consists of emitter followers Q510/Q512 and Q511/Q513 which decouple the low output impedance of Rout from the voltage gain stage.

6. Output Attenuator

The output attenuator provides 20 dB attenuation of the output signal and preserves the 50 Ohm output impedance at the same time.

Both amplitude and offset are attenuated when K505 is switched off and K506 on. Furthermore, the output is disabled when both K505 and K506 are switched off.

7. Trigger Output Amplifier

Introduction

The Trigger Output Amplifier on Board Assy A1 is principally a fixed current source, intended to supply approximately 2.4 V into 50 Ohm; or 4.8 V into high impedance whenever its output is in high state.

The amplifier is a logic driven circuit, its input stimuli coming from Timing IC U300 and Slope Generator IC U201 via multiplexer U104.

Theory of Operation

Longtail Pair Q260 and Q261 are arranged such that Q260 is OFF when a logic low is applied to its base, and ON when a logic high is received. In the meantime, because the pair are complementary, Q261 will be ON when Q260 is OFF, and OFF when Q260 is ON. Similarly Q262 and Q263 are complementary, Q262 being ON as a result of Q261 being ON (logic low input to circuit). Q263 will be turned ON by the action of Q262 turning OFF and its emitter potential therefore being allowed to increase above the fixed base potential of +5 V. Current to the load is drawn through R267 with approximately 50 mA being available. The collector of Q263 when the device is ON will have a potential in the order of +4.8 V when driving into a high impedance load, and assuming very little current is taken. When driving into 50 Ohm, however, because maximum current available is only 50 mA, the potential at Q263 collector will be divided by a factor of two. Thus the circuit output voltage is in the order of 2.4–2.5 V into 50 Ohm, and 4.8–5 V into a high impedance load.

NOTE: If an error code is shown in the display it is necessary to press a key, e.g. LCL, to set the u-Processor to normal routine, then troubleshoot the instrument.

8116A Setting:

MODE . . . . . NORM
FRQ . . . . . 1.00 kHz
AMP . . . . . 999 mV; 9.99 V; 16.0 V
OUTPUT . . . . . triangle

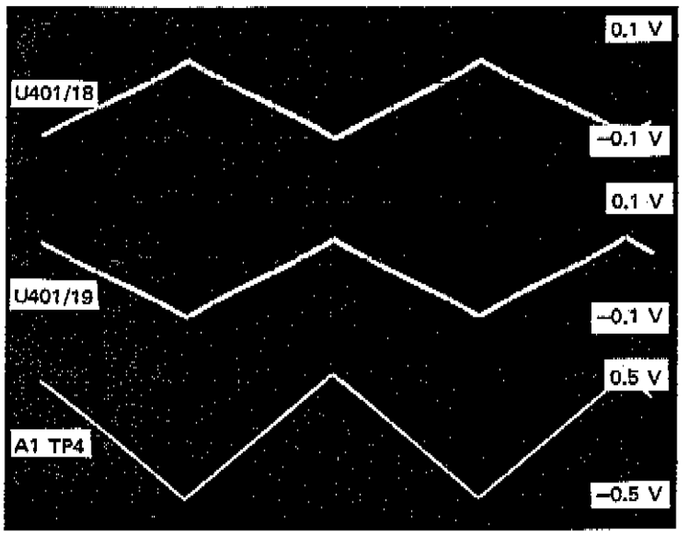


Figure 8–7–3. Shaper IC output signals

NOTE: U401/18 & 19 signals may not necessarily be symmetrical.

8116A Setting:

MODE . . . . . NORM
FRQ . . . . . 1.00 kHz
AMP . . . . . 999 mV; 9.99 V; 16.0 V
OUTPUT . . . . . pulse or square

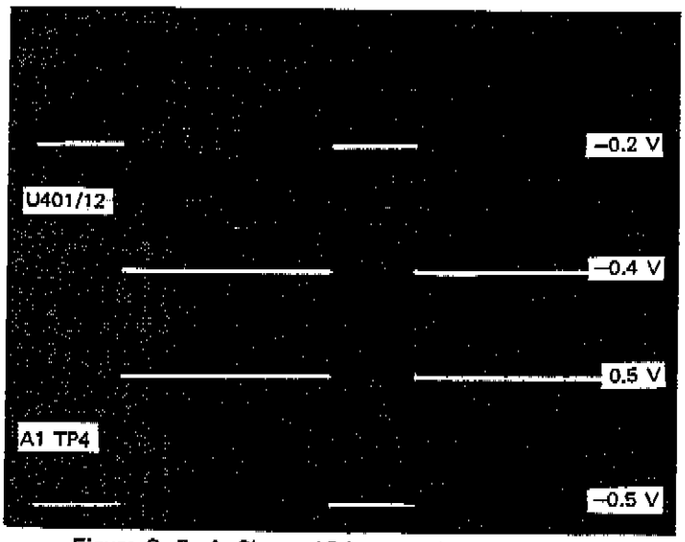


Figure 8–7–4. Shaper IC input and output signals

8-18a

Amplitude Vernier Control Voltage

8116A AMPLITUDE	Voltage at R422/R450 ± 10 %
1.00 V	7.95 V
5.00 V	4.40 V
9.99 V	0.00 V

Table 8–7–1. Offset ... 000 mV

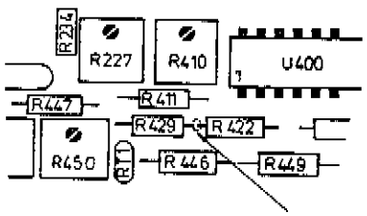


Figure 8–7–5. P/O A1 Layout

Shaper IC Reference Current

Disconnect U401 from its socket and measure the current from socket pin 16 to gnd. It should be approximately 2.5 mA.

For disconnection of U401 turn instrument off. When instrument is turned on again with disconnected U401 error E51 occurs in the display. Press LCL key to set 8116A to normal operation routine.

Current Mirror

To confirm correct operation check that the signal levels at Q401A and Q401B emitters are identical (the transistors are a matched pair).

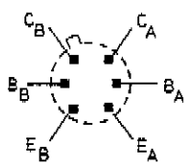


Figure 8–7–6. Q401 Bottom View

Pre-Attenuator, Output Attenuator

Amplitude Range	K1	K2	K3	K4	K5	K6
10.0 V – 16.0 V	L	H	H	H	L	H
1.00 V – 9.99 V	H	L	H	L	L	H
100 mV – 999 mV	H	H	L	L	L	H
10.0 mV – 99.9 mV	H	H	L	L	H	L
Waveform off (> 100 mV) only	H	H	L	H	L	H
DISABLE	X	X	X	X	H	H

Table 8–7–2.

Offset Vernier Control Voltage

8116A Offset	R508/C501
–7.95 V	+3.20 V
–5.00 V	+2.00 V
000 mV	0.00 V
+5.00 V	–2.00 V
+7.95 V	–3.20 V

Table 8–7–3. Amp ... 100 mV

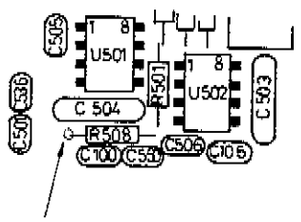


Figure 8–7–7. P/O A1 Layout

Output Amplifier

The following hints will help to isolate a fault in the 8116A output amplifier.

CAUTION

Do not operate without heat sinks on board A1. If replacement of one of the transistors Q505–Q513 is necessary, first remove all heat sink securing screws, then plate or bracket and finally, if necessary, the transistor adaptors. Do not attempt to remove a complete heatsink assembly i.e. plate and transistor adaptors together since damage to transistors will be likely.

Amplifier - Sht 1 of 2

Set 8116A:

Waveform . . . . . off
Offset . . . . . 0.00 V

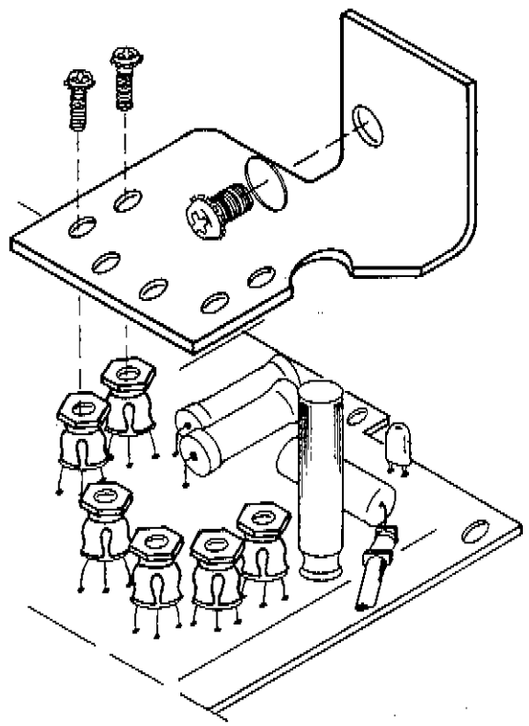


Figure 8–7–8. Heat Sink Removal

Check voltage between CR501 and CR502.
If it is fully negative (approx. –15 V) check U502, Q502, Q504 and Q506. If it is fully positive (approx. +15 V) check Q501, Q503 and Q505 and also U502.

If Q510/511 or Q512/513 fail (emitter/collector short circuit) the +24 V, –23 V Power rail fuses F1 and F2 will blow. If it is necessary to replace any of the output stage transistors Q508–Q513, check that CR505 and CR506 are not defective. They protect the output stage when high amplitude and high frequencies are required by discharging the base/emitter capacitance of Q510–Q513.

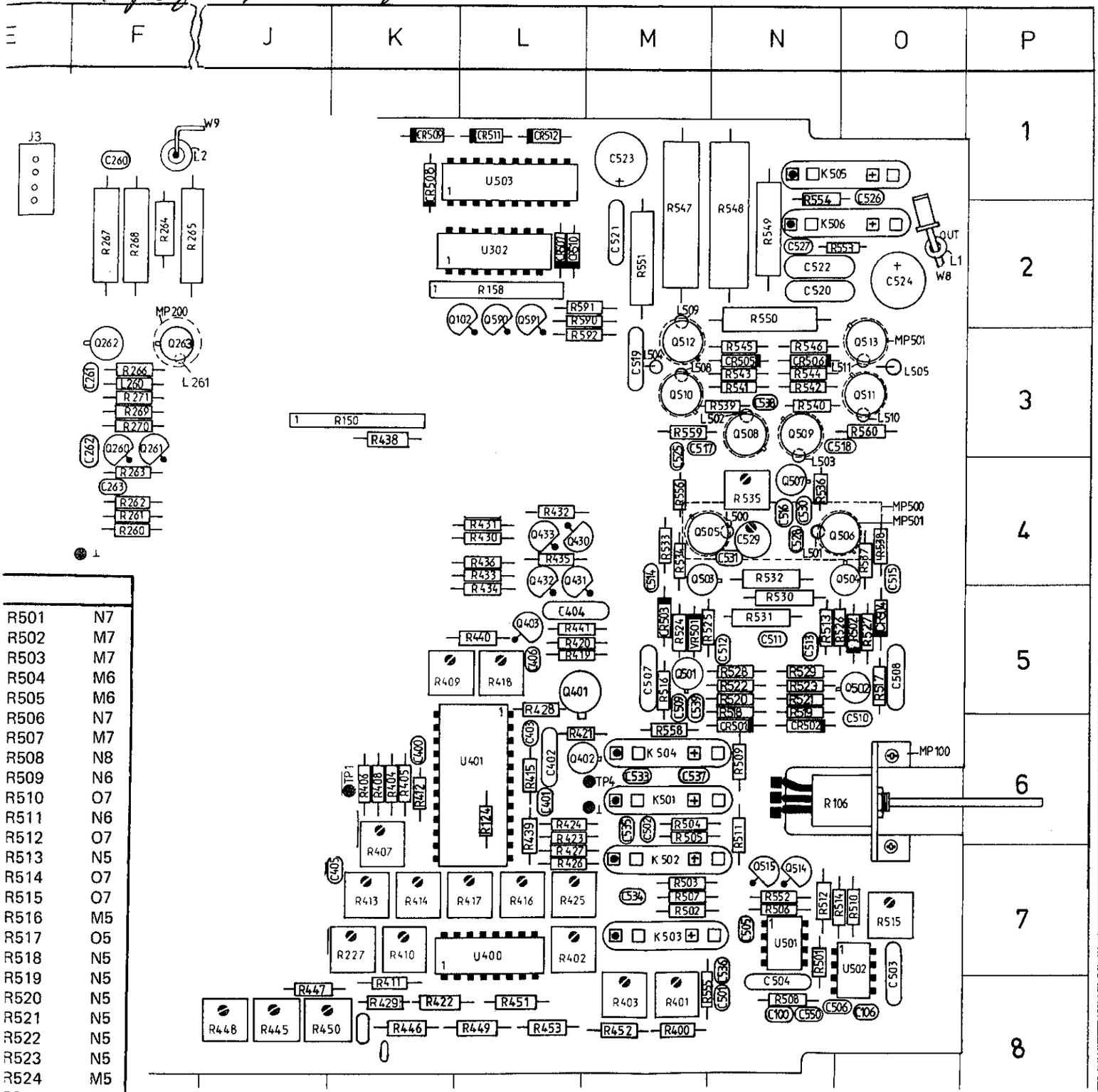
Distorted Leading and Trailing Edges

If the output in pulse or square wave has distorted leading or trailing edges, and the input signal at TP4 is undistorted, then make the following test:

Set the 8116A to high output amplitude.
If the leading edge is distorted, check Q503 and Q505.
If the trailing edge is distorted, check Q504 and Q506.

COMP	REF
C260	F1
C261	F3
C262	F4
C263	F4
C400	K6
C401	L6
C402	L6
C403	L5
C404	L5
C405	K7
C406	L5
C501	N8
C502	M6
C503	O7
C504	N7
C505	N7
C506	N8
C507	M5
C508	O5
C509	M6
C510	O6
C511	N5
C512	N5
C513	N5
C514	M4
C515	O4
C516	N4
C517	M3
C518	N3
C519	M3
C520	N2
C521	M2
C522	N2
C523	M1
C524	O2
C525	M3
C526	O1
C527	N2
C528	N4
C529	N4
C530	N4
C531	N4
C532	M6
C533	M6
C534	M6
C535	M6
C536	N7
C537	M6
C538	N3
C539	M5
C550	N8
CR501	N6
CR502	N6
CR503	M6
CR504	O6
CR505	N3
CR506	N3
CR507	L2
CR508	K1
CR509	K1
CR510	L2
CR511	L1
CR512	L1
J3	E1
K501	M6
K502	M7
K503	M7
K504	M6
K505	O1
K506	O2
L260	F3
L261	F3
L500	N4
L501	N4
L502	N3
L503	N3
L504	M3
L505	O3
L508	M3
L509	M2
L510	O3
L511	O3
Q260	F4
Q261	F4
Q262	F3
Q263	F3
Q401	L5
Q402	L6
Q403	L5
Q430	L4
Q431	L4
Q432	L4
Q433	L4
Q501	M5
Q502	O5
Q503	M4
Q504	O4
Q505	M4
Q506	O4
Q507	N4
Q508	N3
Q509	N3
Q510	M3
Q511	O3
Q512	M3
Q513	O3
Q514	N7
Q515	N7
Q590	L2
Q591	L2
R124	L6
R150	K3
R158	L2
R260	F4
R261	F4
R262	F4
R263	F4
R264	F2
R265	F2
R266	F3
R267	F2
R268	F2
R269	F3
R270	F3
R271	F3
R400	M8
R401	M8
R402	L7
R403	M8
R404	K6
R405	K6
R406	K6
R407	K7
R408	K6
R409	K5
R410	K7
R411	K8
R412	K6
R413	K7
R414	K7
R415	L6
R416	L7
R417	L7
R418	L5
R419	L5
R420	L5
R421	M5
R422	K8
R423	L6
R424	L6
R425	M7
R426	L7
R427	L7
R428	L5
R430	L4
R431	L4
R432	L4
R433	L4
R434	L4
R435	L4
R436	L4
R438	K3
R439	L6
R440	L5
R441	L5
R445	J8
R446	K8
R447	J8
R448	J8
R449	L8
R450	J8
R451	L8
R452	M8
R453	L8
R501	N
R502	M
R503	M
R504	M
R505	M
R506	N
R507	M
R508	N
R509	N
R510	C
R511	N
R512	C
R513	N
R514	C
R515	C
R516	N
R517	C
R518	N
R519	N
R520	N
R521	N
R522	N
R523	N
R524	N
R525	N
R526	C
R527	C
R528	N
R529	N
R530	N
R531	N
R532	N
R533	N
R534	N
R535	N

Amplifier, Sht 2 of 2



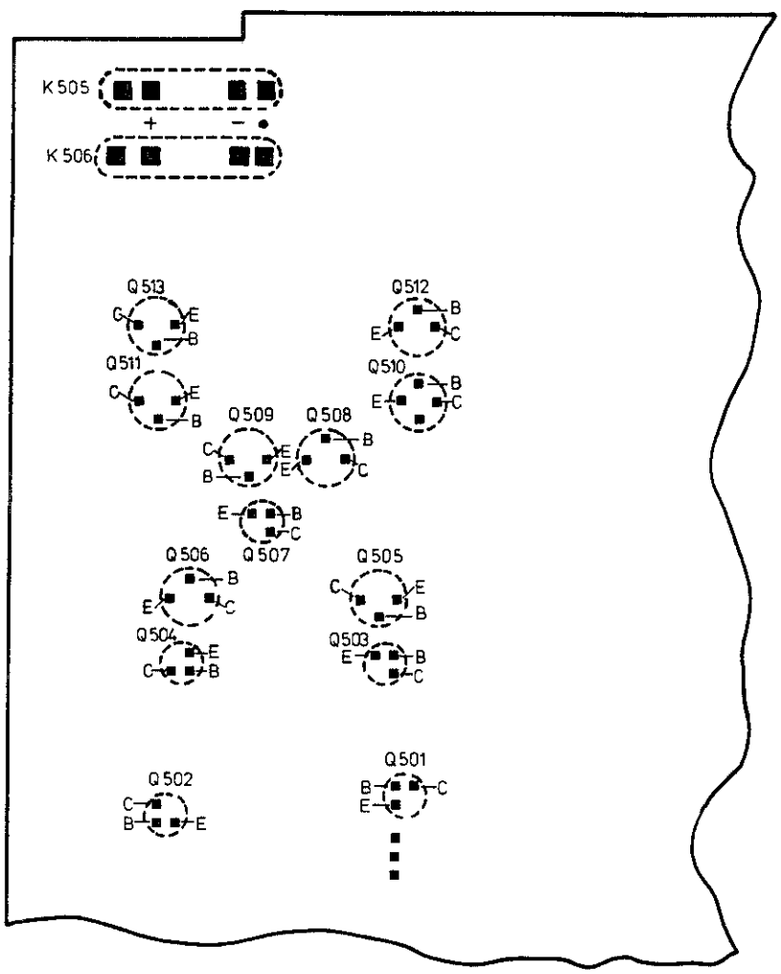
R501	N7
R502	M7
R503	M7
R504	M6
R505	M6
R506	N7
R507	M7
R508	N8
R509	N6
R510	O7
R511	N6
R512	O7
R513	N5
R514	O7
R515	O7
R516	M5
R517	O5
R518	N5
R519	N5
R520	N5
R521	N5
R522	N5
R523	N5
R524	M5
R525	N5
R526	O5
R527	O5
R528	N5
R529	N5
R530	N5
R531	N5
R532	N4
R533	M4
R534	M4
R535	N4

COMP	REF			COMP	REF		
R536	4	R546	N3	R555	N8		
R537	O4	R547	M2	R556	M4		
R538	O4	R548	N2	R558	N6	U400	L7
R539	N3	R549	N2	R559	M3	U401	L6
R540	N3	R550	N2	R560	O3	U501	N7
R541	N3	R551	M2	R590	L2	U502	O7
R542	N3	R552	N7	R591	L2	U503	L1
R543	N3	R553	O2	R592	L2	VR501	M5
R545	N3	R554	N1	U302	L2	VR502	O5

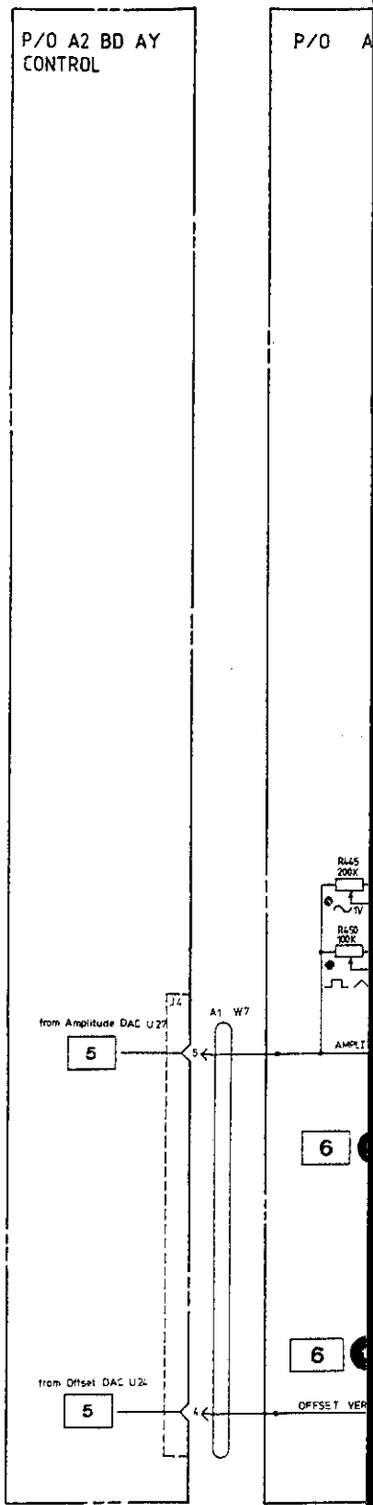
SHAPER AND OUTPUT

AMPLIFIER 7

Amplifier Schematic
Sht 1 of 4

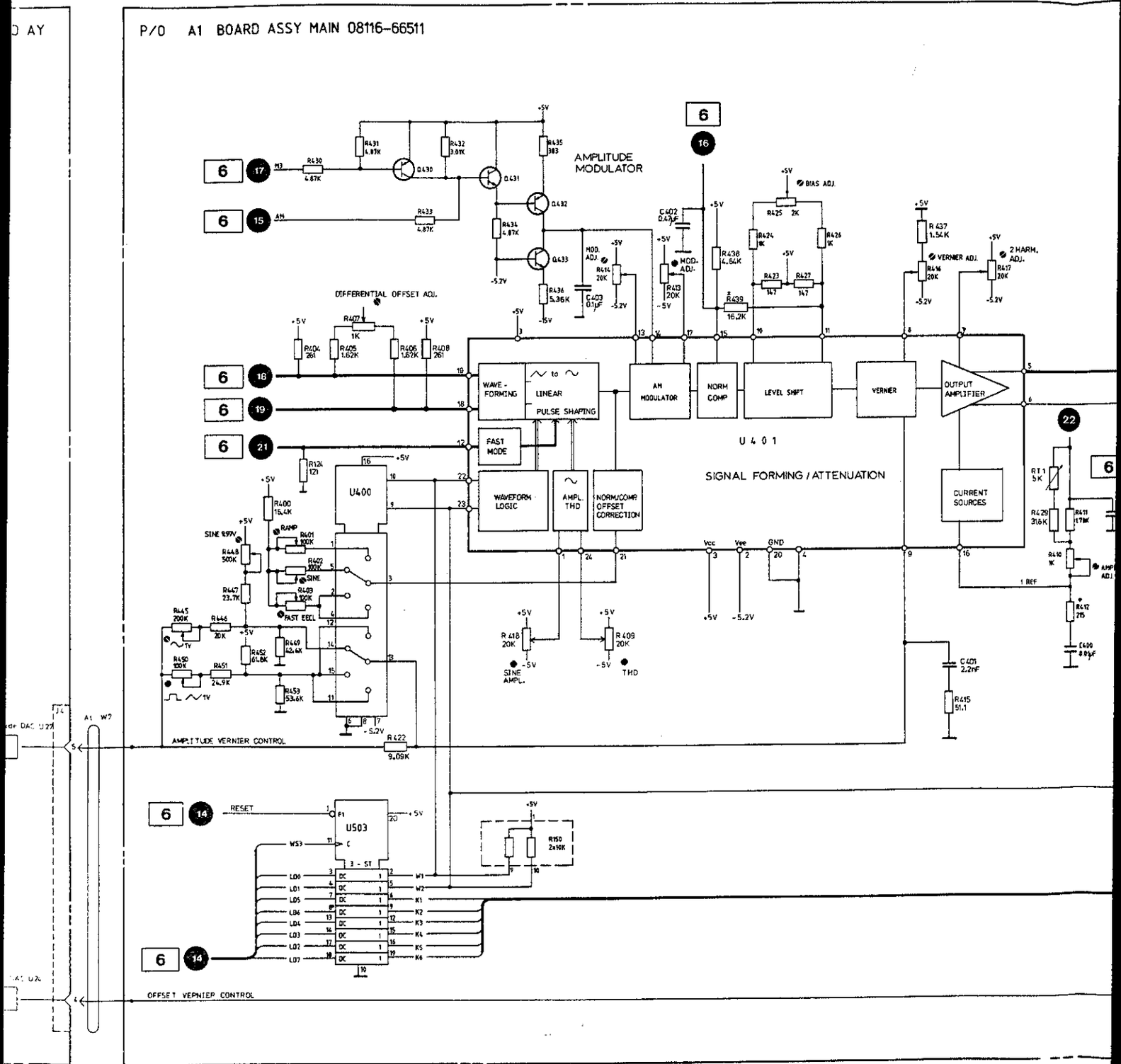


P/O A1 Layout Underside

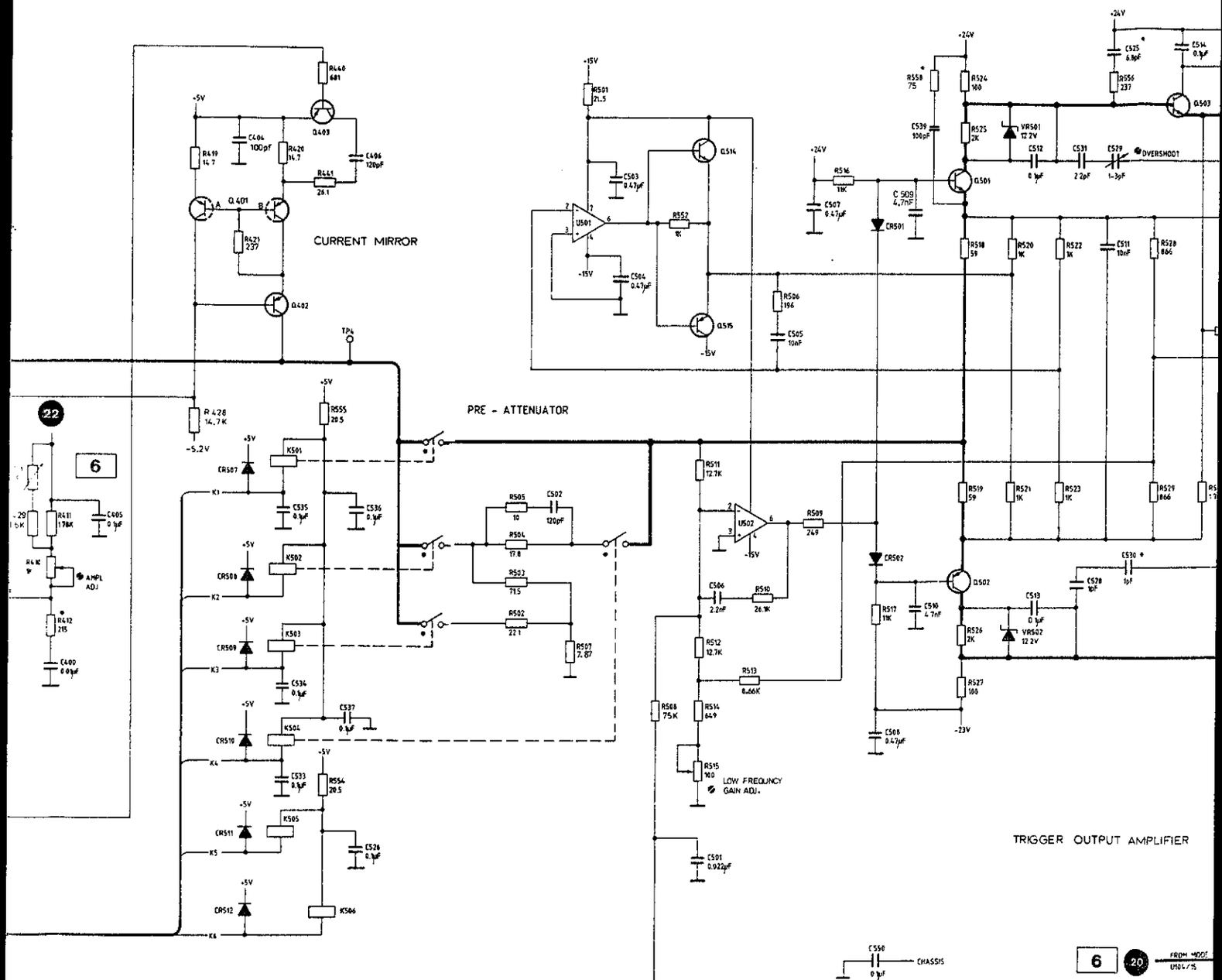


Amplifier Schematic
Sht 2 of 4

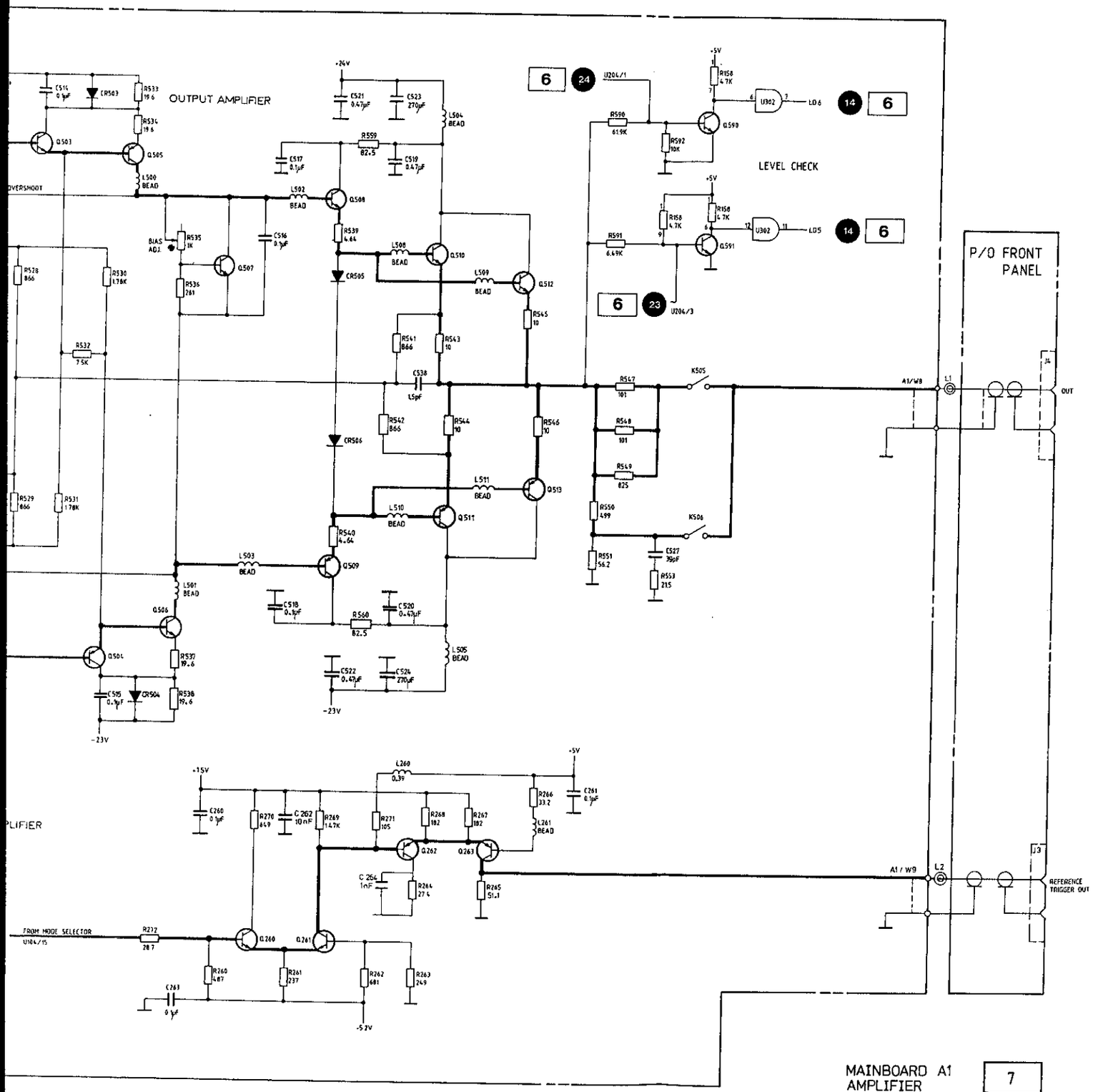
P/O A1 BOARD ASSY MAIN 08116-66511



Amplifier Schematic
Sht 3 of 4



Amplifier Schematic
Sht 4 of 4



SERVICE BLOCK 8

BURST AND SWEEP THEORY OF OPERATION

Introduction

The circuits described in this Service Block are mainly Burst oriented. Sweep mode hardware is limited to 1 DAC and X-output, Hold Input and Marker output functions because actual frequency sweeping is software controlled and, therefore, not discussed in the service section.

Burst

The Burst control circuitry can be divided into the following areas:

Burst Number Acceptors
Counter
Detect "1" circuit
Burst Flip-Flop (Main bd assy)
Oscillator (Main bd assy)

Figure 8—8—1 shows a simplified view of the burst generation circuitry.

The burst number is latched through the acceptors on receipt of $\overline{LBB}$ (low byte burst) and $\overline{HBB}$ (high byte burst) signals from the Address Decoder. The burst counter is then preset to the burst when $\overline{LBC}$ is received. The burst clock then initiates a count-down sequence which ends when the counter reaches "1".

Blocking Flip-Flop

The Blocking Flip-Flop serves a dual-purpose in this configuration. When counters U41 and U42 have cleared, the IC signals are gated by NAND gate U40B, so producing a low signal which sets the flip-flop. The Q output therefore switches high, disabling U41. $\overline{Q}$ output will now be low — the signal being gated to the wired-OR configuration (U32, U37). In the wired OR configuration, a logic high prevails, so in order for a logic low to be maintained (allowing the VCO to be disabled), all signals which come together here have to be low.

For the counter to be re-enabled, logic signal $\overline{LBC}$ must be set true (low) and gated with U40B signal. When $\overline{LBC}$ goes low, the Blocking Flip-Flop Q and $\overline{Q}$ outputs change state. Thus the $\overline{CE}$ signal is set true, enabling the counters and the wired-OR configuration output is high allowing the VCO to output the clock pulses once more.

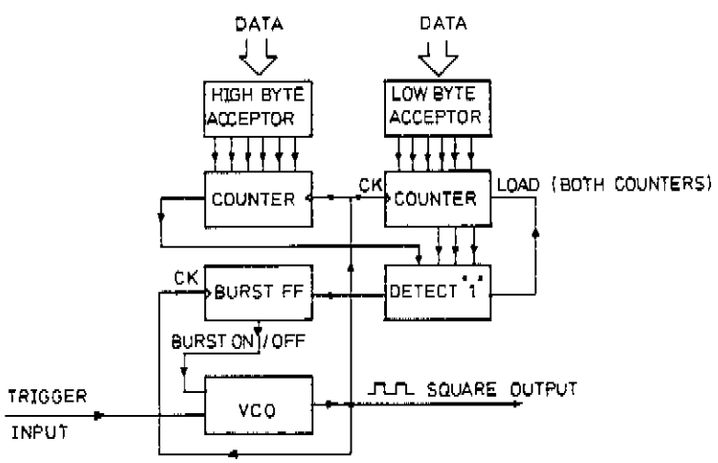


Figure 8—8—1. Simplified Burst generator

X-Output Generator

The principle of operation of this circuit depends upon a Digital to Analog conversion. DAC U29 performs a conversion of data from the latched bus and decoded data from the MPU board. The d.c. signal amplitude of the X-output represents 1.5 V for each frequency decade which has been swept, up to a maximum of 10 V (0 V corresponding to the start frequency).

Figure 8–8–2 shows the relationship between X-output amplitude and swept frequency decades.

Marker Output

The Marker Output is pre-programmed at the instrument frontpanel before the sweep has begun. The signal comes directly from the latched data bus via the offset latch and is converted from ECL to TTL in order to be compatible with any external instruments.

Hold Input

The hold input, on attaining a TTL high state, inhibits latch U3. The capacitance amplifier range on A2 bd is now held at a steady state. The Range Switching circuit on A1 bd is also disabled and, therefore, the VCO ramp capacitor charge is held. The overall effect of these events is that the 8116A sweep output stops at the point in the sweep it has reached instantaneously the hold signal is received. To continue the sweep, Hold must be switched low.

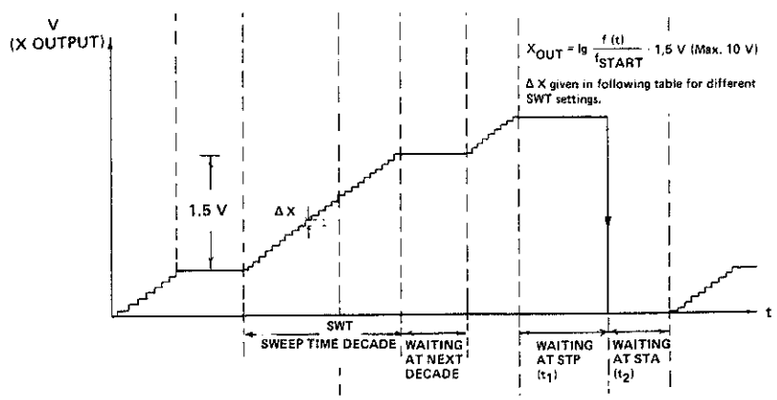


Figure 8–8–2. X output vs swept frequency

1

THIS SERVICE BLOCK APPLIES TO
OPTION 001
INSTRUMENTS ONLY.

NOTE: If an error code is shown in the display it is necessary to press a key, e.g. LCL, to set the u-Processor to normal routine, then troubleshoot the instrument.

The Output Address Decoder, which provides the logic control signals for Sweep Generator DAC, Burst Number Acceptors and Burst Counter on A2 Control Board Assy can be checked with Signature Analysis against table 8–8–2. Set the u-Processor to free run mode by setting the jumper P1 to "P1" position on board A3. Disconnect jumper A2W2 connect RES (A3) to gnd for a short time to reset the u-Processor.

Signature Analyzer	A3 u-Processor Board Assy
Start 	TP "SA"
Stop 	TP "SP"
Clock 	TP "E"
⊥	⊥

Table 8–8–1. Signature Analyzer setting and connection to A3 u-Processor Board Assy

NOTE: Verify that reading at +5 V is 0003. If not, the u-Processor does not run free.

Burst Counter

The correct operation of the Burst Counter can be verifed with the following test procedure, refer to figure 8–8–3 for the waveform and timing data.

1. Turn instrument off.
2. Desolder wire W3 on A2 Control Board and solder it to "test" position.
3. Connect A1 U203 pin 10 to ground.
4. Turn instrument on.
5. Set 8116A:

   MODE . . . . . E.BUR
   FREQ . . . . . 1.00 MHz
   BUR . . . . . 1024 #

6. Press MAN-Pushbutton.

Check logic TTL levels at Burst Number Acceptors U18 and U15.

BN1	thru BN 10	L
BN11		H

Table 8–8–3. U15 & U18 output for Burst Number 1024.

Output Address Decoder (U20)

Mnemonic	Description	"Free Run" Signatures see table 8–8–1
LA3		P5OH
LA4	subdecoded	CH9U
LA5	Addresses	8759
WSG		IFHG
$\overline{LBS}$	Low Byte Sweep	8392
$\overline{HBS}$	High Byte Sweep	5O8P
$\overline{LBB}$	Low Byte Burst	H456
$\overline{HBB}$	High Byte Burst	IIAF
$\overline{LBC}$	Load Burst Counter	FU39

Table 8–8–2. Logic Control Signals-Mnemonics, Description & Signatures

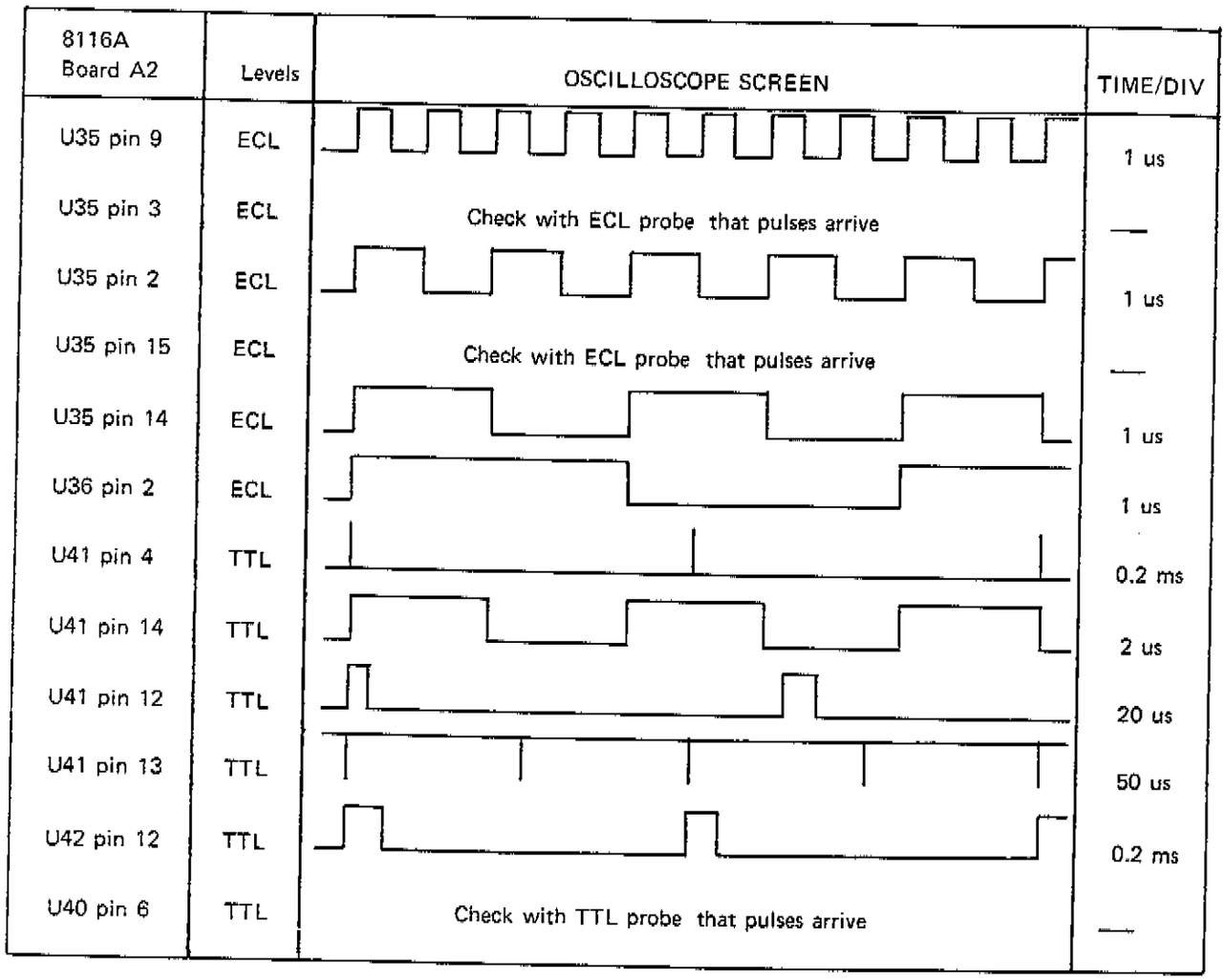
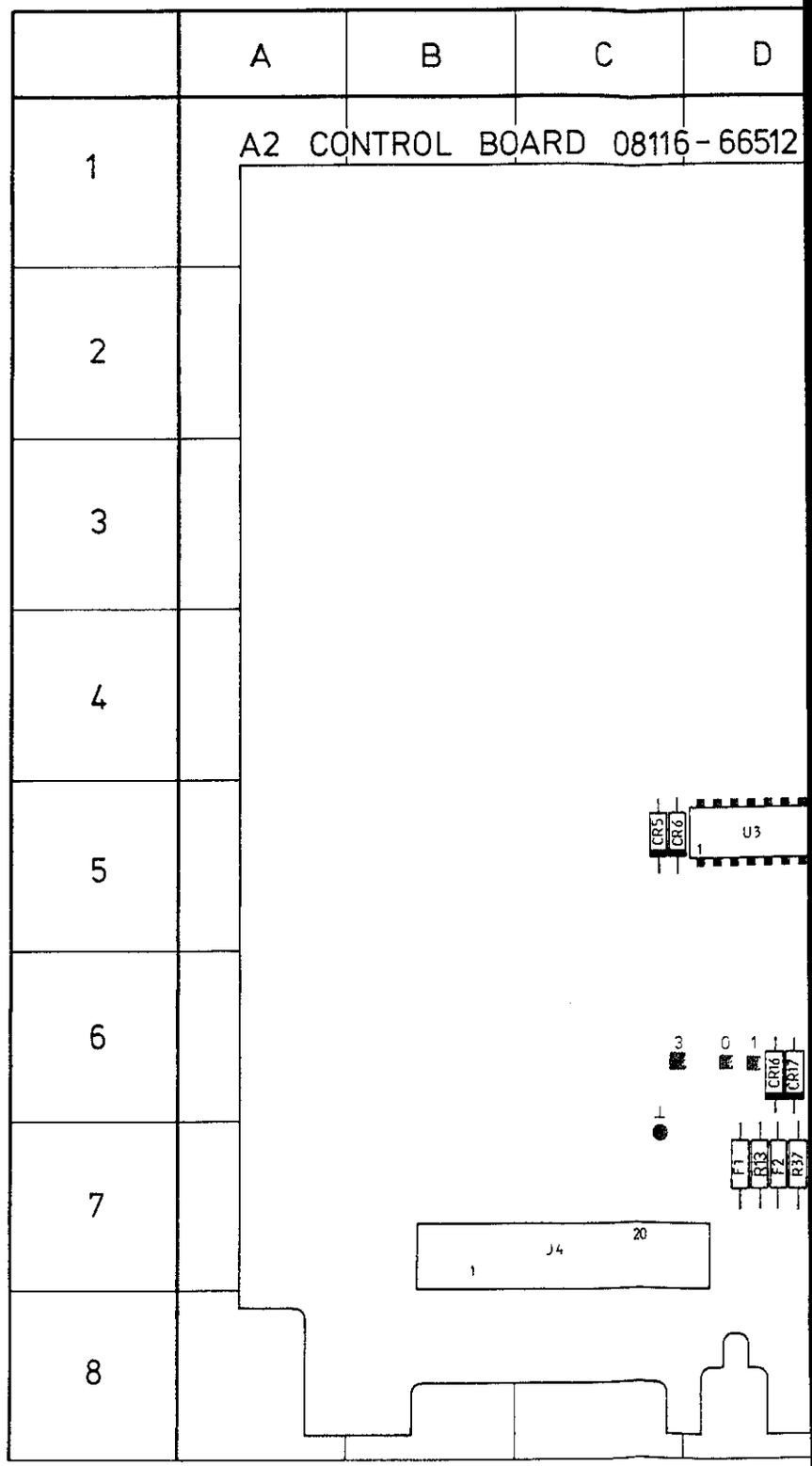


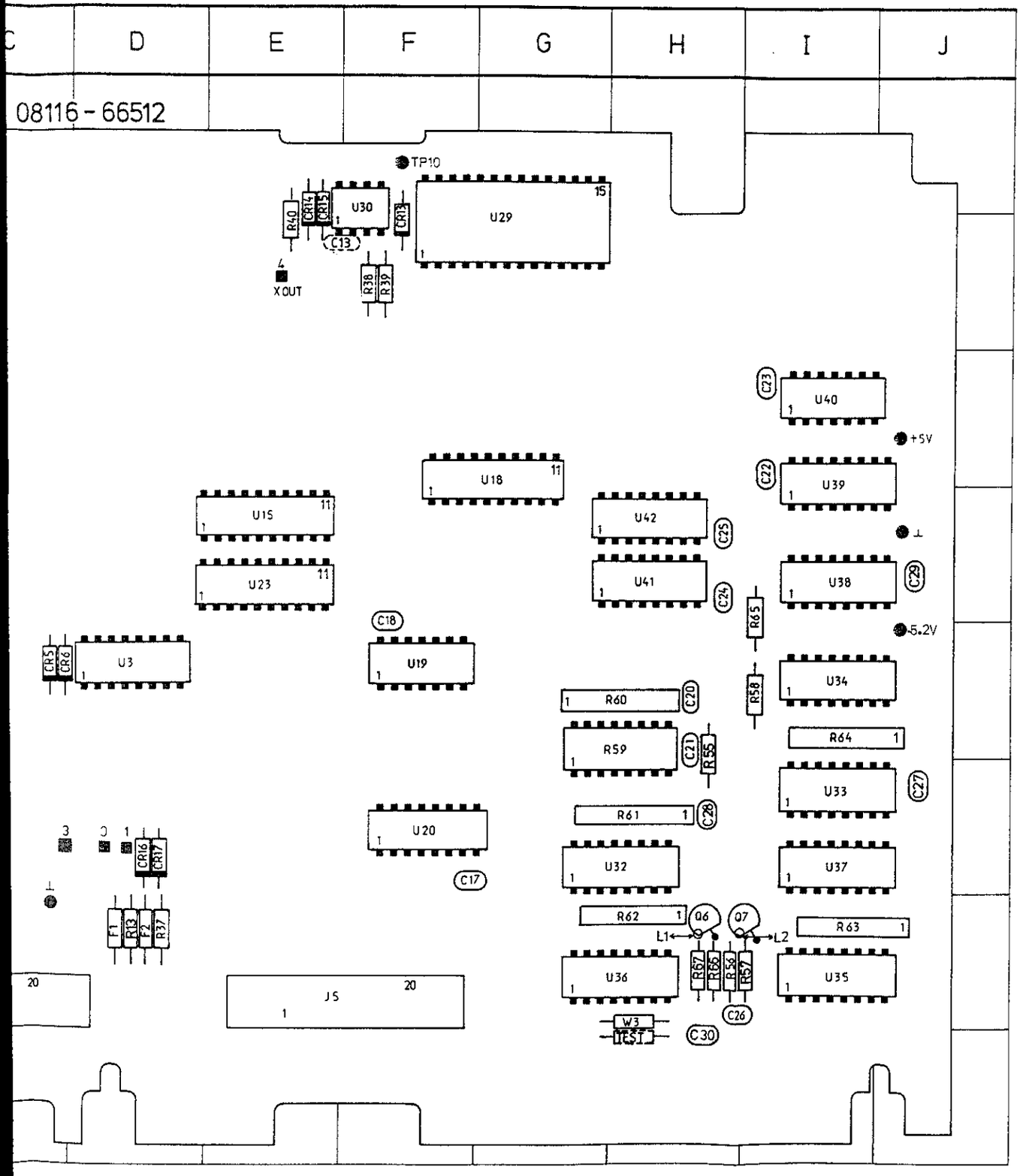
Figure 8–8–3. Burst Counter waveform and timing data

Burst, Sweep
Sht 1 of 2

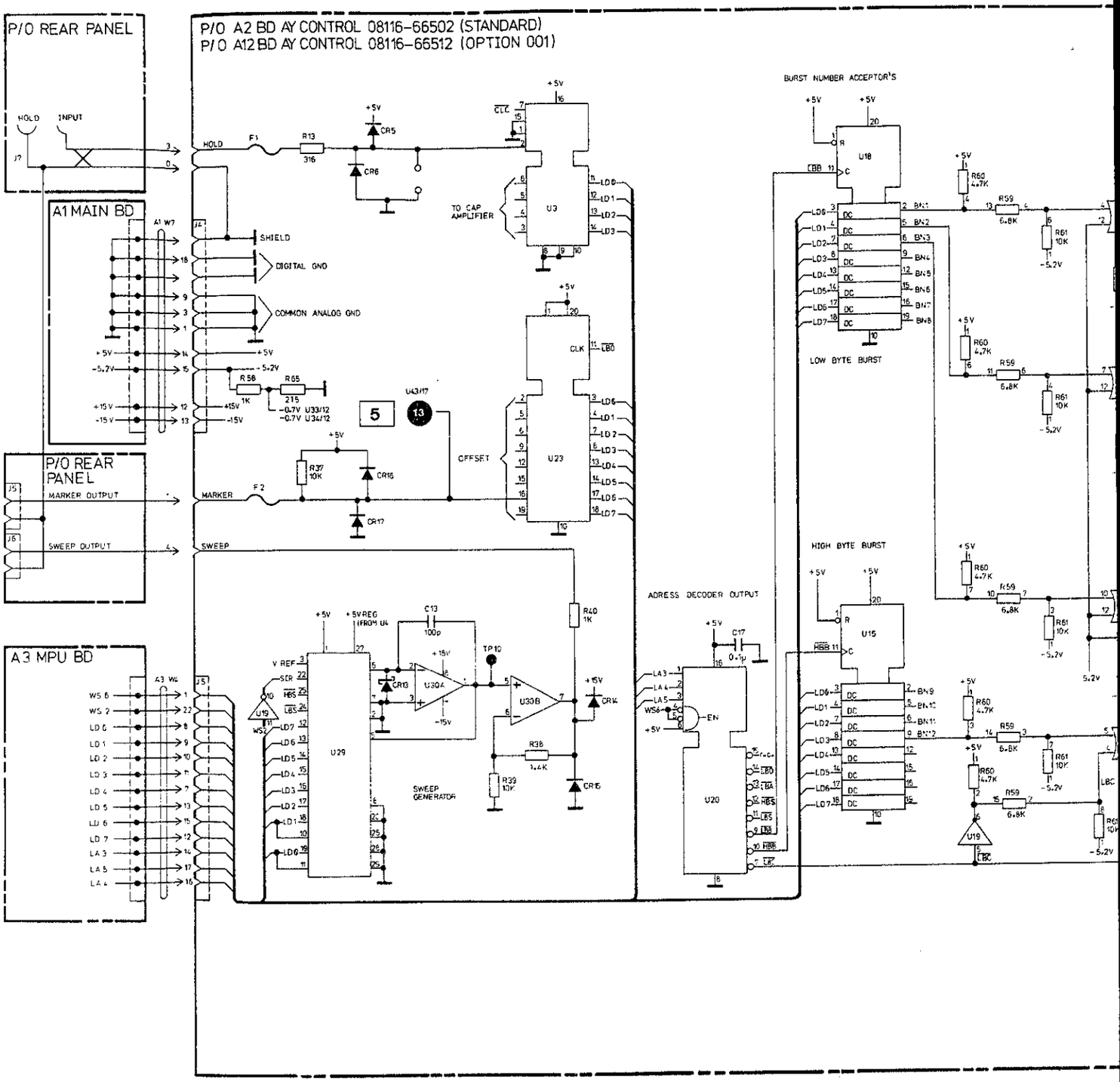
COMP	REF	COMP	REF
C13	E2	R56	H7
C17	F6	R57	H7
C20	H5	R58	H5
C21	H5	R59	H5
C22	I3	R60	H5
C23	I3	R61	H6
C24	H4	R62	H7
C25	H4	R63	I7
C26	H7	R64	I5
C27	J6	R65	I4
C28	H6	R66	H7
C29	J4	R67	H7
C30	H8	U3	B5
CR5	C5	U15	E4
CR6	C5	U18	E3
CR13	F2	U19	F5
CR14	E2	U20	F6
CR15	E2	U23	E4
CR16	D6	U29	G2
CR17	D6	U30	F1
F1	D7	U32	H6
F2	D7	U33	I6
J4	C7	U34	I5
J5	F7	U35	I7
L1	H7	U36	H7
L2	H7	U37	I6
Q6	H7	U38	I4
Q7	H7	U39	I3
R38	F2	U40	I3
R39	F2	U41	H4
R40	E1	U42	H4
R55	H5	W3	H7



Burst, Sweep
Sht 2 of 2

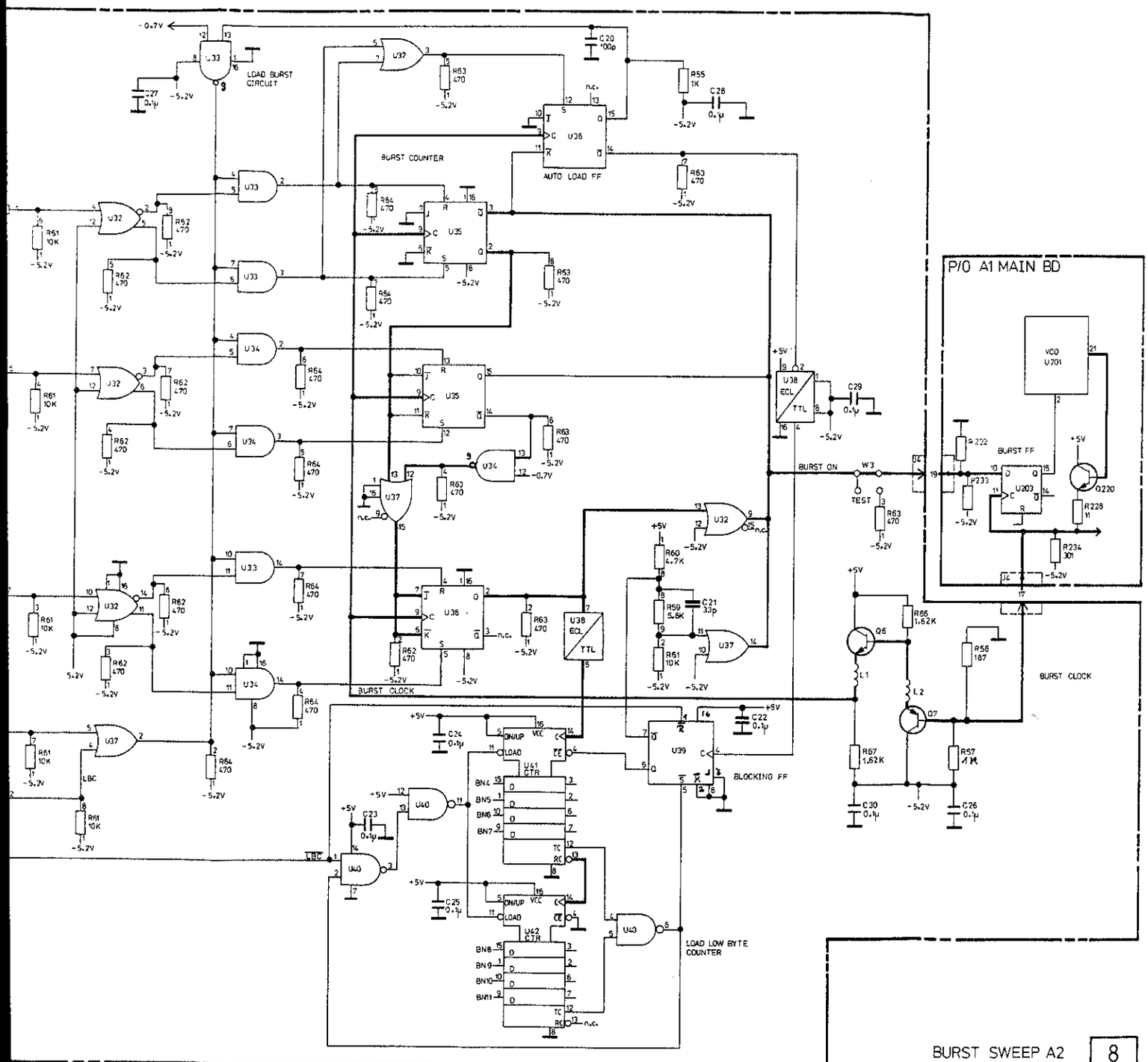


Burst, Sweep Schematic
Sht 1 of 2



8-20e

Burst, Sweep Schematic
Sht 2 of 2



BURST SWEEP A2 8