Service Manual

PCM Channel Measuring Set PCM-4

BN 984/... series A ...

Order No. BN 0984/00.83
Edition 3784/12.89 (3627)

I.11.86 VBS/rth/sl

Wandel & Goltermann
Electronic Measurement Technology

Addendum to PCM-4 Service Manual, BN 0984

Correction to Section 5, figure 5.1.1-15 Display M2, last line of display:

Incorrect:	TX: CHAN. 1	+0.00dBm0	813Hz	Δ = 1
Correct to:	TX: CHAN 1	IDLE FIX.		Δ = 1

March, 27 1992

FIGURES

1 SERVICE CONCEPT

1.1 INTRODUCTION

Maintenance, repairs and calibration are the main tasks involved in servicing a measuring instrument.
All the necessary information is provided in the Description and Operating Manual, together with the Service Manual and the Appendix.

The Description and Operating Manual provides all the necessary information on the instrument, such as technical data, commissioning and notes on measurements. Simple non-electrical maintenance work is also described.

The Service Manual and the Appendix provide all the specific information required for repairs and calibration.
The time taken for fault localization and repair should be as short as possible. Together with the Appendix, the Service Manual offers all the necessary assistance in this context.

Various service tools allow rapid detection of faulty functional assemblies.
Emphasis should be placed on the comprehensive test programs and the monitor program. Depending on the type of fault and the measuring equipment and tools available, these service tools can enable repairs to be made down to the component level.

A simplified repair sequence and the subdivision of troubleshooting into three stages (levels) is shown in Fig. 1.1-1.

In addition to repairs, calibration is also necessary at certain intervals, i.e. verification of the technical data. Section 8 of this Service Manual describes this work in detail.

Test programs are available for efficient functional testing. Please address all enquiries to Customer Service (Department VBS).

The Appendix to the Service Manual contains all the general block diagrams, circuit diagrams and component layout diagrams of the assemblies and circuit boards, together with the corresponding parts lists for ordering spare parts.

Corresponding Section in Service Manual	
No.	Designation
4	Localization to faulty assembly (Top level)
5	Troubleshooting, localization to faulty circuit board (middle level)
6	Troubleshooting, localization to faulty component (Bottom level)
2	Important notes
7	Alignment instructions
8	Verification of technical data

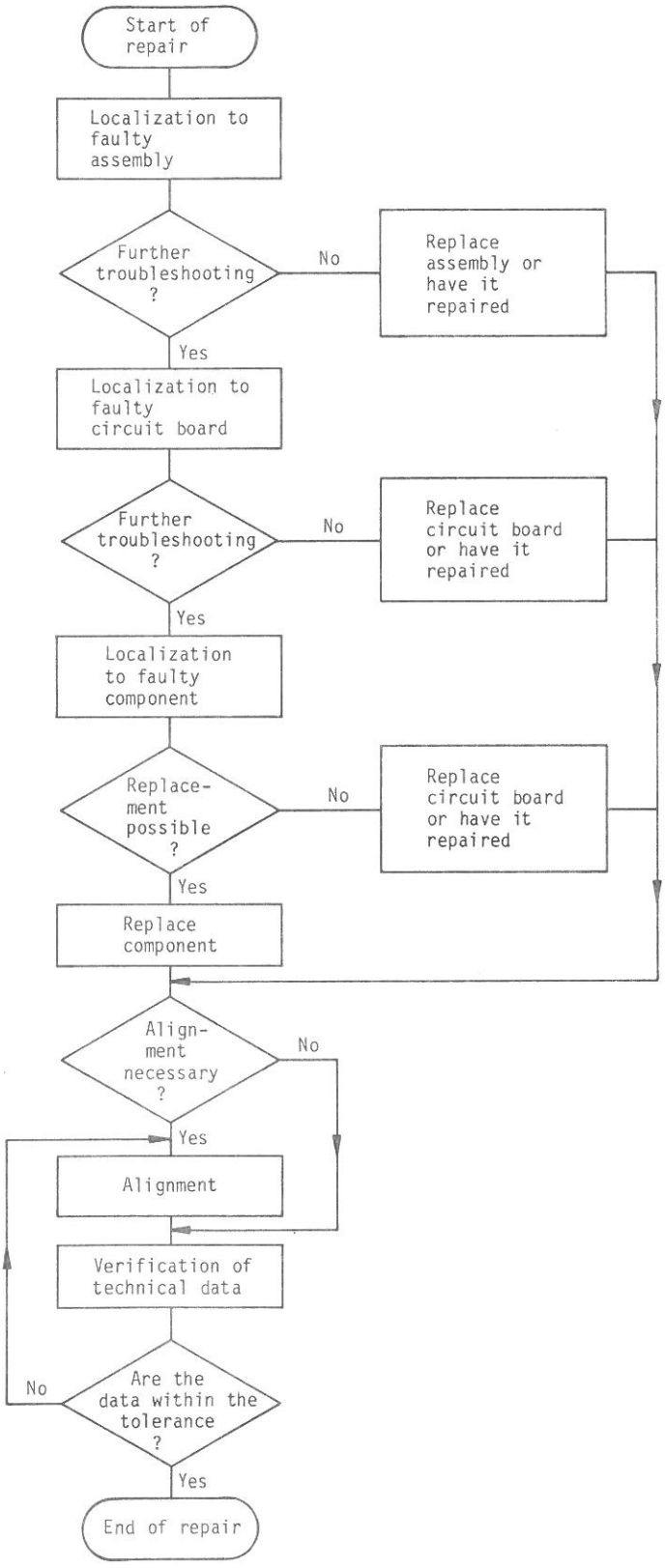


Figure 1.1-1 Repair sequence for a faulty instrument

1.1.1 TROUBLESHOOTING STRATEGY

The right test strategy always starts at the heart, the microprocessor, and works outwards. Refer to Fig. 1.1-2.

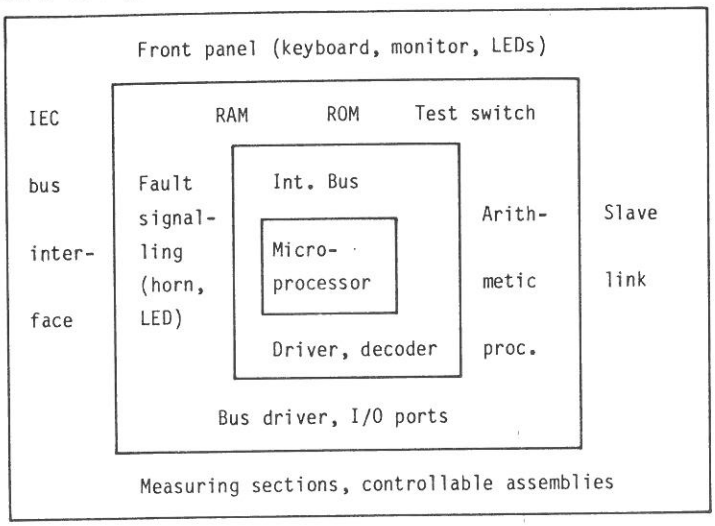


Figure 1.1-2 Test strategy for instruments with microprocessor controller

The Sections on troubleshooting are arranged in the same form as the instrument. This facilitates fault localization.
The following two Sections describe the fault localization strategy, also showing the differences in the measuring equipment required for different objectives - repair down to the component level or only circuit board replacement.

1.1.1.1 Fault localization strategy for assembly or circuit board

(Section 4 or Section 5)

Fault localization tools:

- Measuring equipment: Only simple instruments or auxiliary equipment are required, if any!
- Software tools:
  a) Switching on starts the so-called "Confidence Check". This self-test in the processor section checks the memories, bus systems with drivers and decoders and the arithmetic processor, as well as the most important instrument functions.
  b) Built-in service programs. These programs must be called up separately, either via the front panel keybord or via DIL switches on a CPU board.
  Unlike the Confidence Check, these tests are far more stringent. In some cases, even faulty components can be identified.
  c) The monitor program. This program is operated via the front panel. Gates and memories can be read and written, as well as programs started.

Wherever possible, error numbers or similar displays indicate a certain functional group in the instrument.

1.1.1.2 Fault localization strategy for components

(Section 6)

Fault localization tools:

- Measuring equipment: Depending on the type of fault, the measuring equipment listed (Section 1.2) should be available.
- Software tools:
  a) Hardware-oriented repair programs, cyclic and non-repeating.
  These programs are called up, for example, via the front panel or via DIL switches.
  The "Confidence Check" may also indicate a faulty component.
  b) Free-running of the microprocessor for signature analysis. Troubleshooting in the heart of the microcomputer circuitry (EPROMs, decoder ...).
  c) Stimulus programs for troubleshooting with signature analysis.
  These programs are required in the I/O area, for example.
  d) The monitor program. This can also be a great help in troubleshooting at the component level.

The Circuitry Description in Section 9 of this Service Manual is also of major assistance.

1.1.2 ORDERING SPARE PARTS

Please note the following when ordering spare parts:

- The precise designation can be found in the electrical parts list (Appendix 2).
  Components with BV or WN must be ordered from the manufacturer.

  The following data must be specified in addition to the Order No. (BN):
  - Instrument type and instrument number with Series index
  - Card index or Item No. of the component
  - Item No.

Examples:

Circuit board: PCM-4 BN 984/01
No. A-0062
Card: [984-M]
Software version

Component : PCM-4 BN 984/01
No. A-0062
Component: 2 T 2
(Circuit diag. No.) (Item No.)
Subject No.: 0001-0015.836

Notes on replacing boards:

When replacing card [17] "ADC", only the following combinations in conjunction with card [18] "Analog filter" are permissible for reasons of compatibility:

[984-AR] or [984-K] and [984-J];
[984-AR1] or [984-K1] and [984-J1] (recognizable by the card index on the board).

Similarly, only the following are allowed when replacing analog generator 1:
[984-X] : replace with [984-X1];
[984-X1]: replace with [984-X1] (recognizable by the card index on the board).

The following cards are identical:

[984-U1] = [984-U] from release 5 (PCM-30 Receiver 1)
[984-T1] = [984-T] from release 6 (PCM-30 Generator)
[984-V1] = [984-V] from release 10 (PCM-30 Clock circuit)
[984-AS1] = [984-AS] from release 4 (PCM-30 Receiver 2)

From Series E...

Further notes in Section 10.1.

1.2 MEASURING EQUIPMENT

1.2.1 MEASURING INSTRUMENTS

The measuring instruments listed here as necessary for testing represent a recommendation only. Equivalent instruments from other manufacturers may also be used.

Instrument	Requirements	Rec. Type Order No.	Manufacturer	In Section 4/5	6	7	8
Oscilloscope (with TP 10:1 TP 1:1)	$f_g \geq 100$ MHz	1740 A or 2465	HP Tektronix		x	x	x
Digital voltmeter	4 1/2-digit, accuracy 0.02 % ± 1 digit	8600 A	Fluke			x	
Digital multimeter	5 1/2 digits	3478 A	HP				x
Level meter	200 Hz - 2.5 MHz	SPM-19	W & G				x
Level generator	200 Hz - 2.5 MHz	PS-19	W & G				x
Milliwatt power meter	600 Ω	EPM-1	W & G			x	x
TP	Accuracy 1 mB	TKS-600				x	x
Frequency counter	$T_{resolution}$ = 0.1 µs 800 Hz - 2.5 MHz	HP 5316 A	HP			x	x
Transient recorder or storage oscilloscope	2 channels	TR 940 2430	W & G Tektronix		x		
Transforming attenuator	800 Hz	MOD 1011	EATON				x
Generator	8 kHz ± 25 ppm TTL or 2.37 V	VMS-1 or PCM-4	W & G W & G			x	
Return loss meas. attachment	200 Hz - 2.5 MHz	RFZ-12	W & G				x
Signal balance ratio meas. att.	200 Hz - 120 KHz	SDZ-12	W & G				x
Signature analyzer		5006 A or 5005 A or 5004 A	HP HP HP		x		
Variable attenuator	0 - 60 dB	D 2053	Siemens			x	

Figure 1.2-1 Measuring instruments

1.2.2 AUXILIARY EQUIPMENT

Designation	Rec. Type Order No.	Manufacturer	In Section 4/5	6	7	8
Adapter card, 96-pin	901/00.13 or 901/00.11	W & G	x	x		
Adapter card, 48-pin	[984-AC] 984-7027.001	W & G	x			
Adapter card, 64-pin	[984-BB] 984-7051.006	W & G	x			
3M cable, 20-pin	984-100 984-6500.121	W & G		x	x	
2 x 3M cable, 26-pin	984-36 984-6500.053	W & G		x	x	
Adapter cable, 20-pin	984-102 984-6500.147 (male-female)	W & G		x	x	
Extender cable NT	984-6500.189 984-106	W & G				
Extender cable NT	984-6500.192 984-107	W & G				
Standard resistor for RFZ-12	850 Ω ± 0.1 % 984-6500.066	W & G (40-984)				x
Standard resistor for RFZ-12	900 Ω ± 0.1 % 984-6500.079	W & G (41-984)				x
Standard resistor for RFZ-12	220 Ω + (820 Ω//115 nF) 984-6500.082 R = ± 0.1 % C = ± 1 %	W & G (46-984)				x
Adapter, coax-CF	S 47, S 79					x
Line terminator	75 Ω ± 1 % 984-6500.118	W & G (53-984)				x
1 Bu Subminax-Versacon	S-830	W & G		x	x	
Extension, 8-pin	33-984 984-6500.040	W & G			x	
Group delay test equipment	49-984 984-6500.095	W & G			x	
Subminax cable	K-222	W & G		x	x	
Resistor, 600 Ω	51-984 984-6500.105	W & G		x	x	
Cable, CF-banana	984-6500.176	W & G			x	

Figure 1.2-2 List of auxiliary equipment

1.3 TOOLS

1.3.1 LIST OF TOOLS

Designation	Rec. Type Order No.	Manufacturer	In Section 4/5	6	7	8
Soldering station	WECO/20	Weller				
Soldering tip						
Flat form	ET-B 2.4 mm	Weller				
Flat form	ET-C 3.2 mm	Weller				
Flat form (only in exceptional cases)	ET-L 2.0 mm	Weller				
Flat form	ET-E 6.0 mm	Weller				

Figure 1.3-1 List of tools

2 IMPORTANT NOTES

2.1 SAFETY MEASURES

2.1.1 ELECTRICAL SAFETY

Protection class

This instrument is classified in protection class I to VDE 0411 and IEC Publ. 348. The power cord supplied contains a non-fused earthed conductor. The mains plug may only be plugged into earthed sockets, except in specially approved rooms. The non-fused earthed conductor must not be interrupted either inside or outside the instrument.

Opening the instrument

Live parts may be exposed when covers are opened or parts removed with the aid of a tool. Connecting points may also be live.

The instrument must be disconnected from all power sources before being opened.

If it is essential to perform calibration, maintenance or repair work on the instrument when it is both open and connected to the power supply, such work must only be carried out by a specially trained mechanic who is aware of the potential danger.

Capacitors inside the instrument may still be charged, even if the instrument itself has been disconnected from all power sources; the circuit diagrams must be consulted.

Fuses

Only the specified fuses may be used.

Repairs, replacing parts

Repairs must be performed correctly. Particular care must be taken to ensure that the design features of the instrument are not altered in a manner reducing its safety. On no account must the creepage and air paths or the insulation distances be reduced.

Only use original parts as replacements. Other spare parts may only be used if they do not impair the safety characteristics of the instrument.

Testing after repair and maintenance work

Testing the non-fused earthed conductor

Visually check for correct connection and good condition of the conductor and measure the resistance between the plug connection of the non-fused earthed conductor and the housing. The resistance should be $< 0.5\ \Omega$. Move the connecting lead during this measurement. Fluctuations in the resistance are indicative of damage to the conductor.

Testing the insulation resistance

Measure the insulation resistance between the mains connections and the non-fused earthed conductor at a voltage of 500 V DC. Set the line switch on the instrument to "ON" for this purpose. The insulation resistance should be $> 2\ M\Omega$.

2.2 CIRCUIT PROTECTION

2.2.1 PROTECTION OF MOS COMPONENTS

Be careful when handling MOS components!

A number of MOS (metal-oxide silicon) components are used in this instrument. They can easily be damaged or destroyed by static charges, ripple voltages from unearthed devices or other interference voltages. Damage to the gate insulation does not always lead to immediate component failure, but often only after a certain period of operation. Damage due to static charges can be avoided by noting the following rules:

- Whenever possible, MOS components should remain in the supplier's wrapping until required. All connections must be conductively linked until used (black, electrically conductive foam).
- The electrically conductive part of the packaging must make contact with a reference potential in the form of a conductive worktop or the chassis of the instrument to be repaired before unpacking the MOS components or the circuit boards fitted with such components.
- Before touching the MOS components, touch the conductor acting as reference potential with one hand.
- All tools and instruments, the part to be repaired and the user should have the same potential as the conductor acting as the reference potential (e.g. a conductive worktop or, alternatively, the chassis of the instrument to be repaired). For this reason, first make contact between the reference potential and the tools with which the MOS components are to be handled. Tools must not have insulated handles.
- If work is being carried out on a circuit board or other instrument parts separately from the rest of the instrument and not on a conductive worktop, connect the earth of the circuit board, etc. to the reference potential.

Damage due to ripple voltages during soldering work can be avoided by establishing a permanent connection between the soldering iron and the chassis of the instrument being repaired.

MOS components can be recognized by the letters "MOS", as in CMOS, HCMOS or MOSFET, in the component designations of the electrical parts list.

2.3 MEASURING TECHNIQUE, REPAIR AIDS

2.3.1 NOTES ON OPERATION WITH ADAPTER

The standard adapters specified in the list of auxiliary equipment are used.

Operation of IEC bus card [958-A, B] on adapters can lead to malfunctions or interlocking of the instrument.

When terminating output stage [984-AA, AB] via adapter cable [984-102], pay attention to correct polarity of the output stage multipoint connector.

The cards Analog generator 1 [984-X] and Analog generator 2 [984-Y] can be interchanged in their slots (thus also allowing measurements without adapter on [984-Y]).

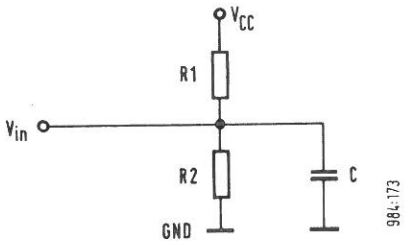
2.3.2 COMPONENT-SPECIFIC MEASURING TECHNIQUE

2.3.2.1 MOS components

This instrument uses both CMOS and HCMOS (high-speed CMOS) modules.

Notes on the measuring technique:

- Only connect measuring instruments after MAINS ON.
  Only disconnect after MAINS OFF.
- Maximum operating voltage:
  HCMOS: $V_{cc_{max}}$ = 6 V CMOS: $V_{cc_{max}}$ = 18 V
- Model of input circuit for $V_{cc} > V_{in} > GND$



R_1, R_2 = Blocking resistors of the protective diodes

Figure 2.3-1 Input circuit

- Outputs
  HCMOS: Not short-circuit proof CMOS: Short-circuit-proof within limits
- Typical switching threshold: See "Transfer characteristic" Figs. 2.3-3 and 2.3-4.

Table 2.3-2 provides an overview of the individual logic families.

GENERAL CHARACTERISTICS (1)

(ALL MAXIMUM RATINGS)

Characteristic	Symbol	TTL			CMOS		Units
		LS	ALS	FAST	14000	Hi-Speed	
Operating Voltage Range	$V_{CC/EE/DD}$	5 ± 5%	5 ± 5%	5 ± 5%	3.0 to 18	2.0 to 6.0	V
Operating Temperature Range	T_A	0 to +70	0 to +70	0 to +70	−40 to +85	−40 to +85	°C
Input Voltage (limits)	V_{IH} (min)	2.0	2.0	2.0	3.5[4]	3.5[4]	V
	V_{IL} (max)	0.8	0.8	0.8	1.5[4]	1.0[4]	V
Output Voltage (limits)	V_{OH} (min)	2.7	2.7	2.7	V_{DD} − 0.05	V_{CC} − 0.1	V
	V_{OL} (max)	0.5	0.5	0.5	0.05	0.1	V
Input Current	I_{in} I_{INH}	20	20	20	±0.3	±1.0	μA
	I_{INL}	−400	−200	−600			
Output Current @ V_O (limit) unless otherwise specified	I_{OH}	−0.4	−0.4	−1.0	−2.1@2.5 V	−4.0 @ V_{CC} − 0.8 V	mA
	I_{OL}	8.0	8.0	20	0.44@0.4 V	4.0@0.4 V	mA
DC Noise Margin Low/High	DCM	0.3/0.7	0.3/0.7	0.3/0.7	1.45[4]	0.90/1.35[4]	V
DC Fanout	–	20	20	33	>50(1)[2]	50(10)[2]	

SPEED/POWER CHARACTERISTICS (1)

(ALL TYPICAL RATINGS)

Characteristic	Symbol	TTL			CMOS		Units
		LS	ALS	FAST	14000	Hi-Speed	
Quiescent Supply Current/Gate	I_G	0.4	0.2	1.1	0.0001	0.0005	mA
Power/Gate (Quiescent)	P_G	2.0	1.0	5.5	0.0006	0.001	mW
Propagation Delay	t_p	9.0	7.0	3.5	125	8.0	ns
Speed Power Product	–	18	7.0	19.2	0.075	0.01	pJ
Clock Frequency (D-F/F)	f_{max}	33	35	125	4.0	40	MHz
Clock Frequency (Counter)	f_{max}	40	45	125	5.0	40	MHz

PROPAGATION DELAY (1)

		TTL			CMOS		Units
		LS	ALS	FAST	14000	HC	
Gate, NOR or NAND:	Product No.	SN74LS00	SN74ALS00	74F00	MC14001B	74HC00	
t_{PLH}/t_{PHL}[5]	Typical	(10)[3]	(5)[3]	3.7	25	(8)[3]10	ns
	Maximum	(15)[3]	10	5.0	250	(15)[3]20	ns
Flip-Flop, D-type:	Product No.	SN74LS74	SN74ALS74	74F74	MC14013B	74HC74	
t_{PLH}/t_{PHL}[5] (Clock to Q)	Typical	(25)[3]	(12)[3]	6.2	175	(23)[2]25	ns
	Maximum	(40)[3]	20	8	350	(30)[3]32	ns
Counter:	Product No.	SN74LS163	SN74ALS163	74F163	MC14163B	74HC163	
t_{PLH}/t_{PHL}[5] (Clock to Q)	Typical	(18)[3]	(10)[3]	7	350	(20)[3]22	ns
	Maximum	(27)[3]	24	10	700	(27)[3]29	ns

NOTES: 1. Specifications are shown for the following conditions:
a) V_{DD}(CMOS) = 5.0 Vdc ± 10% (DC), 5.0 Vdc(AC); V_{CC}(TTL) = 5.0 Vdc ± 5% (DC), 5.0 Vdc(AC)
b) Basic Gates: LS00 or equivalent
c) T_A = 25°C
d) C_L = 50 pF(ALS, FAST, HC), 15 pF(LS, 14000 and Hi-Speed)
e) Commercial grade product
2. ( )fanout to LSTTL
3. ( ) C_L = 15 pF
4. DC input voltage specifications are proportional to supply voltage over operating range.
5. The number specified is the larger of t_{PLH} and t_{PHL} for each device.

Figure 2.3-2 Overview of logic families

Transfer function, standard CMOS

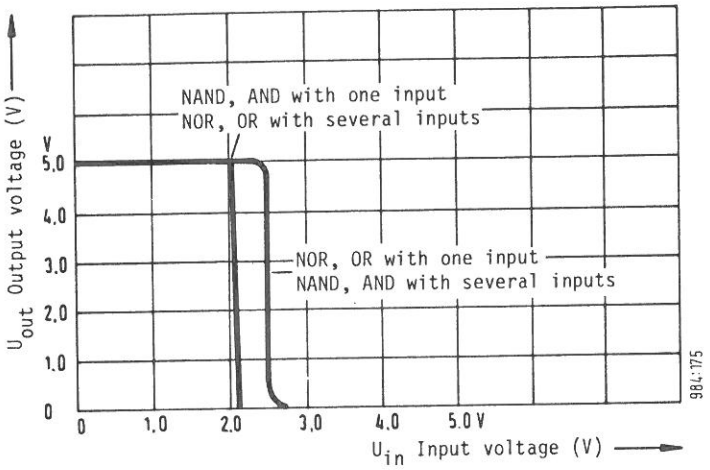


Figure 2.3-3 Standard CMOS transfer characteristic

Transfer function, HC-CMOS

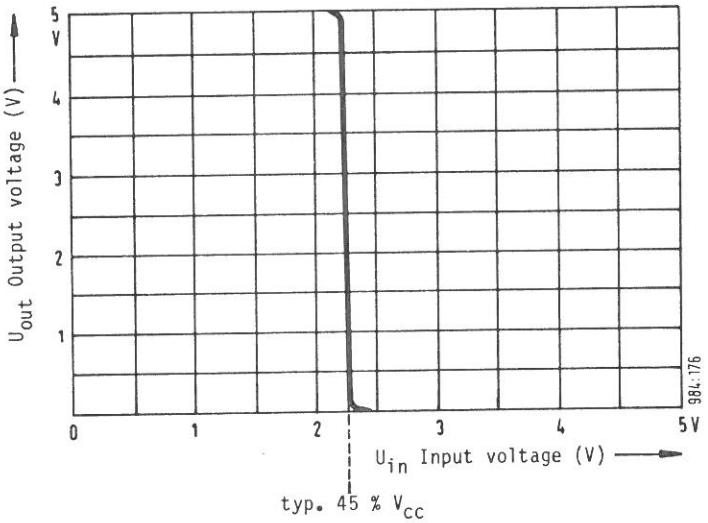


Figure 2.3-4 HCMOS transfer characteristic

There are 3 different types of HCMOS module which must not be interchanged:

Type	Remarks
HC	CMOS input level, buffered outputs
HCU	Unbuffered; input/output levels may deviate from HC types
HCT	With LSTTL-to-CMOS input buffer stage at V_{CC} = 5 V. Outputs fully buffered for driving LSTTL or HCMOS modules

The safety measures described in Section 2.2 must be observed!

2.3.3 SIGNATURE ANALYSIS

A signature analyzer (e.g. hp 5004A/5005A/5006A) can be used for unambiguous and simple checking of digital signal strings of any desired length. Constant signatures are obtained on the lines to be tested if defined and repeatable bit patterns are present in relation to a time window (= START/STOP frame). The bit stream to be measured is sampled via a probe in sychrony with the clock of the unit under test (UUT). If the signature analyzer has a qualifier input, the bit stream can be switched through it, e.g. by chip selection of an EPROM. In this case, the bit stream is then only analyzed within this "window". The resultant bit string is then compressed into a 4-digit display by a process of data compression. The signature analyzer has a built-in 16-bit shift register with feed-back for data compression, into which the data are read. Transfer to the shift register is dependent on the bit combination in the feed-back circuit of the register at the time in question (see Fig. 2.3-5). The shift register can assume a total of 2^{16} (or 65536) possible status combinations via a correspondingly long data stream.

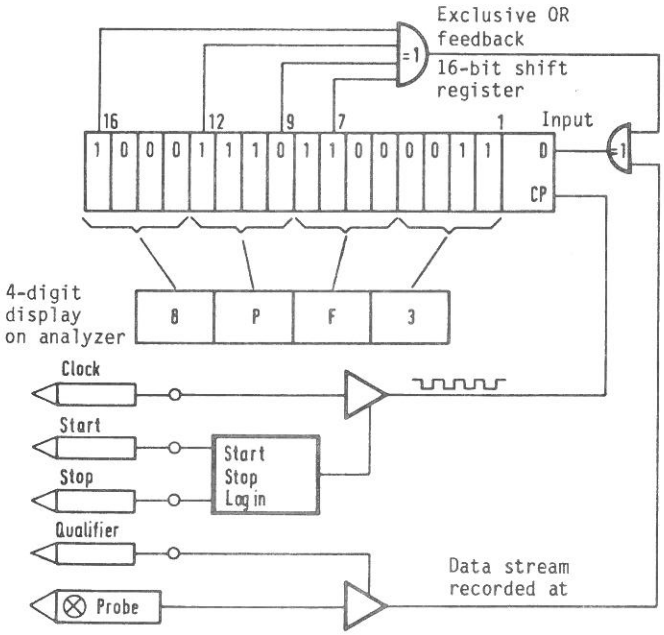


Figure 2.3-5 Elementary circuit diagram of a signature analyzer

This status combination is then decoded, shown in pseudo-hexadecimal form via four 7-segment displays and thus becomes a signature.

This signature now represents the characteristic activity at this circuitry point for a precisely defined period. Any change (e.g. a missing or additional bit, or a time offset in relation to the clock signal) will produce a different signature, thus indicating a fault.

The CLOCK signal used is a signal fulfilling the time conditions RD or WR for the microprocessor. The timing of the CLOCK, DATA, START and STOP signals must be correct, since unstable signatures otherwise occur. Similarly, this timing cannot be guaranteed if signature analyzers other than those recommended by us are used, since they may have different input circuits. Consequently, the signals may deviate from the expected results in these cases.

Two frequently occurring signatures need brief explanation:

The signature of the 0 V line is always 0000, irrespective of the START/STOP frame. The signature of the +5 V line is referred to as the "FRAME SIGNATURE". The frame signature shows whether the START/STOP frame is correctly connected and whether the edges for the START/STOP frame are correct. In addition, it may be assumed that the microprocessor is working.
If the frame signature occurs on an address or data line, this means a short-circuit against the supply voltage; the signature 0000 indicates a similar short-circuit, but to earth. If two address or data lines have the same signature, this is most probably due to a short caused by the lines touching.
In order to obtain meaningful signatures for the RAM and/or I/O area, verifiable contents must first be written into the RAM and the I/O ports then addressed periodically. This can only be done by a program, the so-called stimulus. Such programs can be called up via a switch, for example.

2.3.4 MONITOR FUNCTIONS

The assemblies in this measuring instrument are mainly microcomputer-controlled. The instrument has monitor software to facilitate or enable troubleshooting.

This software contains the so-called WORIS functions.

-W: (Write) Write to memory location
-O: (OUT) Output to a gate
-R: (Read) Read memory location
-I: (IN) Input from a gate
-S: (Start) Start of a program

Section 6 describes how to enter the Monitor Mode in more detail.
The monitor functions are controlled via the front panel keyboard.

2.3.4.1 Description of the basic functions of the monitor software

A command consists of
- a header W:, O:, R:, I: or S:,
- a 2 or 4-digit address field in hexadecimal notation (2-digit for O: and I:),
- a 2-digit data field in hexadecimal notation (only for W:, O: and S:).

The command is entered by pressing the corresponding keys.

"CLR RESLT" key:
The "CLR RESLT" key can be used to delete the last character entered.

"ENTER" key:
Execution of the command is triggered by pressing the "ENTER" key.

The "W:" command: Write to a memory location

Syntax:	W:xyzt.dd xyzt: Address of the memory location (hexadecimal) dd: Data byte (hexadecimal)
Effect:	The data byte dd is stored at address xyzt after pressing the "ENTER" key. Execution of the command is confirmed by the display: "W:xyzt.dd!"
Abbreviated entry	The address and the data byte may be entered with less than 4 or 2 digits. In this case, they are padded with leading zeros (e.g. 3 is interpreted as ØØØ3 or Ø3, respectively).

If a number key (Ø...F) is pressed after operating the "ENTER" key, the address is automatically increased by one and the number accepted as the first digit of the data byte. The second digit of the data byte is then entered in the usual manner.

If the "ENTER" key is pressed twice in succession, the address is automatically increased by one and the same data byte stored at this memory location.

If the /./ key is pressed after operating the "ENTER" key, the address remains unchanged. The data field is cleared and ready for entry of the data byte.

The "O:" command: Output to an output gate

Syntax: O:xy.dd
xy: Address of the output gate (hexadecimal)
dd: Data byte (hexadecimal)

Effect: The data byte dd is output to the gate xy after pressing the "ENTER" key. Execution of the command is confirmed by the display: "O:xy.dd!"

Abbreviated entry: The address and the data byte may be entered with less than two digits. In this case, they are padded with leading zeros (e.g. 3 is interpreted as Ø3).

If a number key (Ø...F) is pressed after operating the "ENTER" key, the address is automatically increased by one and the number accepted as the first digit of the data byte. The second digit of the data byte is then entered in the usual manner.

If the "ENTER" key is pressed twice in succession, the address is automatically increased by one and the same data byte output to this gate.

If the /./ key is pressed after operating the "ENTER" key, the address remains unchanged. The data field is cleared and ready for entry of the data byte.

The "R:" command: Read memory location

Syntax: R:xyzt
xyzt: Address of the memory location (hexadecimal)

Effect: The data byte dd is read from the address xyzt after pressing the "ENTER" key. Execution of the command is confirmed by the display: "R:xyzt.dd!"

Abbreviated entry: The address may be entered with less than 4 digits. In this case, it is padded with leading zeros (e.g. 3 is interpreted as ØØØ3).

If the "ENTER" key is pressed twice in succession, the address is automatically increased by one and its contents read out.
If the /./ key is pressed after operating the "ENTER" key, the address remains unchanged. The data field is cleared. The address contents are read out again after pressing the "ENTER" key.

The "I:" command: Input from an input gate

Syntax: I:xy
xy: Address of the input gate (hexadecimal)

Effect: The contents of gate xy are read out after pressing the "ENTER" key. Execution of the command is confirmed by the display: "I:xy.dd!"

Abbreviated entry: The address may be entered with less than 2 digits. In this case, it is padded with leading zeros (e.g. 3 is interpreted as Ø3).

If the "ENTER" key is pressed twice in succession, the address is automatically increased by one and the corresponding gate contents read.
If the /./ key is pressed after operating the "ENTER" key, the address remains unchanged. The data field is cleared. The gate contents can be read again by pressing the "ENTER" key.

The "S:" command: Starting a program

Syntax: S:xyzt
xyzt: Start address of the program (hexadecimal)

Effect: The program with the address xyzt is called up after pressing the "ENTER" key. Execution of the command is confirmed by the display: "S:xyzt!"

Abbreviated entry: The address may be entered with less than 4 digits. In this case, it is padded with leading zeros (e.g. 3 is interpreted as ØØØ3).

If the "ENTER" key is pressed twice in succession, the same program is called up again.

The "W:" function can be used to write a machine program into a free RAM area for subsequent starting with the "S:" function. Such a program may be, for example, a repeating INPUT function.

2.4 SOLDERING INSTRUCTIONS

2.4.1 SOLDERING ON CIRCUIT BOARDS OF PLATED-THROUGH DESIGN

The use of thin soldering tin with little flux is recommended, e.g. the standard solder "ELSOLD L-Sn 60 Pb Cu 2 C3 F-Sw 32; 3,5%" from Messrs. Bleiwerke Goslar GmbH & Co.

The following points must also be kept in mind:

- The soldering time should not exceed 1 to 3 seconds.
- The best soldering temperature for the above-mentioned solder is 240 to 280 °C.
- In this case, the soldering iron temperature should be about 325 ± 5 °C.
- Broader soldering tips must be used for soldering points with a high heat requirement (e.g. earth connections). If this measure proves inadequate, a more powerful soldering iron must be used (70 W, 100 W).

  Note: The soldering iron temperature must not be increased to cover a higher heat requirement! This is because temperatures in excess of 300 °C cause severe oxidation of the solder; also, the flux loses some of its activity at temperatures above 280 °C. In extreme circumstances, a "cold joint" may still result.

- Avoid flux splashes on switch contacts.
- When soldering on switch contacts or other electromechanical components, try to prevent flux getting onto contacts.

Note on desoldering components with numerous connections:

The best method by far is to remove the solder of each individual connecting wire by suction using special-purpose desoldering equipment. Move the wire gently back and forth while desoldering, to check that each individual connection is free. Do not use force!
Through-platings are sensitive to tensile stresses during soldering!
In the case of dual in-line components, the stress on the circuit board can be reduced considerably by severing the connections on the component side and desoldering the individual connections.

3 MECHANICAL DESIGN, MAINTENANCE

3.1 INSTRUMENT DATA

The following instrument data are required for enquiries, spare parts orders and to establish whether this Service Manual belongs to the instrument to be repaired:

Type designation, designation of the specific model, software version number, options installed, Series index and instrument number.

Fig. 3.1-1 shows where the individual data items are to be found.

3.1.1 IDENTIFICATION OF THE SOFTWARE VERSION

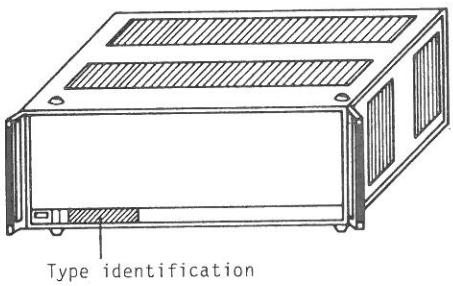
The software version number is entered on the signature list.

When subsequently adding options or new software, it must be ensured that the signature list is amended or replaced, as appropriate.

The software version can be called up with Mode A01 from Series E onwards.

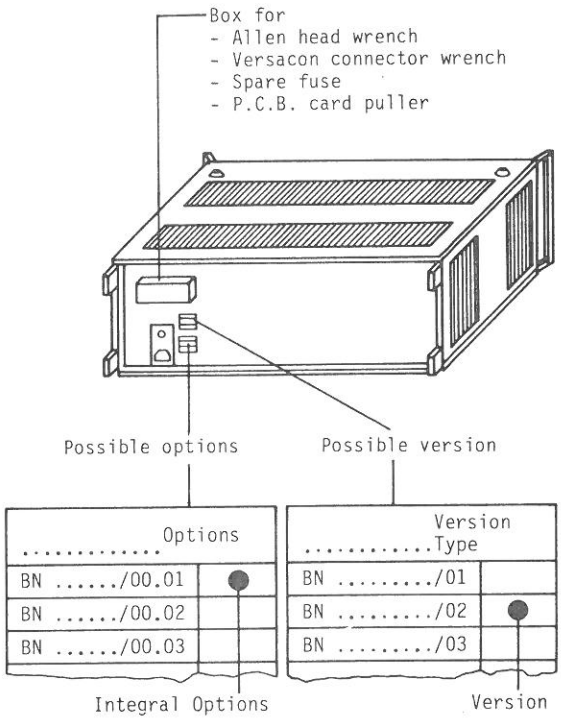
Instrument data:

Front view of instrument



C 0013
- Serial number of instrument
- Series index

Back view of instrument



The version or OPTION is identified by a dot stuck on behind the printed Order No. (BN).

Fig. 3.1-1 Instrument data (see Fig. 10.4-2)

3.2 LOCATION OF ASSEMBLIES

see Fig. 10.4-2

3.3 ASSEMBLY INSTRUCTIONS

3.3.1 OVERALL INSTRUMENT AND HOUSING

To open the overall instrument, remove the Allen screws in the cover and base, then remove the cover, base and left-hand side wall. Assemble in reverse order.

3.3.2 FRONT UNIT, COVER PLATE

Remove the Allen screws in the cover and remove the cover. Lift the instrument chassis up and out of the housing and place it diagonally on top of the housing. Remove the four screws of the cover plate. Remove two screws each on the left and right which hold the cover plate on the inside. Remove the cover plate. Control card [984-C] is now accessible. Assemble in reverse order.

3.3.3 SWITCH PANEL AND PRESELECTION STAGE

Dismantle the instrument as per Section 3.3.1 and stand on the rear housing wall so that the chassis base is visible. Remove the fastening screws shown in Fig. 10.4-3. Carefully pull out the switch panel. Undo the two screws of the mounting plate of the CF sockets. Extend the coaxial cable connection behind this plate with a Subminax cable. Measurements can now be made. For removal, disconnect the ribbon cable and AMP plug. Assemble in reverse order.

3.3.4 PCM-30 INPUT/OUTPUT

Dismantle the instrument as per Section 3.3.1.

Undo the four fastening screws shown in Fig. 10.4-3 and pull the PCM-30 I/O out towards the front. Assemble in reverse order.

3.3.5 OUTPUT STAGE

Dismantle the instrument as per Section 3.3.1. Undo the four fastening screws of the output stage shown in Fig. 10.4-3. Pull out the output stage a short distance and disconnect the 7-pin AMP plug. Pull the output stage all the way out. Connect the output stage and output stage connector card [984-W] with adapter cable (984-102). To do so, connect the adapter cable to the multipoint connector of [984-W] from above. (Pay attention to correct polarity, i.e. 1:1 connection output stage-[984-W]-multipoint connector!)
Re-connect the 7-pin AMP plug to the output stage. Measurements can now be made on the output stage. Assemble in reverse order.

3.3.6 MONITOR

Observe Section 6.1.4 when working on the monitor tube!

Dismantle the instrument as per Sections 3.3.1 and 3.3.3. Remove the PCM-30 I/O (see Section 3.3.4). Disconnect the two ribbon cables (above the tube neck), the black angle connector and the CRT plug. Mark the position of the shielding plate above the tube neck (pencil). Remove the nine screws of "Control" card [984-C], disconnect the ribbon cable at the rear of card [984-C] and remove card [984-C]. Remove the total of four screws on the shielding plate (bent around the tube neck). Two of these screws are accessible from above and two from below through notches above the multipoint connector of the previously removed PCM-30 I/O.

NOTE: Proceed with extreme caution to stop screws or washers dropping into the instrument! (Magnetic screwdriver).

Now undo the four screws to the left and right of the screen from the front. Carefully pull out the CRT towards the front. Carefully disconnect the high-voltage connection (see Fig. 10.4-5) at the same time. The CRT can now be pulled completely forwards and out of the instrument. Assemble carefully in reverse order. (Take care not to displace the deflector unit on the tube neck.)

To remove the Monitor card, BN 980, undo the 4 screws on the back panel (see Fig. 10.4-2 at the end of the Service Manual). Disconnect the CRT plug, angle connector and high-voltage connection on the tube. Pull the card backwards out of the instrument. Assemble in reverse order.

3.3.7 POWER SUPPLY UNIT

Disconnect the mains cable. Remove the instrument cover. Lift out the chassis and disconnect the two connecting cables to the power supply unit (Bu 1 and Bu 4). Remove the right-hand side wall. The power supply unit block can be unscrewed and replaced after desoldering the mains cable on the mains filter (see Fig. 10.4-4). When re-assembling, make sure that the earth conductor is connected correctly! (Also refer to the "Note" to Fig. 10.4-4!)

3.4 INSTALLING OPTIONS

Some of the options are plugged in from the rear of the instrument (see Fig. 10.4-2). The instrument cover must be removed to install option BN 984/00.10 or BN 984/00.11 (measuring bridge). The measuring bridge can then be plugged into the appropriate slot (to the right of the CRT) from above.
The DC decoupling attachment (BN 984/00.13) is plugged into the input/output sockets of the analog section from the front. The DC loop-holding circuit option GH-1 (BN 984/00.12) is connected externally via cables.

3.4.1 INSTALLING THE OPTION LOW-PASS FILTER, 120 kHz, BN 984/00.14

CAUTION!
Only install the filter after measuring the natural frequency response; see Section 3.4.2, Item 1.2.

Measuring instruments required:
SPM-19, PS-19, 2 resistors 301 Ω, 0.1 %.

The option is used to suppress out-of-band interference at approx. 256 kHz.
The interference is attenuated with a low-pass filter, f_g = 100 kHz. The low-pass filter is installed upstream of the input transformer. Resistors R 14 and R 15 must be de-soldered from the board for this purpose. Contact pins (L = 18 mm) must be soldered into the eyelets with the long pin facing upwards. The long hexagonal retaining bolt must be replaced by a bolt of 16.5 mm length. The left-hand M 2.5 screw on the transformer shield must be removed. The retaining bracket must be mounted on the transformer with the threaded hole facing upwards. Now insert the filter board into the contact pins and screw tight with an M 2.5 screw and a hexagonal bolt (L = 17.5 mm). Re-assemble the preselector unit.

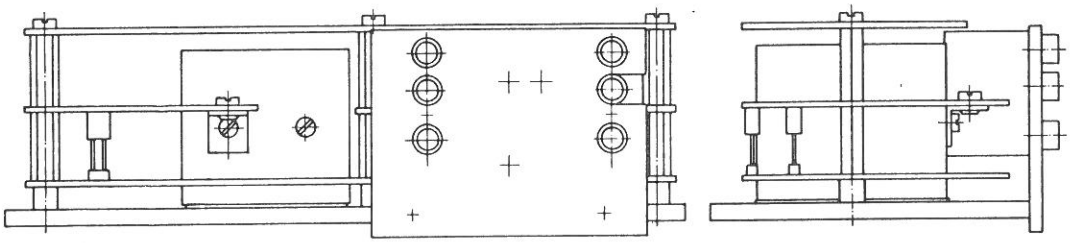


Figure 3.4-1 Option 984/00.14

3.4.2 SHORT TEST

PCM-4/BN 984 with 120 kHz low-pass filter

1.0 Natural frequency response of PCM-4 and SPM-19/PS-19

1.1 Connect PCM-4 generator socket [25] to receiver socket [23].
MA 13, manual/single, L = 0 dB, f = 1 kHz, START
Result displayed: 0 dB ± 0.3 dB

1.2 Connect the test generator PS-19 to PCM-4 receiver socket [23] and the test receiver SPM-19 to analog filter output socket [36].
Use the PS-19 and SPM-19 to measure the frequency response from 1 kHz to 256 kHz. Enter the values in Table 1 (reference frequency = 1 kHz).

1.3 Switch off the instrument! Install the 120 kHz low-pass filter in the preselector unit (see conversion instructions).

2.0 Low-pass filter frequency response measurement

2.1 Switch on the instrument and repeat the measurements under Items 1.1 and 1.2.
Compare the values of measurements 1.2 and 2.1. The calculated difference must lie between the given tolerance values.

Frequency	Measurement a (without filter)	Measurement b (with filter)	Difference (a-b)	Tolerance ≤
1 kHz				± 0.10 dB
2 kHz				"
5 kHz				"
10 kHz				"
20 kHz				"
50 kHz				"
72 kHz				± 0.25 dB
100 kHz				± 2.00 dB
120 kHz				± 3.50 dB
256 kHz				≥ 34 dB

Figure 3.4-2 Table for short test

3.0 PCM-4 signal balance ratio measurement with low-pass filter

3.1 Connect the PS-19 level generator to receiver socket [23] via two resistors 301 Ω, 0.1% (see sketch).
MA 13, manual/rep., START
Measure the signal balance ratio at f = 72 kHz. Required value = > 40 dB.
If this value is exceeded, adjust to maximum attenuation with trimming capacitor 2C2 in the preselector stage.

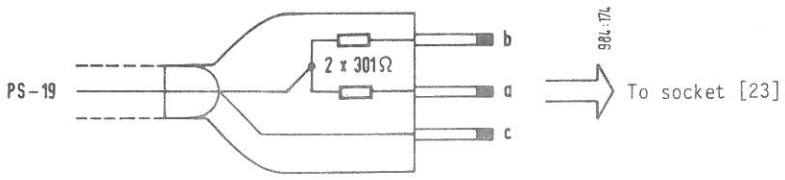


Figure 3.4-3 Auxiliary equipment, Item No. 984-6500.176

3.5 MAINTENANCE WORK

3.5.1 STORAGE BATTERIES

To replace the storage batteries, lift the instrument chassis up and out of the housing. The storage batteries are located on the power supply unit block and can be replaced after removing the retaining bracket. Assemble in reverse order.

3.6 CLEANING WORK

Front panel and housing must not be cleaned with solvents:

- Solvents (e.g. naphtha or methylated spirit) may dissolve the lettering and impair the sharpness of its contours.
- Cleaners for plastic surfaces and furniture often have a polishing effect. They may damage the lettering and leave shiny marks on the cover plate.

The simplest cleaning liquid is warm water with a little added washing-up liquid. The cloth wetted with this water must only be damp. On no account must water be allowed to drip into the instrument. In order to avoid stripes and spots, the instrument should be wiped off with a dry cloth while still damp.

The CRT cover should only be cleaned damp, in order to avoid scratches and static charges.

Trifluoro-trichloroethane (TTE) can also be recommended for cleaning. TTE is non-inflammable, virtually non-toxic and odourless. It is an excellent solvent for all greases and oils, but does not attack paints and plastics. It is available under the tradenames Freon, Kaltron, Frigen and Flugène.

4 TROUBLESHOOTING: LOCALIZATION TO FAULTY ASSEMBLY

This Section contains a brief description of the self-test, a flowchart (with the aid of which the faulty assembly can usually be identified), a breakdown of the "Error page" displayed in the event of a fault, and a brief description of the monitor functions. (In this respect, reference is also made to Section 2.3.4, which contains a detailed description of the monitor functions and their operation.)
The last part of this Section describes the operation for polling the software version.

4.1 NOTES ON TROUBLESHOOTING

Generally speaking, the PCM-4 is capable of testing the most important instrument characteristics itself without additional auxiliary equipment. This is achieved by connecting analog input [23] and analog output [25] via a CF cable and selecting certain measurement modes via the keyboard. Measurements in these modes yield precisely defined results. Deviating results permit conclusions to be drawn as to the nature, location and severity of a fault.

A fundamental distinction must be made between faults affecting the control sequence and aspects relating to the parameters and those occurring in the area of the actual analog or digital measuring path.
The former are subsequently referred to as "Faults in the control section", the latter being called "Faults in the analog section" or "Faults in the digital section".

4.1.1 START OF TROUBLESHOOTING, STRATEGY

It is best to start troubleshooting by considering whether the fault observed is to be found in the control, digital or analog section. To facilitate this decision, a short test of the control section (PCM-4 self-test) is run first. If passed successfully, it is followed by a short test of the measuring sections (Section 5.1), after which the other tests on the measuring sections are performed, etc.

There is certainly a fault in the control section if the self-test (CPUs, coupler) as per Section 4.2 does not run in the manner described. In this case, a check of the control section in accordance with Section 5.2 will lead to further localization of the fault.

There is certainly a fault in the analog or digital section (measuring section) if the test as per Section 5.1 does not run in the manner described after a successful self-test.

Faults in transmission between the control section and the measuring sections or vice versa can usually be located by using the test in Section 5.1. Thought as to whether the fault affects the "Generator" or the "Receiver" in the measuring sections leads to closer localization. This is primarily achieved using the possibility described in Section 4.1 of circumventing calibration by holding down the "9" key when switching on the instrument. In this case, all correction values are set to zero.

If the above steps do not allow unambiguous localization of the fault, the following general "recipe" applies:

- Observe the reaction of the measuring sections in the event of a fault in a certain situation (e.g. divider setting for MA 11).
- Did this reaction occur as a result of a "command" from the control section via the data bus?
  If "Yes": Fault in transmission or control
  If "No" : Fault in the measuring section

Two adapters [984-AC] and 901/00.13, one oscilloscope, f_{gr} = 100 MHz, and one test probe are required as auxiliary equipment for this purpose.

4.2 PCM-4 SELF TEST

4.2.1 DESCRIPTION

A self-test is performed automatically after switching on the instrument. The sequence and error signals (visual and acoustic) are shown in the structural diagram (Fig. 10.5-1 at the end of the Service Manual). The selection of the indicators used for the error messages (horn, lamp, screen) is predefined by the sequence of their own successful testing. The master CPU-2A/1 and coupling card 2 are tested first. The second test phase checks the transmission of data between the master CPU-2A/1 and the two slave computers (CPU-2A/2 and CPU-2/3).

In the third and fourth test phases, the slave computers check their ROM and RAM areas, as well as their lower-ranking control cards. These are the screen control card on the CPU-2A/2 and the evaluation circuit for CPU-2/3.

The fifth test phase includes the test of the clock and clock signal generation on coupling card 2.
Analog calibration is displayed on the screen in large letters. Calibration cannot be performed if analog assemblies are faulty or subject to excessive tolerances. In this case, an "Error display" appears, which permits conclusions to be drawn as to the nature and location of a fault. The list of error codes can be found in Figs. 4.3-1 and 4.3-2.

If the program is in the "Error display" status as a result of an error message, it can be continued by pressing the uppermost softkey (S 17) for > 3 seconds. However, measurement results may be incorrect in this case.

The final test phase consists of a test of the key pad (sticking keys).

The calibration phase can be avoided when switching on the instrument by holding down the "9" key while switching on. In this case, all correction values to be determined during calibration are set to zero. Since the absolute values for divider, amplifier and basic attenuation become active without correction, conclusions as to the location of the fault can be drawn in the event of service work. Above all, it is now possible to attribute a fault to the generator or receiver section, whereas, if normal calibration takes place, for example, a fault in the "receiver section" might be carried into the correction of the "generator section" and thus possibly lead to misinterpretations.

Details of the calibration phase can be found in Section 4.3.

If the instrument does not get to the calibration phase when switched on, the fault can be localized more closely in accordance with Sections 5 and 6, particularly Section 6.1.1 (Cyclic self-test).

4.3 ERROR PAGE

Interpretation of error messages:

An "X" appears in the display if:

- Δ a $\geq \pm$ 1 dB for dividers and amplifiers
- Δ a $\geq \pm$ 2 dB for pass-band attenuations
- Offset $\geq$ 100 digits

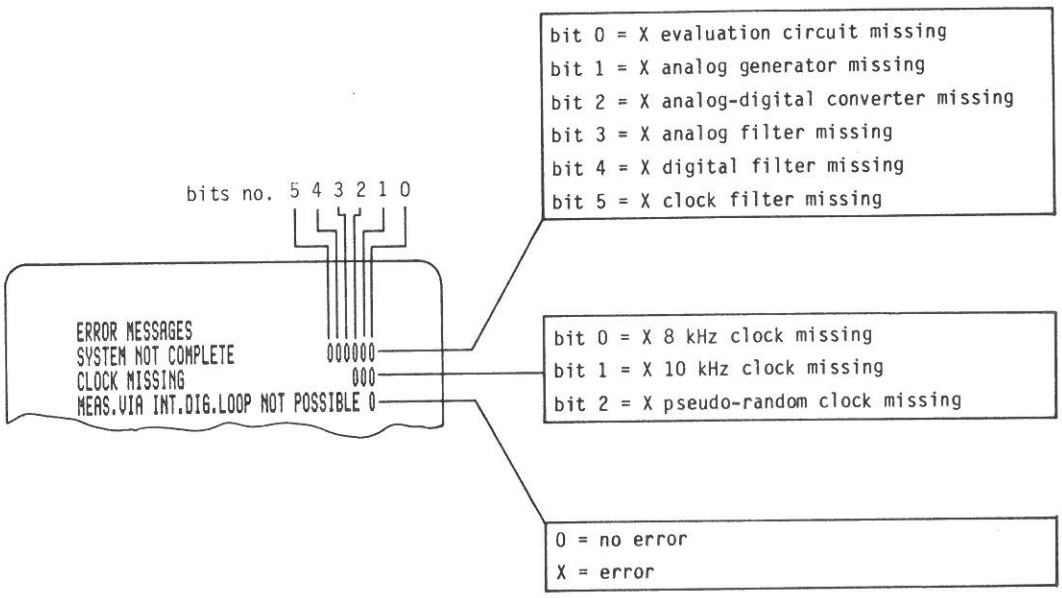


Figure 4.3-1 Error messages, Part 1

SYSTEM INCOMPLETE:

Whether or not the individual cards are fitted is established by polling whether certain PINs (e.g. "DIGITAL FILTER fitted") are connected to earth or by polling gates on the cards to be identified.

MISSING CLOCK:

Apart from clock generation, the paths for the 8 kHz/10 kHz clocks are identical.
8 kHz generation : VCO (T1, T2) with "8 kHz PDA" as reference signal on Clock filter card [984-L].
(For DD measurement) f = 4.096 MHz at Pt. 3 b.

10 kHz generation: Crystal oscillator 052 (10.24 MHz) on Clock filter card [984-L].
(For AA measurement) f = 5.12 MHz at Pt. 3 b.

Further processing is identical in both cases:
At TP 4 4.096 MHz or 5.12 MHz on Digital filter card [984-F]. f/2 is present at IC 3/3.
Via IC 6/9 to binary counters IC 8, IC 7 (f = 256 kHz or 320 kHz at IC 8/15).
At IC 7/11 f = 16 kHz or 20 kHz.
Via IC 3/5 and IC 6/7 f = 8 kHz or 10 kHz present at Pt. 28 b.
Via "Data valid", IC 42/5, IC 43/2, IC 43/12 (TP 16), the signal "Data valid LSB" (20 c) passes to Evaluation circuit card [984-M] (8 b).
Via IC 29, the CPU monitors the presence of the corresponding clock.
The pseudo-random clock is completed by means of IC 26 to IC 32 (see Section 9.2.10).

INT. DIG. LOOP MEAS. NOT POSSIBLE:

Digital loop:
PDG-64 -> Clock filter -> Digital filter -> Evaluation circuit
The signals "8 kHz PDA" (28 a), "64 kHz PDA" (29 a), "64 kbit/s PDA" (27 a) arrive from the PDG-64 [984-H] and are passed to Clock filter [984-L] Pt. 3 c, 2 b, 4 c.
The 64 kHz clock is used to read the 64 kbit/s signal into IC 13, the "8 kHz PDA" clock loading it byte by byte into IC 16,20.

For further processing, refer to Section 9.2.10.

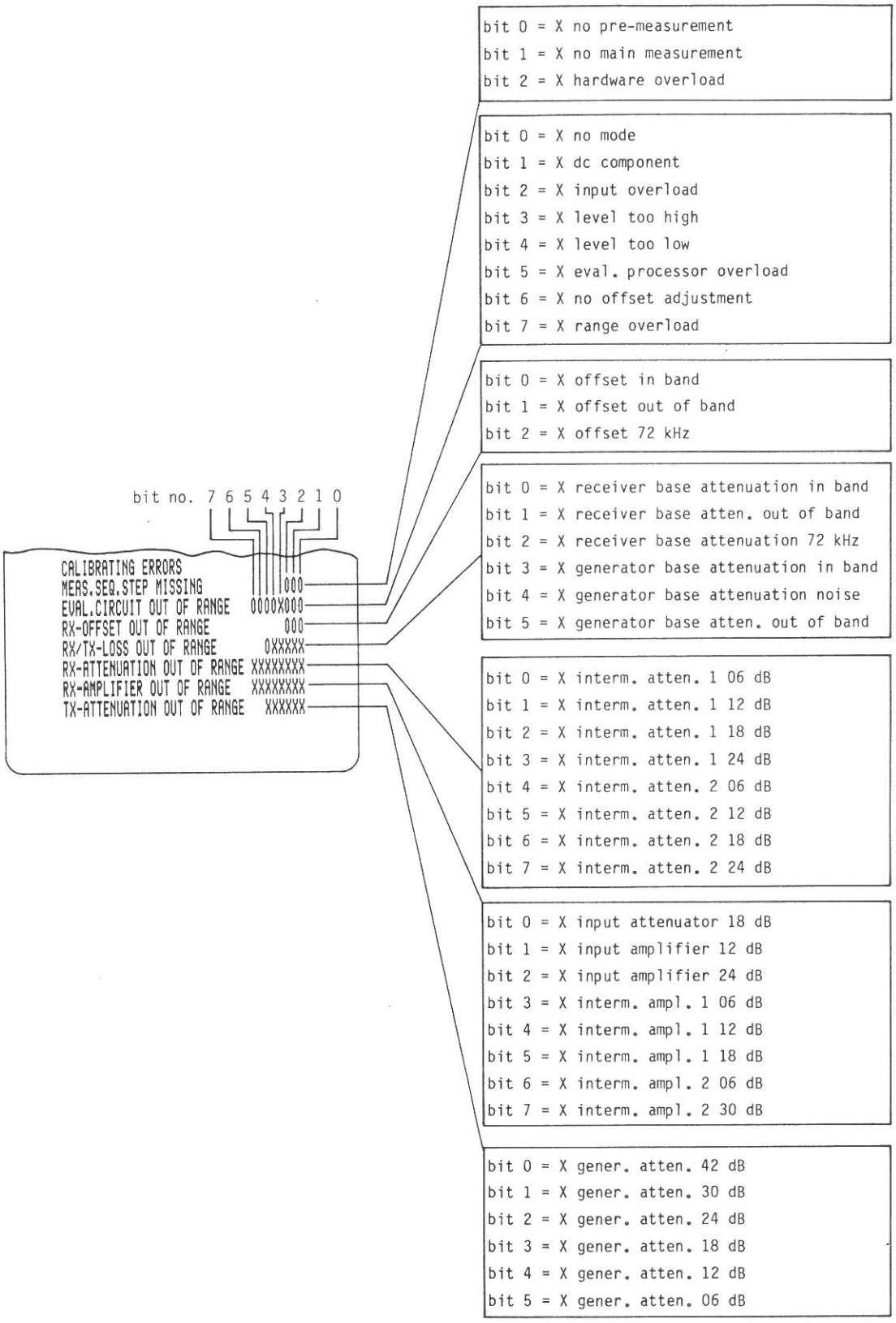


Figure 4.3-2 Error messages, Part 2 (calibration)

Exiting the error page:

The following applies for instruments up to Series D:

- The error page cannot be exited following faults in the system test (see Fig. 4.3-1).
- Following faults in calibration, the error page can be exited by holding down softkey "A"* for approx. 5 seconds. The system then jumps to the "Mode list A" page.

The procedure is as follows from Series E onwards:

1. Hold down softkey "A"* for approx. 5 seconds.
2. Press key "Mode list A" or "Mode list B" or "Genrl. Reset".

The system exits the error page.

* Softkey "A" is the uppermost key of the six vertical keys to the right of the screen.

4.4 TROUBLESHOOTING WITH THE MONITOR FUNCTION

4.4.1 SWITCHING ON MONITOR CONTROL

The PCM-4 provides two methods of entry:

a) When switching on the instrument, press key "0" until the horn sounds. The monitor program is switched on automatically.

b) If the instrument is in an operating mode, e.g. MA 11 ("Results page"), the monitor program can be switched on by pressing the VAR. MODE key and then holding down the uppermost softkey for approx. 4 to 5 seconds.

Note: When using method "a)", the RTN softkey has no function.

The difference between monitor V002 and monitor V003 is that the 3 CPUs can be selected individually in version V003 (CPU-2/1, CPU-2/2, CPU-2/3). Selection is accomplished by "paging" with the softkey [CPU ↑] (≙ Digit word). The current position or selected CPU is displayed. When working (pressing the softkeys WRITE ... START) with the monitor, the display of the selected CPU is deleted.

Monitor V003 is entered via VAR. MODE by pressing one of the top three softkeys for several seconds.

Softkey A -> Monitor area of CPU-2A/1
Softkey B -> Monitor area of CPU-2A/2
Softkey C -> Monitor area of CPU-2/3

A detailed description of the monitor functions can be found in Section 2.3.4.

4.4.2 SCREEN DISPLAY OF MONITOR V002

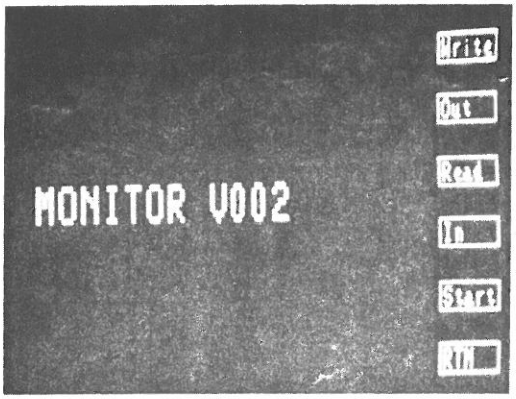


Figure 4.4.2-1 Basic display, monitor V002

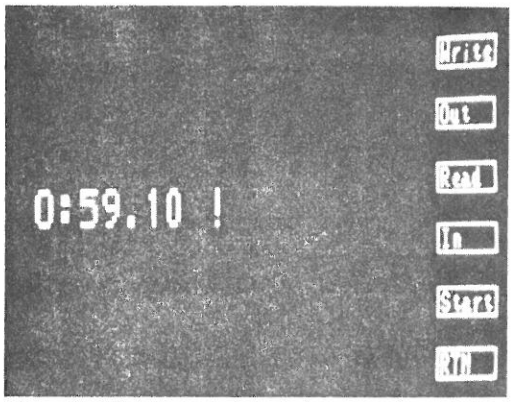


Figure 4.4.2-2 Example of a gate output

Selected: Mode OUT
Address: 59
Data: 10 H
Confirmation of data transfer
after "Enter" by "!"

4.4.3 SCREEN DISPLAY OF MONITOR V003

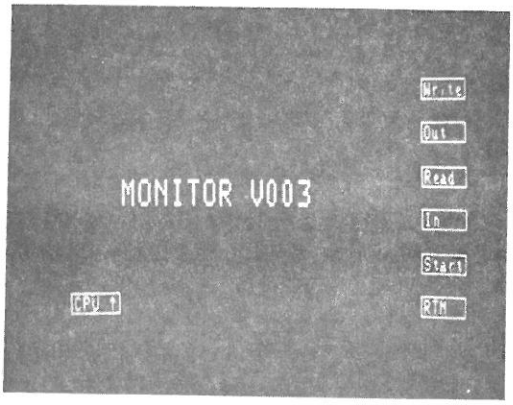


Figure 4.4.3-1 Display after switching on monitor V003

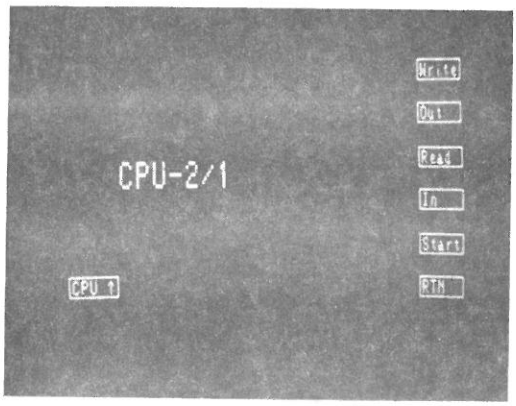


Figure 4.4.3-2 Display after selecting CPU-2/1 (= control circuit)

Options: CPU-2/1 = Control circuit
CPU-2/2 = Display circuit
CPU-2/3 = Measuring circuit

4.4.4 DOUBLE KEYBOARD ASSIGNMENTS

In order to allow entry of HEX numbers, the following keys are defined as letters in the monitor program:

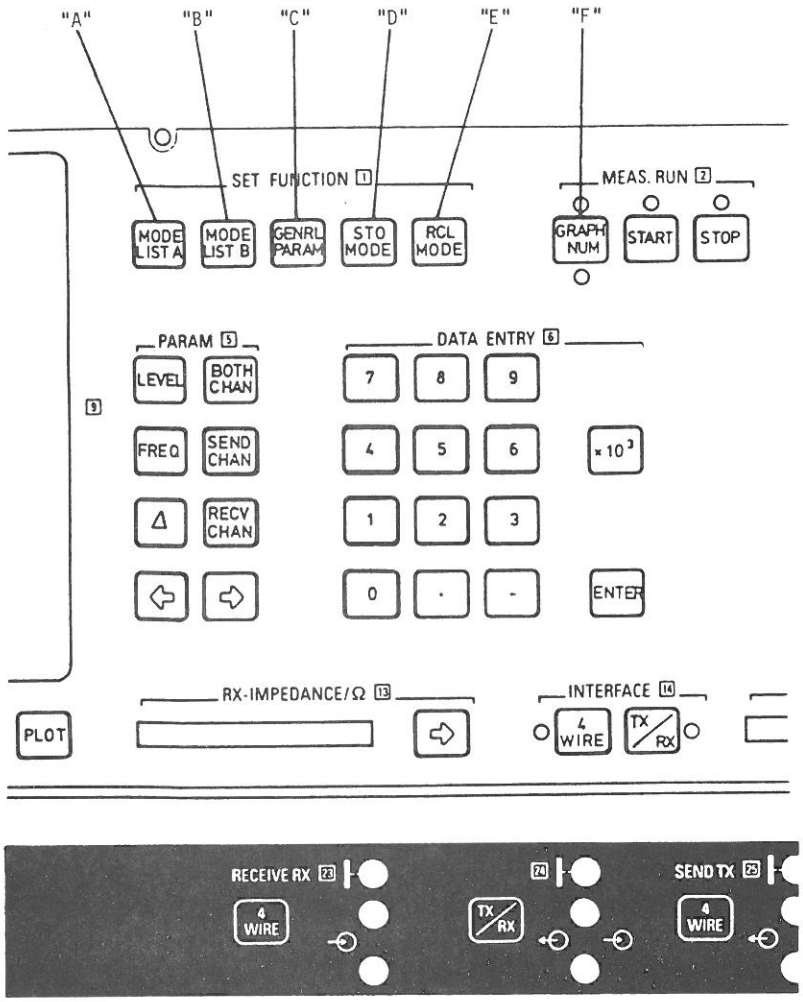


Figure 4.4.4-1 Keyboard assignments

4.4.5 SUMMARY OF MONITOR COMMANDS

Write: Write data into memory

Out : Write data into output ports

Read : Read memory cell

In : Read input ports

Start: Start program from entered address

Note: Before a monitor command is executed, it must be ensured on the basis of the memory allocation (see Section 4.4.7) and gate assignments (Section 10.2) that the command in question may be exucuted at the selected point!

4.4.6 INTERPRETATION OF THE ADDRESS DESIGNATIONS IN THE APPENDIX (CIRCUIT DIAGRAMS)

Rxxxx
or
Rxx
$\overline{\text{Rxx}}$
} ≅ READ address xx

e.g. $\overline{\text{R33}}$ ≅ Read data from address 33 (clock)

Wxxxx
or
Wxx
or
$\overline{\text{Wxx}}$
} ≅ WRITE address xx

DADxx ≅ Measuring circuit OUT address xx
MWxx ≅ Measuring circuit WRITE address xx
MRxx ≅ Measuring circuit READ address xx

In some circuit diagrams (e.g. analog generator), only the addresses are shown.

In principle, block circuit diagram (0) shows which computer CPU can access which circuits via its own I/O bus.

4.4.7 MEMORY ALLOCATION

The absolute addresses are not shown in the diagram of the RAM memory areas, since the allocations may differ from one software version to the next.

Address pointers are stored in the master PROM area for the common data fields; they each point to the start of the data fields (see Fig. 4.4.7-1).

INTDAT*, MINTDAT*, SINTDAT* are the CPUs' own data fields. The SINTDAT* data fields of the display circuit are, with a few exceptions, identical with those of the memory expansion. Each time the banks are switched, the display circuit takes the necessary data from one bank to the other.

The two STACKs shown for the display circuit are different. The display circuit has a total of 4 STACKs.

---

* INTDAT, MINTDAT, SINTDAT are designations only used here.

Address list for data fields

```
ADRTAB      ORG    090
          90 DW     MESSART            ; Start of SETTING DATA
          92 DW     MESSERGEBNIS       ; Start of RESULT FIELD
          94 DW     TRGADR
          96 DW     LOCADR
          98 DW     REGPSW
          9A DW     TFEHLR             ; Error status word for test programs
          9C DW     TOL_MASK           ; Variable pointer for external tolerances
          9E DW     TOL_LIST           ;         -"-
          A0 DW     TOLWERT            ;         -"-
          A2 DW     TOL_L_INDX         ;         -"-
          A4 DW     TOL_INDX           ;         -"-
          A6 DW     MESSERGEBNIS_2     ; Address for further results from AWR
          A8 DW     ANA_SIGNAL_GEN     ; Start of VARMO_DATA
          AA DW     HAUPTZUSTAND       ; Start of SEQUENCE_DATA
          AC DW     ERG_FERTIG         ; Start of SCALE_DATA
```

Figure 4.4.7-1 Address list

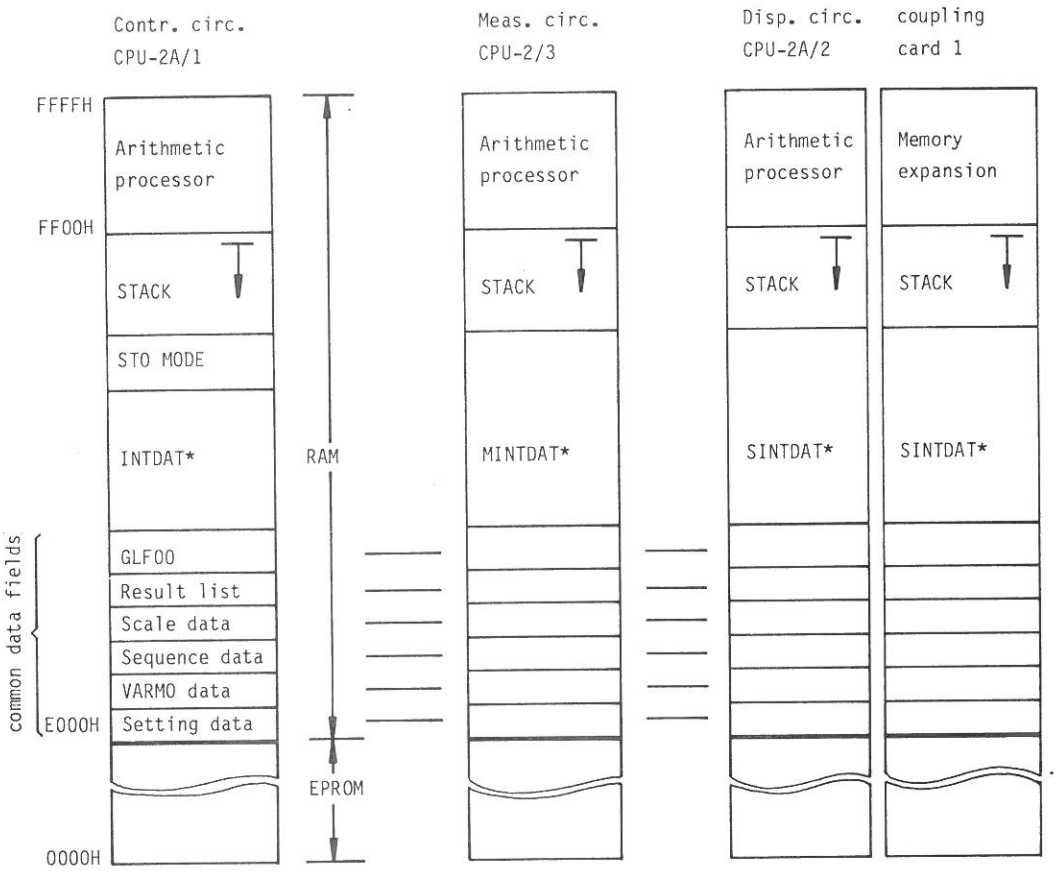


Figure 4.4.7-2 Memory allocation

4.4.8 PCM-4 SOFTWARE IDENTIFICATION

The identification of the software status is stored in the so-called descriptor list in the MASTER CPU, starting at address 40 H.

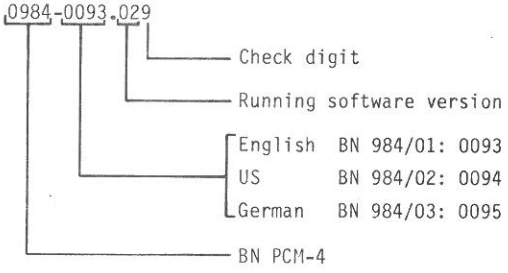
The identification has the following format:

"0984-009X.XXX", CR, LF*
"WANDEL & GOLTERMANN", CR, LF
"PCM-4", ETX

CR, LF, ETX are ASCII control characters.

Line 1 contains the BV No. of the signature lists for the current software status.

Example: 0984-0093.029



The identification can be read out via

1. the IEC bus (WORIS function "W: 0040"),
2. the built-in monitor.

Reading via built-in monitor

MODE A	1	1	ENT	Set mode A 11 (result page)
VAR MODE				Select VAR. MODE selection page
KEY A				Press softkey A for approx. 5 s -> MONITOR
READ	4	0	ENT	The first character of the identification
			ENT	then appears. The output is the hexadecimal
			.	representation of the ASCII code.
			.	
			ENT	

* The number depends on the software version involved

Output format:	Example:
	↓
R:0040.30 !	0
R:0041.39 !	9
R:0042.38 !	8
R:0043.34 !	4
R:0044.2D !	-
R:0045.30 !	0
R:0046.30 !	0
R:0047.39 !	9
R:0048.33 !	3
R:0049.2E !	.
R:004A.30 !	0
R:004B.32 !	2
R:004C.39 !	9
R:004D.0D !	CR
R:004E.0A !	LF

From Series E onwards, the software identification can be displayed on the screen by means of "MODE A01" "Enter".

5 TROUBLESHOOTING: LOCALIZATION TO FAULTY CIRCUIT BOARD

This Section describes the localization of a fault to a faulty circuit board by means of a short test program, as well as the major control functions and most important signal paths in the instrument.

5.1 PCM-4 SHORT TEST

5.1.1 SHORT TEST OF THE ANALOG AND DIGITAL MEASURING SECTIONS (Fig. 5.1.1-1)

MAINS ON
Instrument runs self-test

Self-test o.k.?

Yes:

- GEN.RESET [10]:
  Connect [23] to [25]

- MA 11 ENTER, [A-A]
  Run parameter "LEVEL"
  Mode "SWP/S"
  Δ = 1 dB ENTER
  START

Display A o.k.?

Yes:

- MA 14 ENTER, [A-A]
  Mode "SWP/S"
  Δ = 1 dB ENTER
  START

Display B o.k.?

Yes:

- MA 31 ENTER, [A-A]
  Y top + 0.2 ENTER
  Y bottom - 0.1 ENTER, RTN
  Mode "SWP/S"
  START, LINK RESLT

No:

Fault classification as per "Error messages" Table. The sequence of the tests and their priorities approximately match the sequence in the "Error messages".

See Sec. 4.3

No:

- Level shift over entire measurement range: Basic attenuations wrongly stored. Level shift in parts of the range: Ref. divider (input 1) faulty. Divider correction values wrongly stored.

See Sec. 6.3.2 a)

No:

- Clock for 8 kHz noise generator missing!

See (22)

Display C o.k.?

Yes:

- MA 41 ENTER, [A-A]
  Y top + 0.2 ENTER
  Y bottom - 0.1 ENTER, RTN
  X top + 10 ENTER
  X bottom - 77 ENTER, RTN
  VAR MODE <521>
  - 120 dBm ENTER, RTN
  Mode "SWP/R"
  START
  Wait approx. 10 sweeps
  then
  STOP

No:

- Component fault on (18) in range TP 4 kHz

Display D o.k.?

Yes:

- MA 51 ENTER, [A-A]
  Y top + 70 ENTER
  X bottom - 77 ENTER, RTN
  Mode "SWP/S"
  START, LINK RESLT

No:

Offset correction working incorrectly.
Settling problems in presel. stage/input 1
Offset of analog generator too great at $\geq$ -30 dBm0

See Sec. 6.3.2b and 6.3.2d

Display E o.k.?

Yes:

- MA 52 ENTER, [A-A]
  Y top + 70 ENTER
  X bottom - 77 ENTER
  X top + 13 ENTER, RTN
  Mode "SWP/S"
  START, LINK RESLT

No:

- Amplifier in preselector stage/input 1 unacceptably noisy or oscillating.
  ADC: Faulty stage.
  Natural ratio too small.
  Analog gen.: Output filter attenuation inadequate.

Display F o.k.?

Yes:

- MA 11 ENTER [A-A]
  Mode "MAN/R"
  VAR MODE <521>
  - 120 dBm ENTER, RTN
  Bu [23] open
  START

No:

- As for MA 51

Display $\leq$ -103 dB?

Yes:

- STOP
  VAR MODE <312> ENTER, RTN
  START

No:

- Amplifier in preselector stage/input 1 unacceptably noisy or oscillating.
  Fault in power supply unit?

Display $\leq$ -87 dB?

Yes:

- STOP
  MA 83 ENTER, [A-A]
  VAR MODE <521>
  -120 dBm ENTER, RTN
  Mode "MAN/R"
  Bu [23] open
  START

No:

- Power supply unit supplies ripple voltage.
  Stray field carrier in power supply unit; inadequate input transformer screening;
  50 Hz interference from frame sweep of monitor (93)

Display ≤ -75 dB?

Yes:

- STOP
  MA 13 ENTER, [A-A]
  VAR MODE <521>
  -120 dBm ENTER, RTN
  Mode "MAN/R"
  Bu [23] open
  START

Display ≤ -80 dB?

Yes:

- Instrument has no detectable major [A-A] fault; if necessary, define fault more closely!
- TESTS of the digital measuring assemblies follow.

END OF ANALOG TEST

- GENERAL RESET
- Connect [20] to [21]
- MA 11 ENTER [D-D]
  Run parameter "LEVEL"
  Mode "SWP/S"
  Δ = 1 dB ENTER
  START

Display G o.k.?

Yes:

- MA 31 ENTER [D-D]
  Y top + 0.2 ENTER
  Y bottom - 0.1 ENTER, RTN
  Mode "SWP/S"
  START, LINK RESLT

Display H o.k.?

Yes:

- MA 41 ENTER [D-D]
  X top - 30 ENTER
  Y top + 0.5 ENTER
  Y bottom -0.5 ENTER, RTN
  Mode "SWP/S"
  Δ = 0.1 dB ENTER
  START, LINK RESLT

Display I o.k.?

Yes:

- MA 51 ENTER [D-D]
  Mode "SWP/S"
  START, LINK RESLT

No:

- Switch-mode power supply unit supplies noise voltage;
  16 kHz interference form line scan of monitor;
  common-mode alignment of input 1 incorrect;
  amplifier in presel. stage/input 1 oscillating.

No:

- As for MA 83

No:

- PDG-64 (22) operating incorrectly;
  evaluation circuit operating incorrectly;
  increased test stringency over self-test!

No:

- No filter or wrong filter activated

No:

- A/μ-law interchanged on generator and receiver = mixed mode

---

Display K o.k.?

Yes:

- MA 52 ENTER [D-D]
  Mode "SWP/S"
  Δ = 0.1 dB
  START, LINK RESLT

  (can be carried out with
  Δ = 0.5 dB to save time)

No:

- Test stringency of self-test inadequate.
  Spec. level settings not possible with PDG-64.

Display L1, L2 o.k.?

Yes:

- MB 45 ENTER [D-D]
  NUM, SWP/S
  L = 0 dBm0 ENTER
  START, then

No:

- Same remarks as for MA 51!
  Since theoretical values must be reached here, a general fault must be present in the program sequence or the PDG-64.

Display M1 o.k.?

Yes:

- VAR MODE <251> (000)
  ENTER, RTN
  START, then

No:

- Major fault in program sequence:
  μ-law instead of A-law?

Display M2 o.k.?

Yes:

- B 41 ENTER
  VAR MODE <211> ENTER
  <31> ENTER 3.8 dBm0 ENTER
  RTN, NUM
  START

No:

- Major fault in program sequence.

Display N o.k.?

Yes:

- [23] —||— [25] R_i = 600, R_e = 600
  0.25 μF
  MB 51 ENTER [A-A]
  GRAPH., SWP/S
  Y top 100 μs ENTER, RTN
  START, LINK

No:

- Fault in evaluation circuit program.

Display O o.k.?

Yes:

- Connect [38] to [39]
  MB 65 ENTER [A-A]
  SWP/S
  START

No:

- Fault in evaluation circuit program

Display P o.k.?

Yes:

No:

- Assembly (12) "Signalling distortion measurement" faulty.

Are 64 kbit opts. installed?

Yes:

- Depending on option, connect 64 kbit generator and 64 kbit receiver*
  GEN.PAR. <112>
  ENTER, RTN

- MB 82 ENTER
  MAN/R, run parameter "CHANNEL"
  START, after approx. 30 s STOP

No:

- Connect [20] to [21]
  GEN.PAR. <111>
  ENTER, RTN

Display Q o.k.?

Yes:

- CLEAR RSLT
  BOTH CH1 ENTER, START
  Press ERROR key 10 times
  within the 10 s measuring time
  STOP

No:

- If <>: Interface faulty. If "NOSYNCH":
  PLL not locking or GEN.PAR. configuration
  incorrect

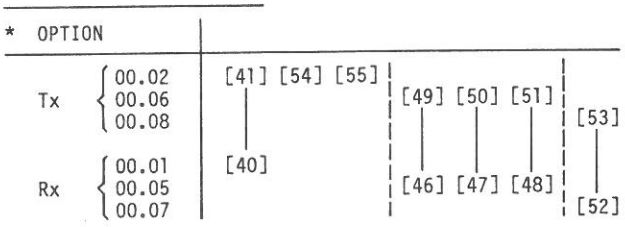
Display R o.k.?

Yes:

No:

- 64 kbit interface faulty
  2 Mbit interface faulty
  PLL not synchronizing

END OF DIGITAL TEST



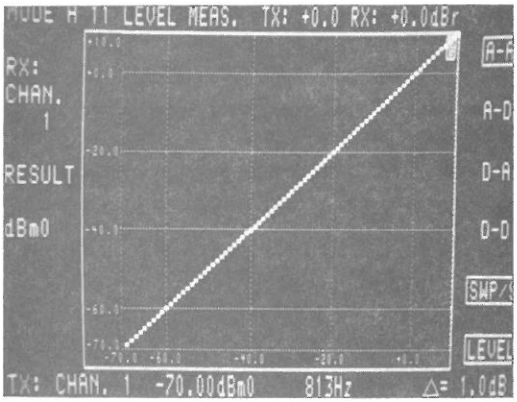


Figure 5.1.1-2 Display A

The measured points must pass through the intersection points of the scaling lines. There must be no visible displacements or offsets.

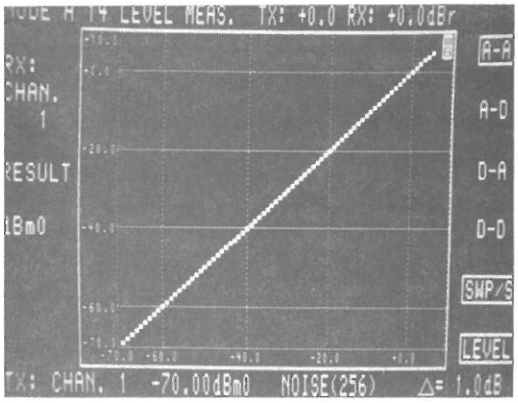


Figure 5.1.1-3 Display B

Same remarks as for display A.

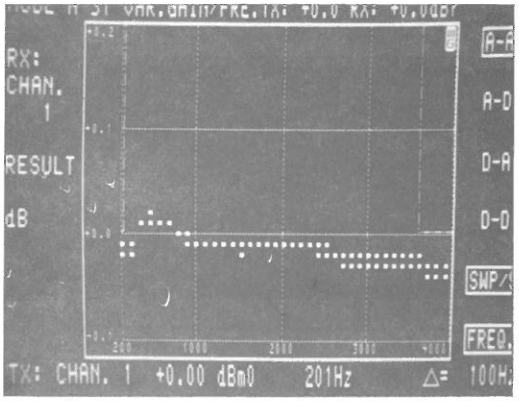


Figure 5.1.1-4 Display C

Display C shows a range of values, from which the measured values may only deviate by $\pm$ 1 mB.

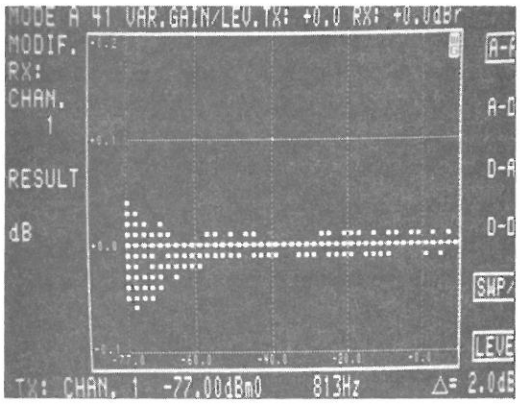


Figure 5.1.1-5 Display D

The measured values should lie within the scatter range defined by an imaginary enveloping curve.

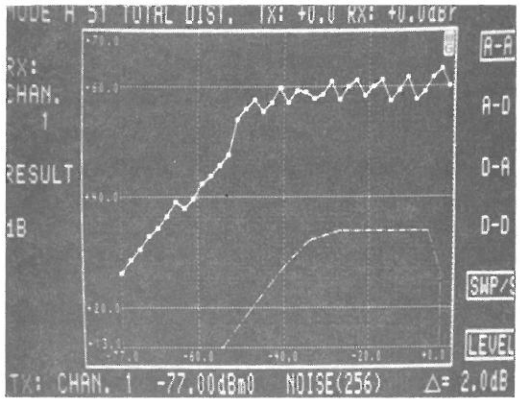


Figure 5.1.1-6 Display E

The inherent distortion ratio should be $\geq$ 54 dB in the level range from 0 to -50 dBm0. Can also be checked by switching to [NUM] ([2]).

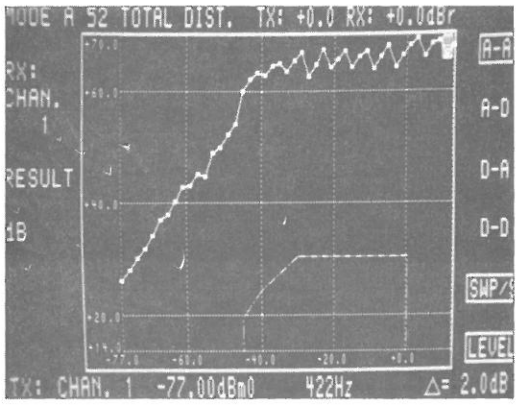


Figure 5.1.1-7 Display F

The inherent distortion ratio should be $\geq$ 60 dB in the level range from 0 to -40 dBm0. Can also be checked by switching to [NUM] ([2]).

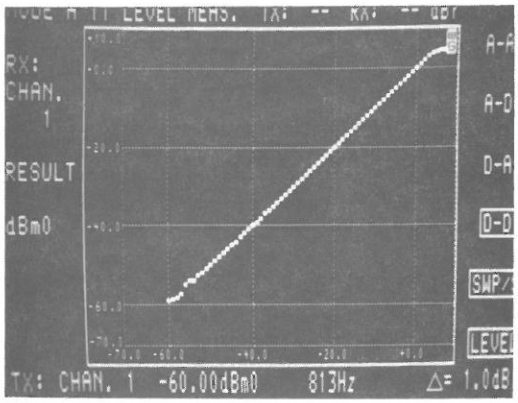


Figure 5.1.1-8 Display G

The "ripple" in the curve at approx. -55 dBm0 is due to the principle used, as is the downward bend in the curve above +3 dBm0.

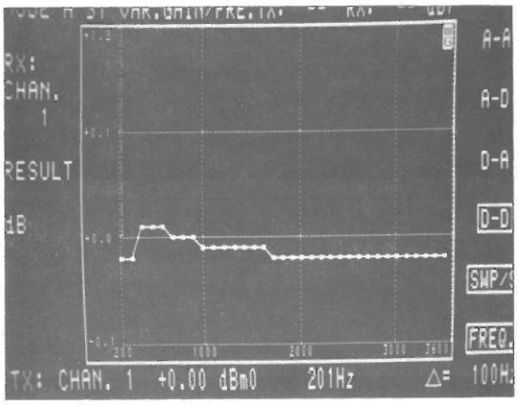


Figure 5.1.1-9 Display H

Since the digital filter operates alone here, no further tolerance values are required. Only rounding errors of ± 1 mB can occur.

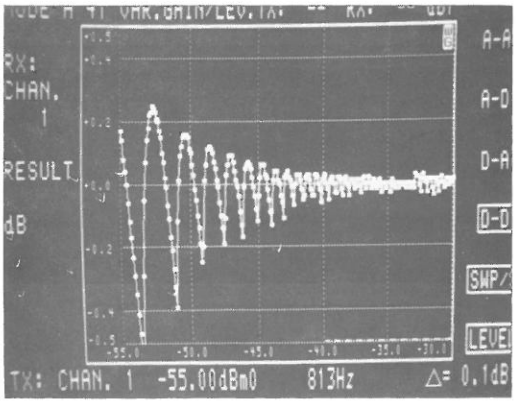


Figure 5.1.1-10 Display I

This curve corresponds to the theoretically calculable values.

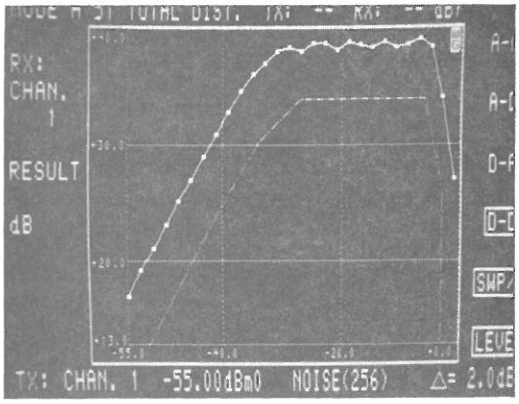


Figure 5.1.1-11 Display K

The marked measured points in this curve correspond to the theoretically calculable S/Q values.

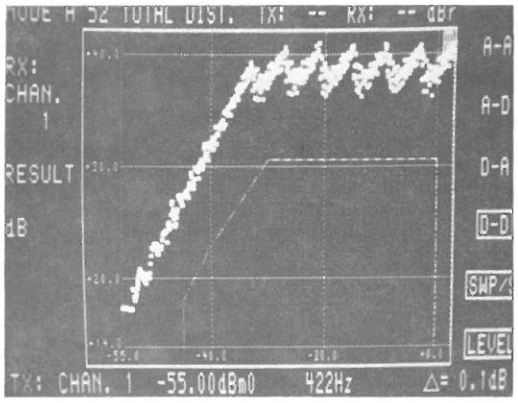


Figure 5.1.1-12 Display L1

Due to the large number of measured points, this curve requires a long measuring time; therefore, display L2 is recommended for a quick overview. (Δ = 0.5 dB)

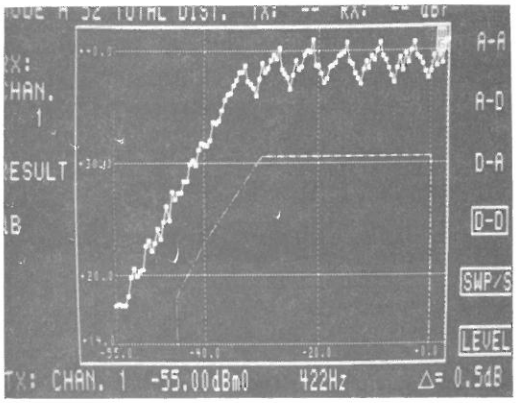


Figure 5.1.1-13 Display L2

The characteristic S/Q garlands are only roughly outlined here, as the horizontal resolution is only 0.5 dB. For better resolution, but with a longer measuring time, refer to display L1.

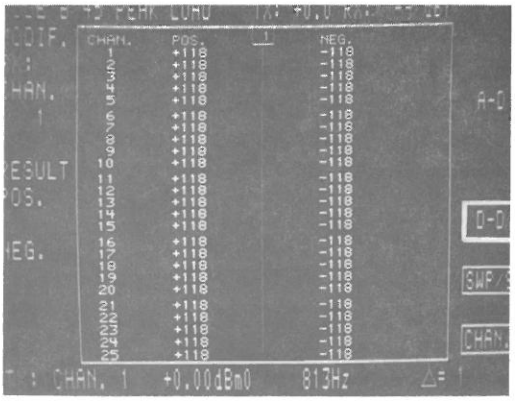


Figure 5.1.1-14 Display M1

An ideal PCM system yields the maximum code values +118 / -118 for a level of 0 dBm0. The "ideal" PCM system is represented by the digital generator.

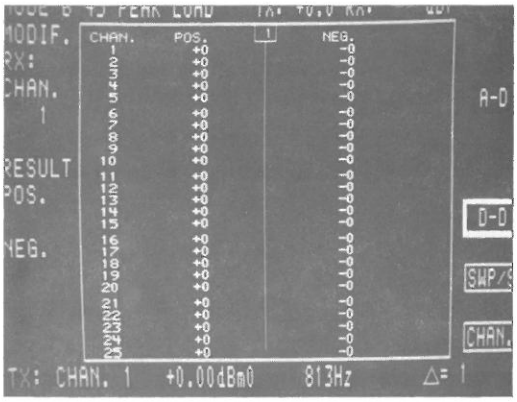


Figure 5.1.1-15 Display M2

The negative and positive maximum code word both drop to the value + 000 here, as set with VAR MODE <251>.

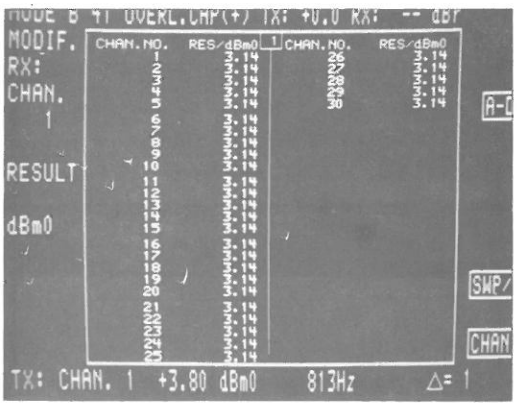


Figure 5.1.1-16 Display N

The operating limit of an ideal PCM system is 3.14 dBm0. Here, the "ideal" PCM system is represented by the digital generator.

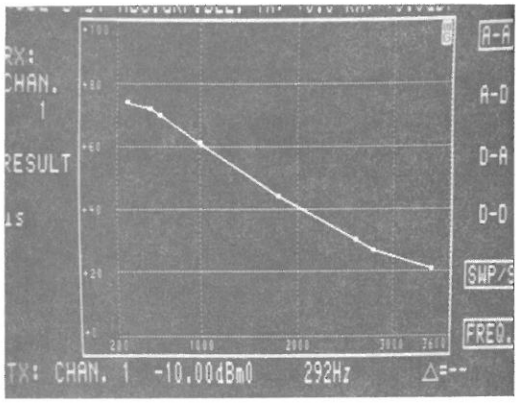


Figure 5.1.1-17 Display O

The capacitor C = 0.25 µF between the a and b conductor should be accurate to within about 1%.

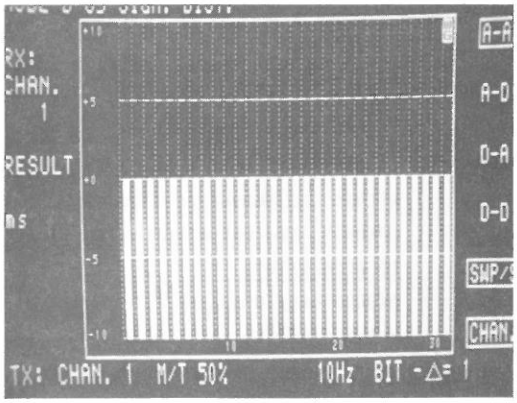


Figure 5.1.1-18 Display P

This simple test does not allow representation of defined signalling distortions other than the value "0". Further information can be obtained by disconnecting [38] ⇵ [39]. In this case, < > must appear.

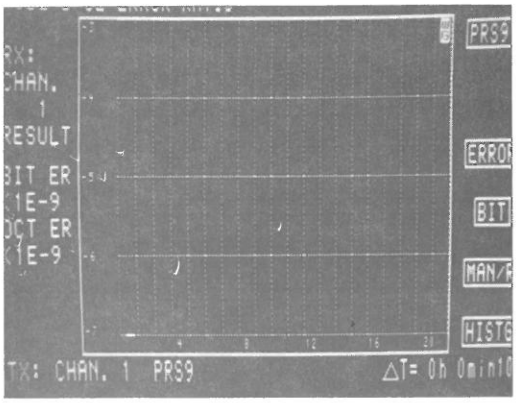


Figure 5.1.1-19a Display Q1

With a measuring time > 30 s, a measurement is made over at least 3 channels with 10 s integration time each. The PLL in the clock circuit must thus re-synchronize several times. If this is not the case, < > or "NOSYNC" appears.

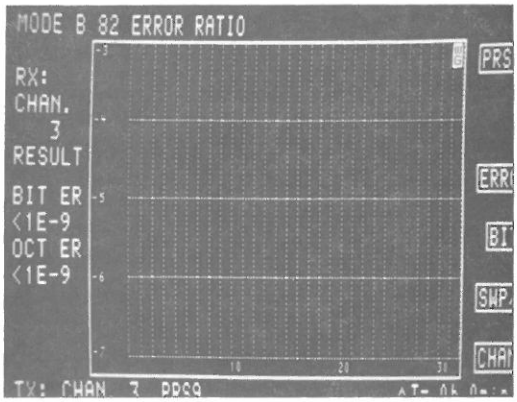


Figure 5.1.1-19b Display Q2

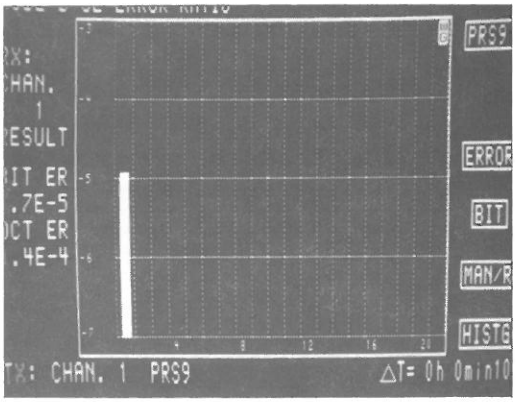


Figure 5.1.1-20a Display R1

The numerical value appearing under RESULT is only relevant in relation to the order of magnitude.
If the ERROR key is pressed 10 x within the measuring time of a channel, the bit error ratio is

$$\frac{10 \text{ errors}/10 \text{ s}}{640000 \text{ bit}/10 \text{ s}} = 1.56 \times 10^{-5}$$

$$\approx 1.6 \times 10^{-5}$$

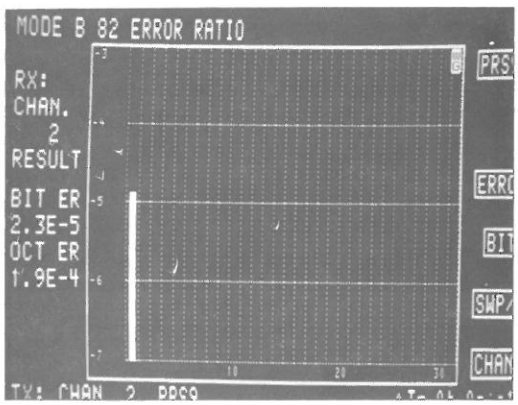


Figure 5.1.1-20b Display R2

5.2 TROUBLESHOOTING IN THE PCM-4 CONTROL SECTION

Note: The following Section refers to block circuit diagram 0 in the "Appendix" at the end of the Service Manual (Fig. 10.6-1).

5.2.1 TESTING THE BASIC FUNCTIONS

The control section is a multiprocessor system with one master computer and two slave computers. The microprocessor interfaces are located on Coupling card 1 and Coupling card 2. The DMA controller and DMA coupler (DMA = Direct Memory Access) are integrated into Coupling card 1, while the interrupt controller is on Coupling card 2. Refer to Sections 9.1.4 and 9.2.6 for a functional description.

Troubleshooting: The PCM-4 self-test after switching on the instrument includes a test of the microprocessor interface. The instrument emits audible signals to indicate faults in the control section. A description of the different horn signals can be found in Section 10.5 (Fig. 10.5-1).

Remarks : Should the self-test be completed without any faults, i.e. if display synthesis and calibration are o.k., it is highly unlikely that there is a fault in the microprocessor interface.

5.2.2 INTERFACE FUNCTION

As shown in the "Control section" block circuit diagram, only the master CPU has access to the internal bus systems of the slave computers, i.e. the master CPU must handle the communication (e.g. data transfer) of the two slave computers. This data transfer is carried out in DMA mode.

Tasks of the master computer in controlling the slave computers:

- The master computer writes control parameters into the measuring circuit memory of the display circuit memory.
- The master computer fetches measurement results from the measuring circuit memory and passes them to the display circuit unit for display.
- The master computer starts display synthesis and measurement via RST 7.5.
- Etc.

The control signals mentioned in Sections 5.2.5.1 and 5.2.5.2 can be checked in order to localize the fault.

Example: To synthesize a "Mode" display, the master CPU passes the display number (written into memory by DMA) to the display circuit and causes the display circuit to synthesize the display with SRTS 7.5.

Signals:		
	MHOLD	Active several time
	MHOLDA	Active several times
	SSOD	Active several times
	MRST 7.5	Active once

5.2.3 DISPLAY MEMORY EXPANSION ON COUPLING CARD 1

If the keyboard is used to enter a command forcing a change in the screen display, the display circuit accesses the memory expansion (CC1). This access presupposes bank-switching.
However, the absence of bank-switching does not necessarily indicate a fault in the bank-switching function (CC1).
The bank-switching control software is in the ROM area of CPU-2A/2. The software for switching back the memory expansion is located in the expansion itself.

5.2.4 CLOCK MODULE

In order to prevent any incorrect clock interrupts during the test, the clock module can be removed without affecting the remaining instrument functions. However, in this case, there will be no automatic instrument calibration 20 minutes after switching on and every 2 hours thereafter. Naturally, it is then also impossible to display the time.
The horn sounds for approx. 5 seconds during the input test, i.e. clock module faulty or missing.

5.2.5 CONTROL SIGNALS OF THE MULTIPROCESSOR SYSTEM

SRST 7.5	Start signal for display synthesis to the display circuit.
MRST 7.5	Start signal for start of measurement to the measuring circuit.
SSOD MSOD	"Finished" message from the display or measuring circuit.
MES END	Interrupt signal from the measuring circuit at the end of the measurement.
TAS INT	Keyboard interrupt.
MHOLD SHOLD	DMA request.

Processor communication is executed via the above signals. These signals are explained in more detail below and a general description is given of the conditions for their activation.

5.2.5.1 Master CPU - Measuring circuit CPU

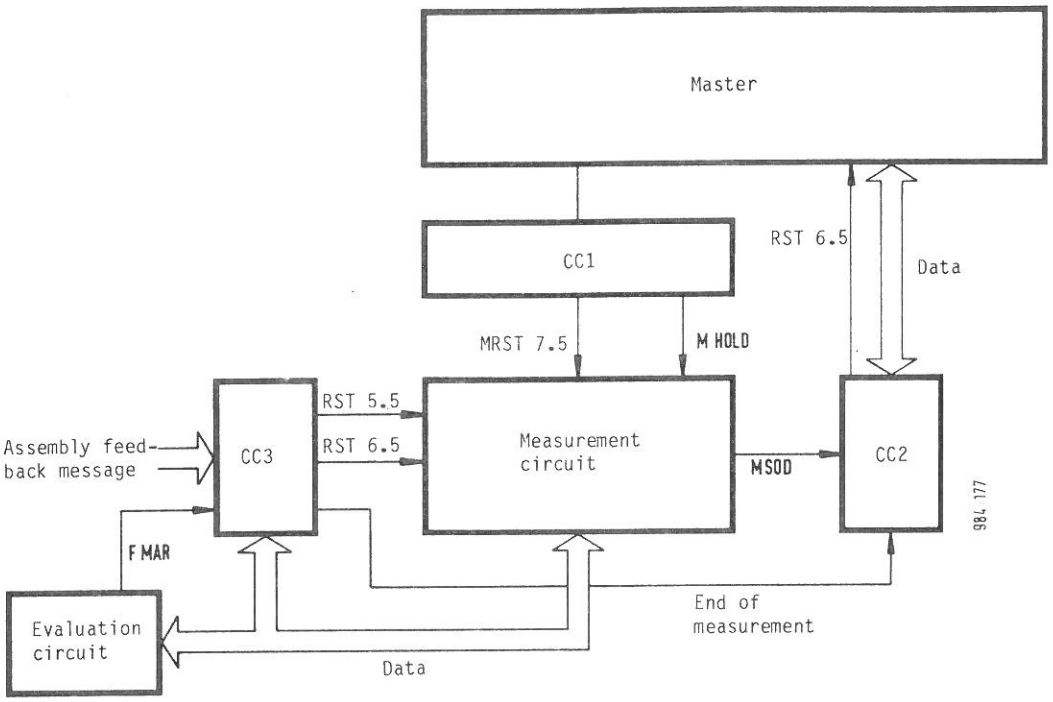
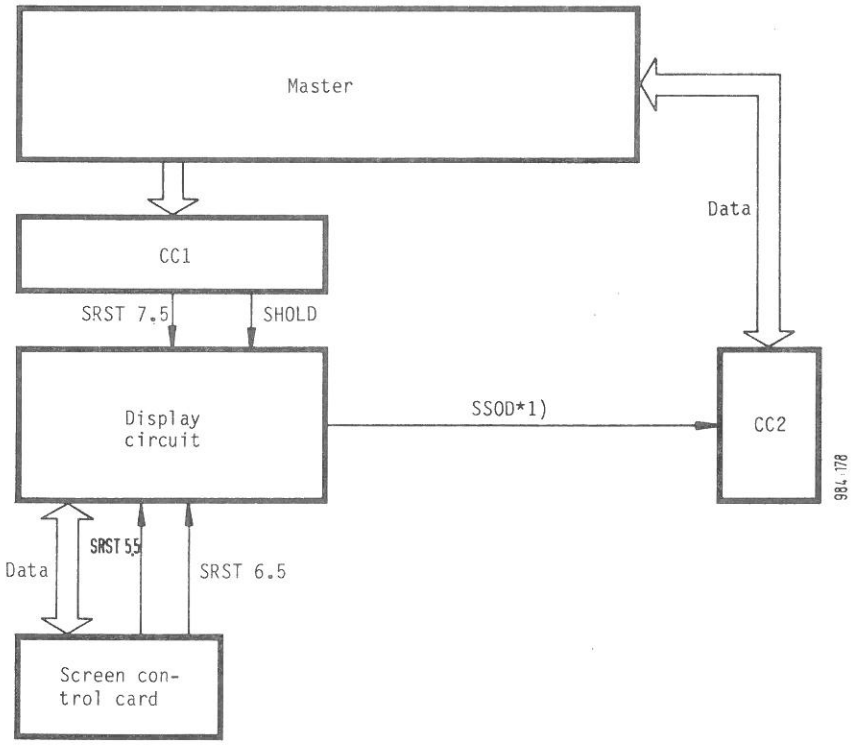


Figure 5.2.5.1-1 Master-to-measuring circuit control signals

- The master starts (or interrupts) a measurement with MRST 7.5.
  (When a measurement is interrupted, the evaluation circuit is also interrupted via OUT 80H (W-80)).
- The measuring circuit sets MSOD = 0 "BUSY" during measurements
  and otherwise MSOD = 1 "READY"
  (READY sets MSOD = 1 and enables RST 7.5. The master interrupt is thus made possible).
  At the end of the measurement, the measuring circuit sets the interrupt FF on CC2 (MES END)
  -> End of measurement, data transmission (RST 6.5).
- The measuring circuit starts the evaluation circuit by writing the mode into register W-80 (after previously writing all the required parameters into W-80 - W-83).
  At the same time, MRST 5.5/MRST 6.5 is enabled (via CC3).
  MRST 6.5: FMAR ("Finished" message of evaluation circuit), M RES INT, INT/ALA, OVERLOAD
  MRST 5.5: WKZ 64 k Int 1, WKZ 64 k Int 2, SIGN SEND, SIGN EMP
- MHOLD: The master requests the address and data bus in order to carry out a DMA.

5.2.5.2 Master CPU - Display circuit CPU



*1) The triggering of RST 5.5 by SSOD on Coupling card 2 is inhibited by the software via IC 7 (CC2). The SSOD line is polled cyclically, like MSOD.

Figure 5.2.5.2-1 Master-to-display circuit control signals

- The display circuit sets SSOD = 0 "BUSY" during display synthesis
  and otherwise SSOD = 1 "READY"
- The master starts display synthesis with RST 7.5
- SRST 6.5 sends Screen control card, blanking gap
- SRST 5.5 [Flashing cursor] - not used.
- SHOLD Master requests address and data bus in order to carry out a DMA.

5.3 TROUBLESHOOTING IN THE ANALOG SECTION

5.3.1 SWITCHING FIELD - PRINCIPAL SIGNAL PATHS

The following schematic diagram of the switching field shows the different signal paths (relay contact positions) set as a function of the mode.
The Tables provide the bit combinations and the associated addresses.

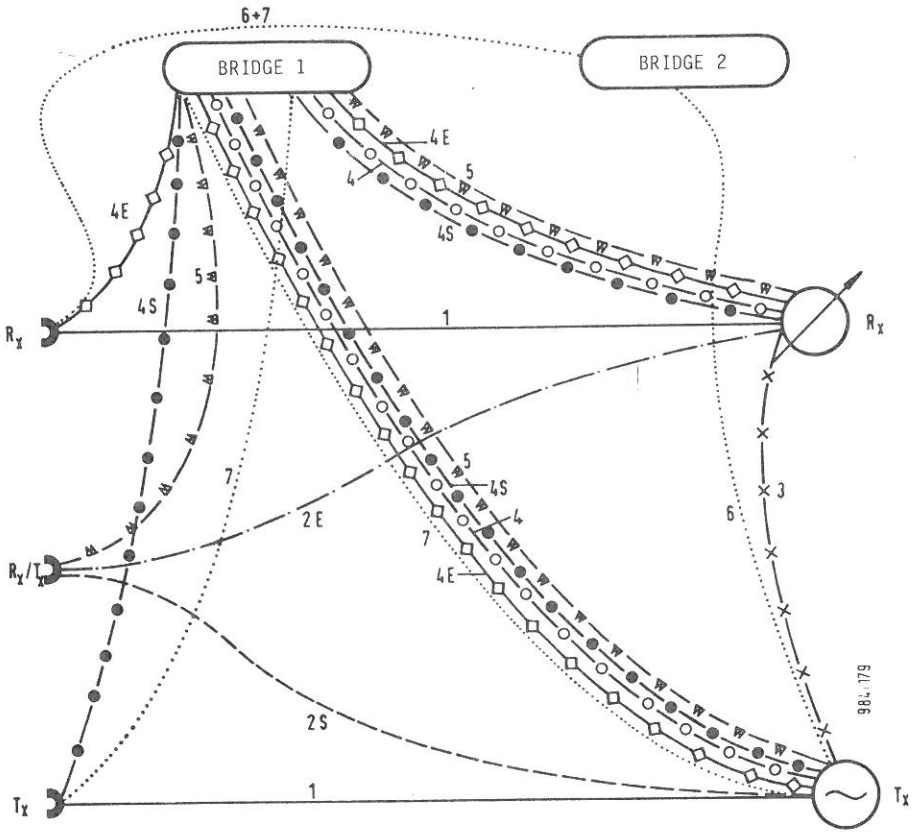


Figure 5.3.1-1 Schematic diagram of the switching field in the receiver section

The connecting lines symbolize a connection between the corresponding circuitry sections. The numbers 1 ... 7 identify the different signal path types shown in the following Tables (also see Section 9.2.29).

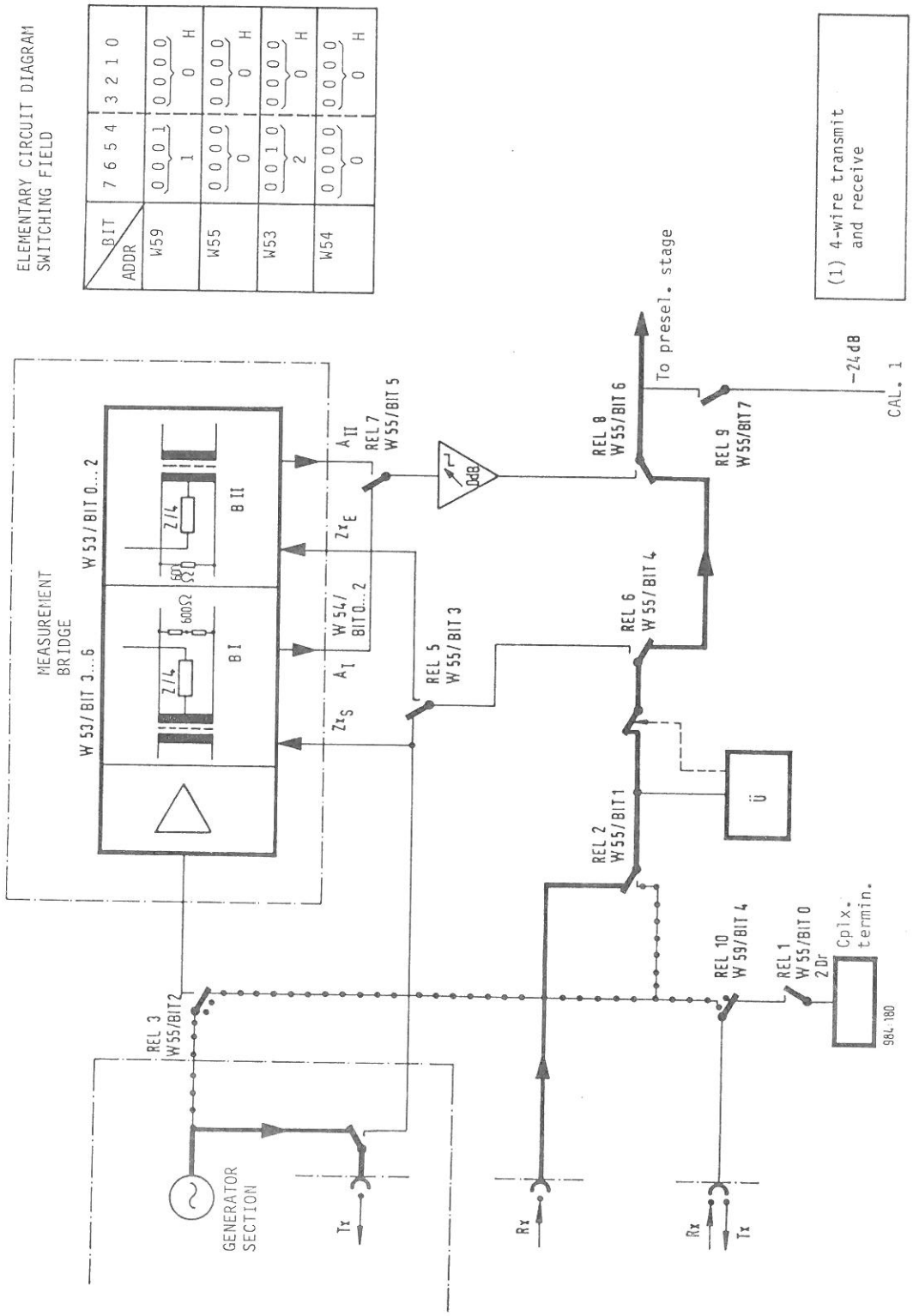
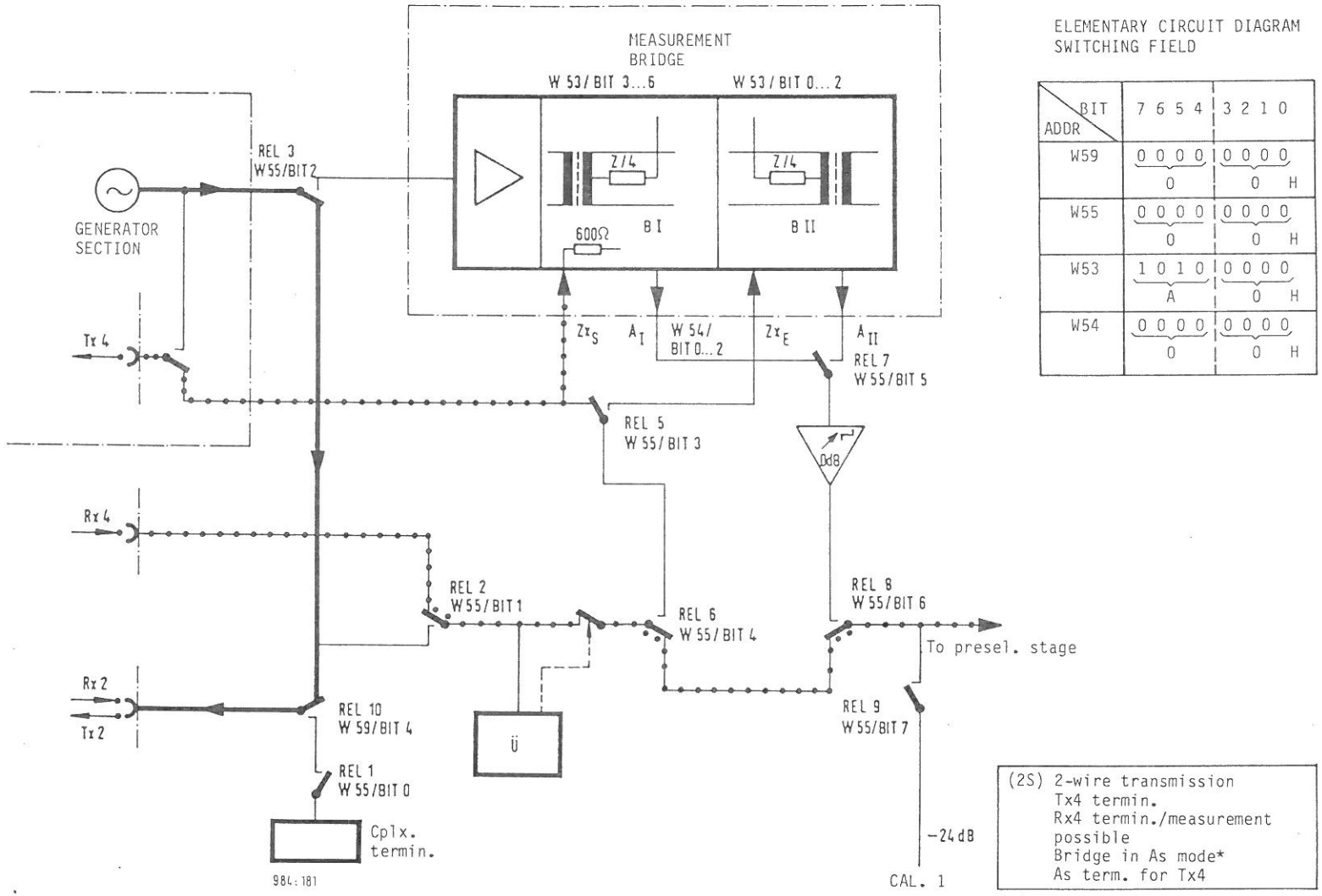


Figure 5.3.1-2 4-wire transmission and reception



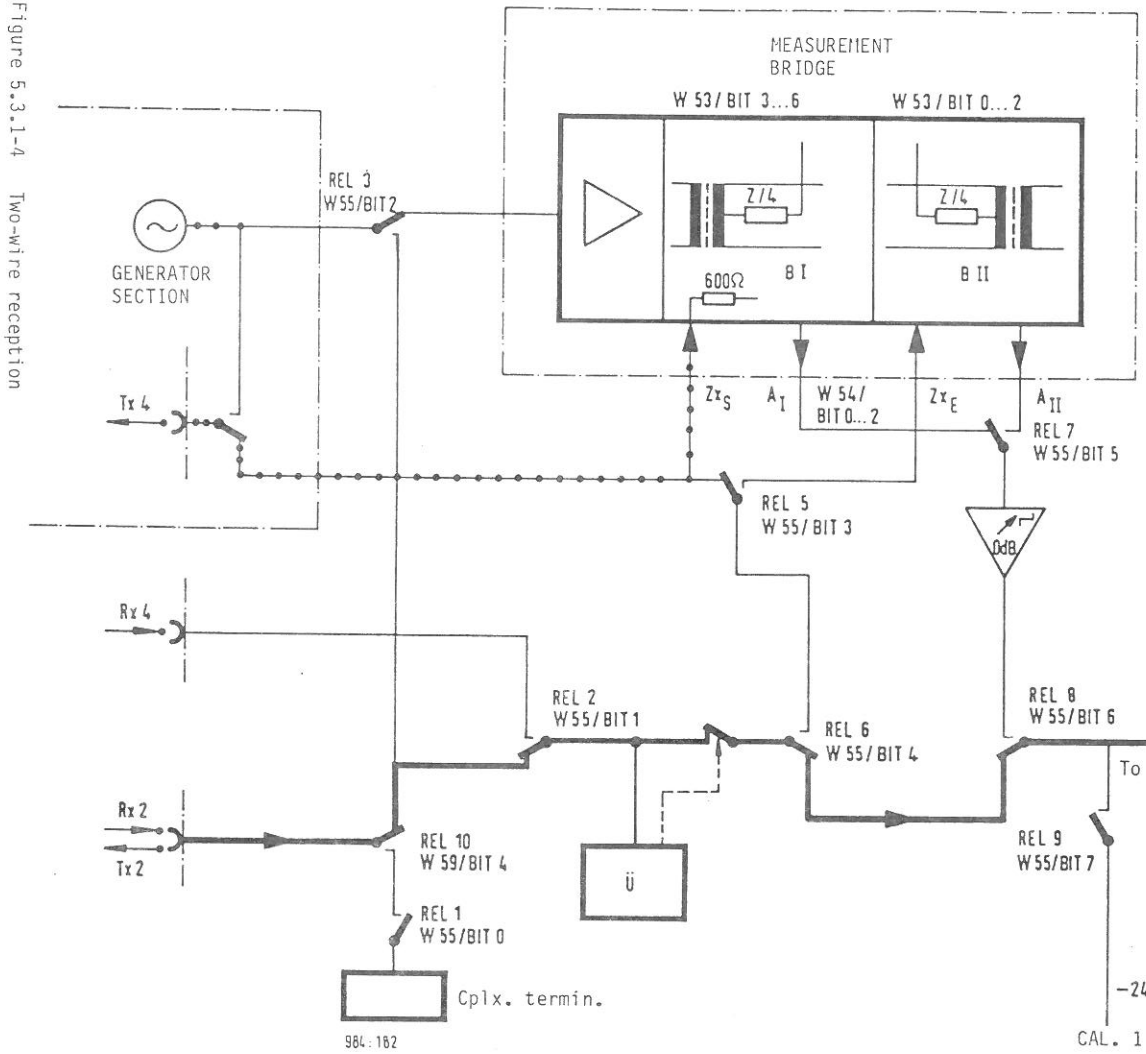
ELEMENTARY CIRCUIT DIAGRAM
SWITCHING FIELD

BIT / ADDR	7 6 5 4	3 2 1 0
W59	0 0 0 0 (0)	0 0 0 0 (0 H)
W55	0 0 0 0 (0)	0 0 0 0 (0 H)
W53	1 0 1 0 (A)	0 0 0 0 (0 H)
W54	0 0 0 0 (0)	0 0 0 0 (0 H)

(2S) 2-wire transmission
Tx4 termin.
Rx4 termin./measurement possible
Bridge in As mode*
As term. for Tx4

* As = return loss measurement

Figure 5.3.1-3 Two-wire transmission



ELEMENTARY CIRCUIT DIAGRAM
SWITCHING FIELD

BIT / ADDR	7 6 5 4	3 2 1 0
W59	0 0 0 0	0 0 0 0
	0	0 H
W55	0 0 0 0	0 1 1 0
	0	6 H
W53	1 0 1 0	0 0 0 0
	A	0 H
W54	0 0 0 0	0 0 0 0
	0	0 H

(2E) 2-wire receive
generator section int. term.
Bu Tx4 term.
Bu Rx4 open
Switch off send level
in generator section
Bridge in As mode

Figure 5.3.1-4 Two-wire reception

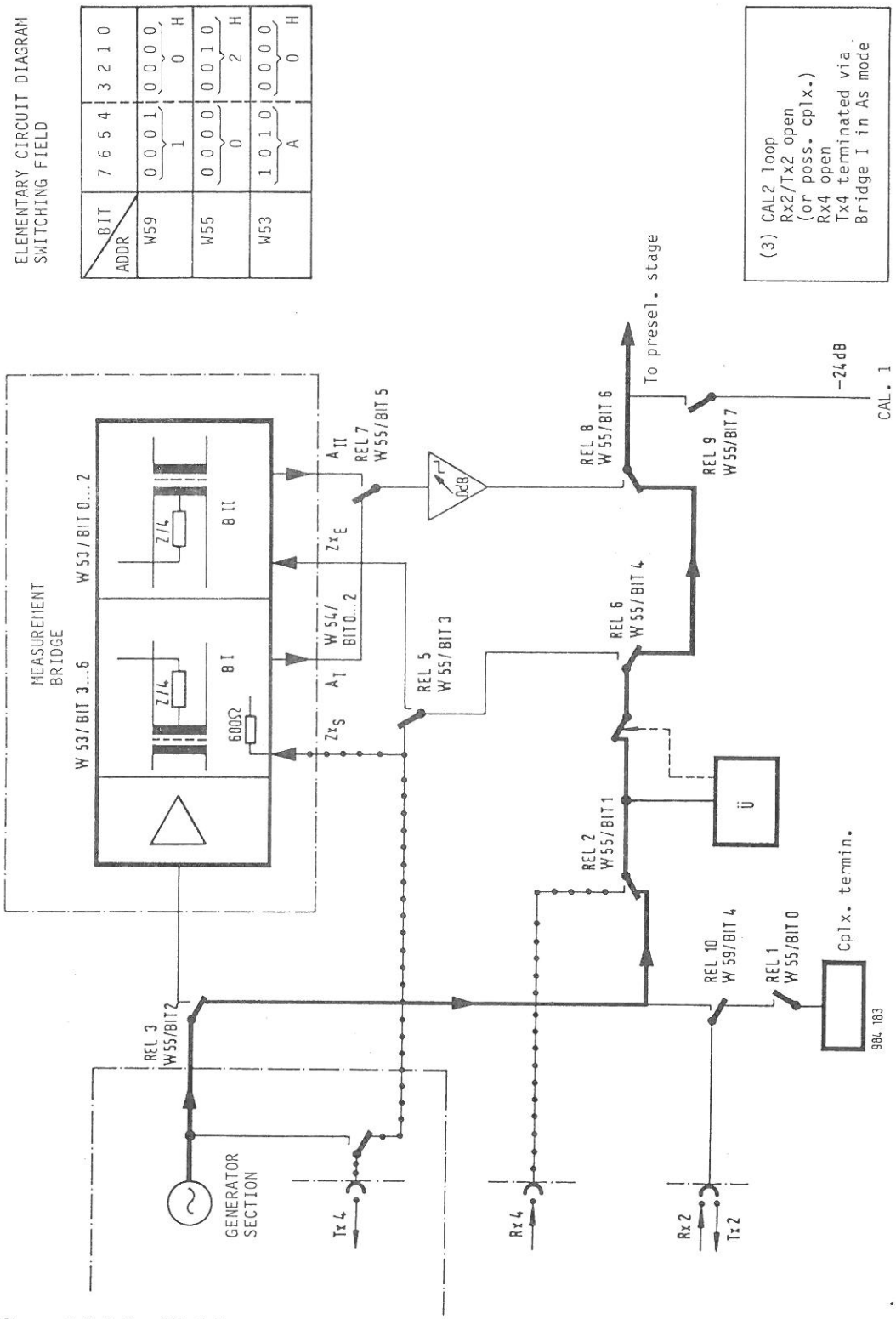


Figure 5.3.1-5 CAL 2 loop

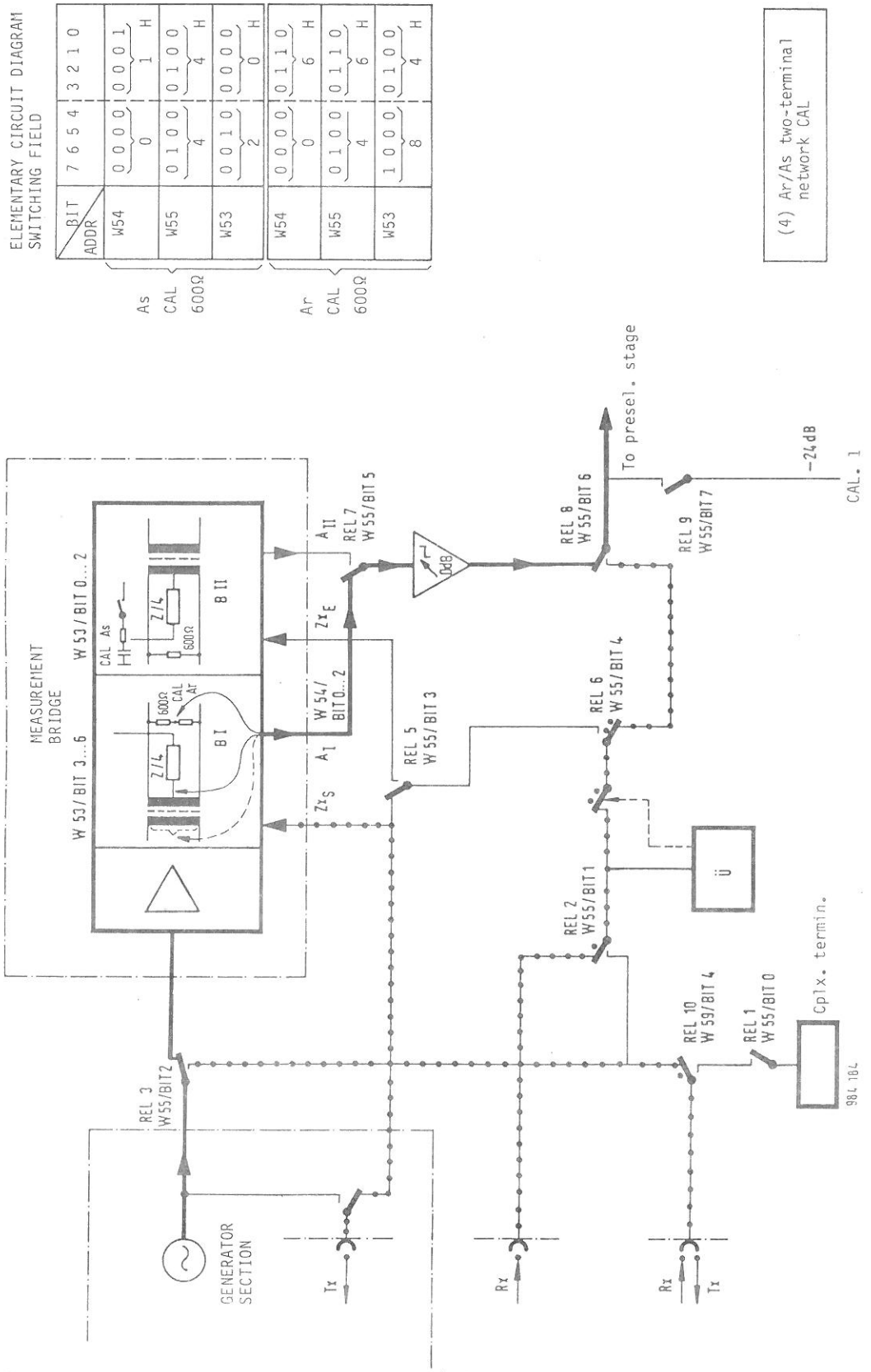


Figure 5.3.1-6 Ar/As two-terminal network CAL (Ar/As = signal path for return loss measurement)

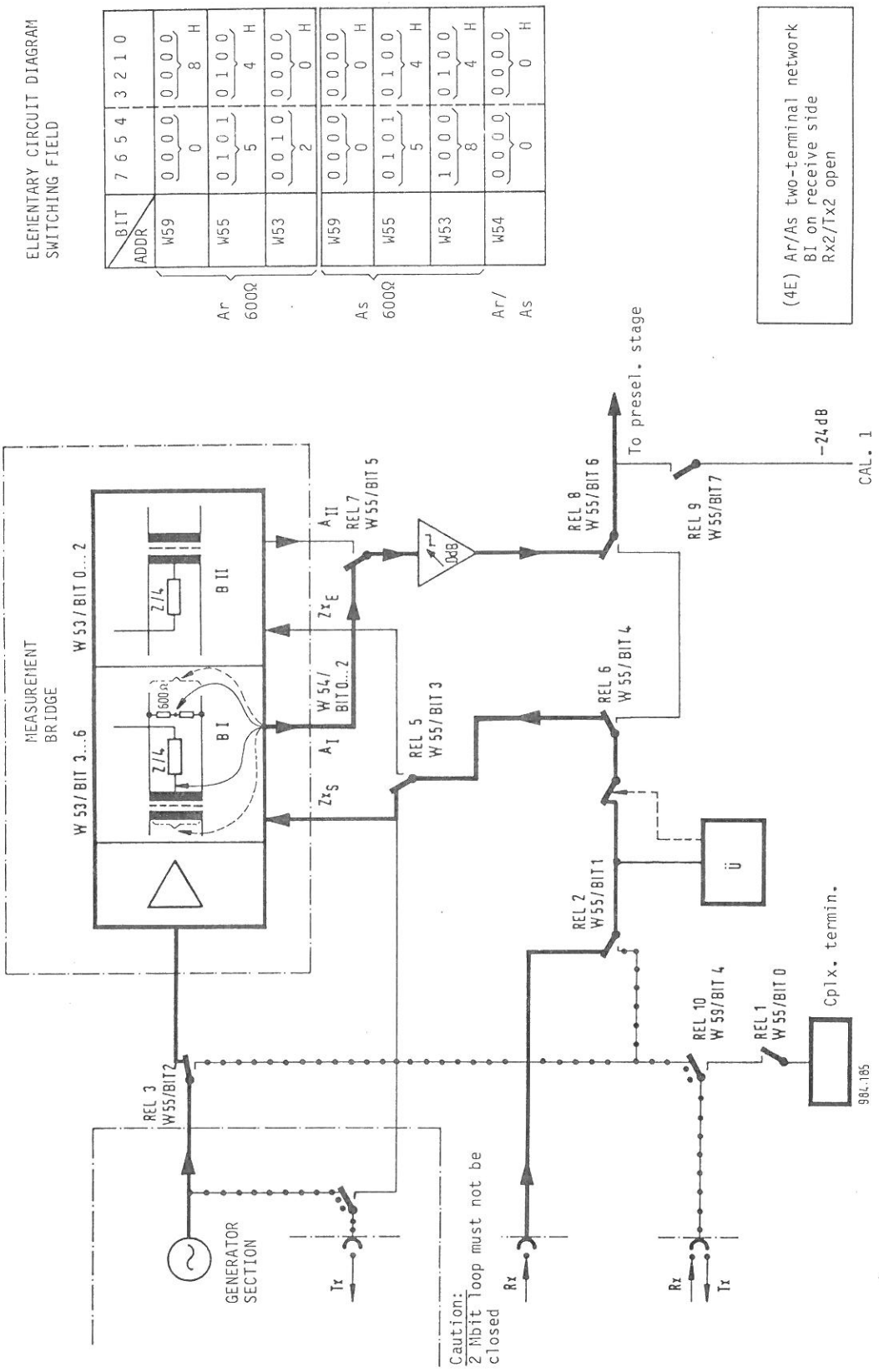


Figure 5.3.1-7 Ar/As two-terminal network BI on receiver side

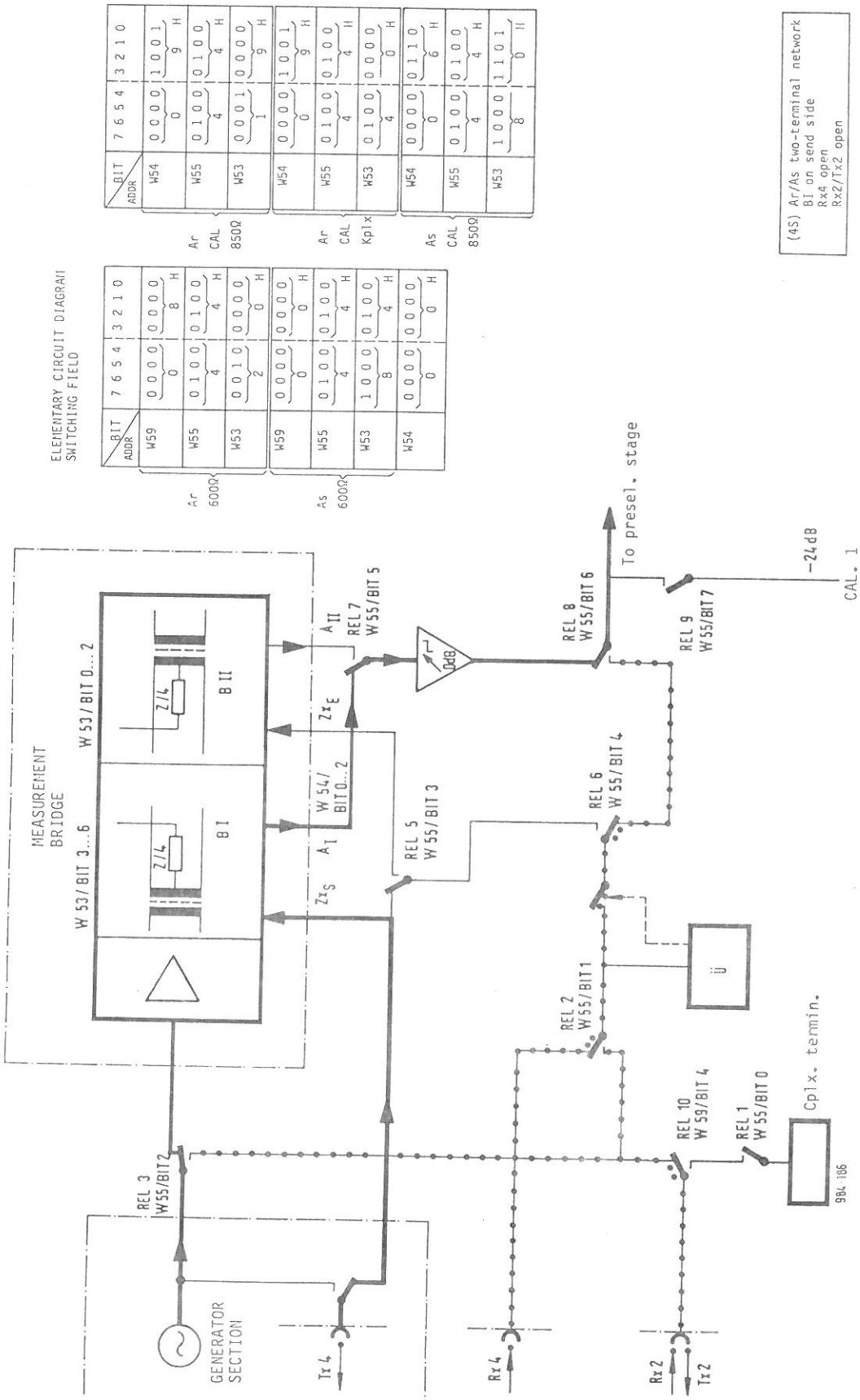


Figure 5.3.1-8 Ar/As two-terminal network BI on generator side

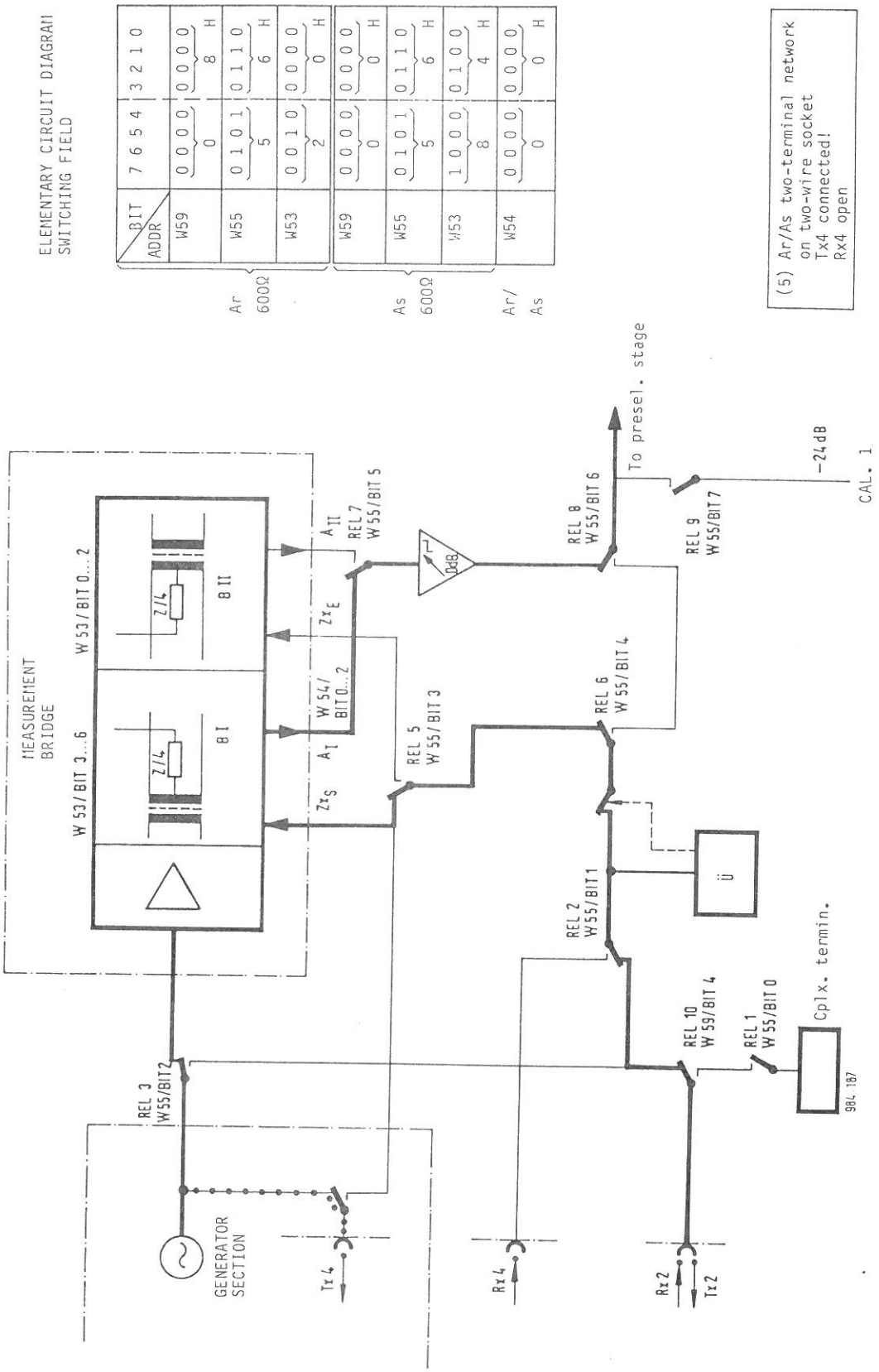


Figure 5.3.1-9 Ar/As two-terminal network on two-wire socket

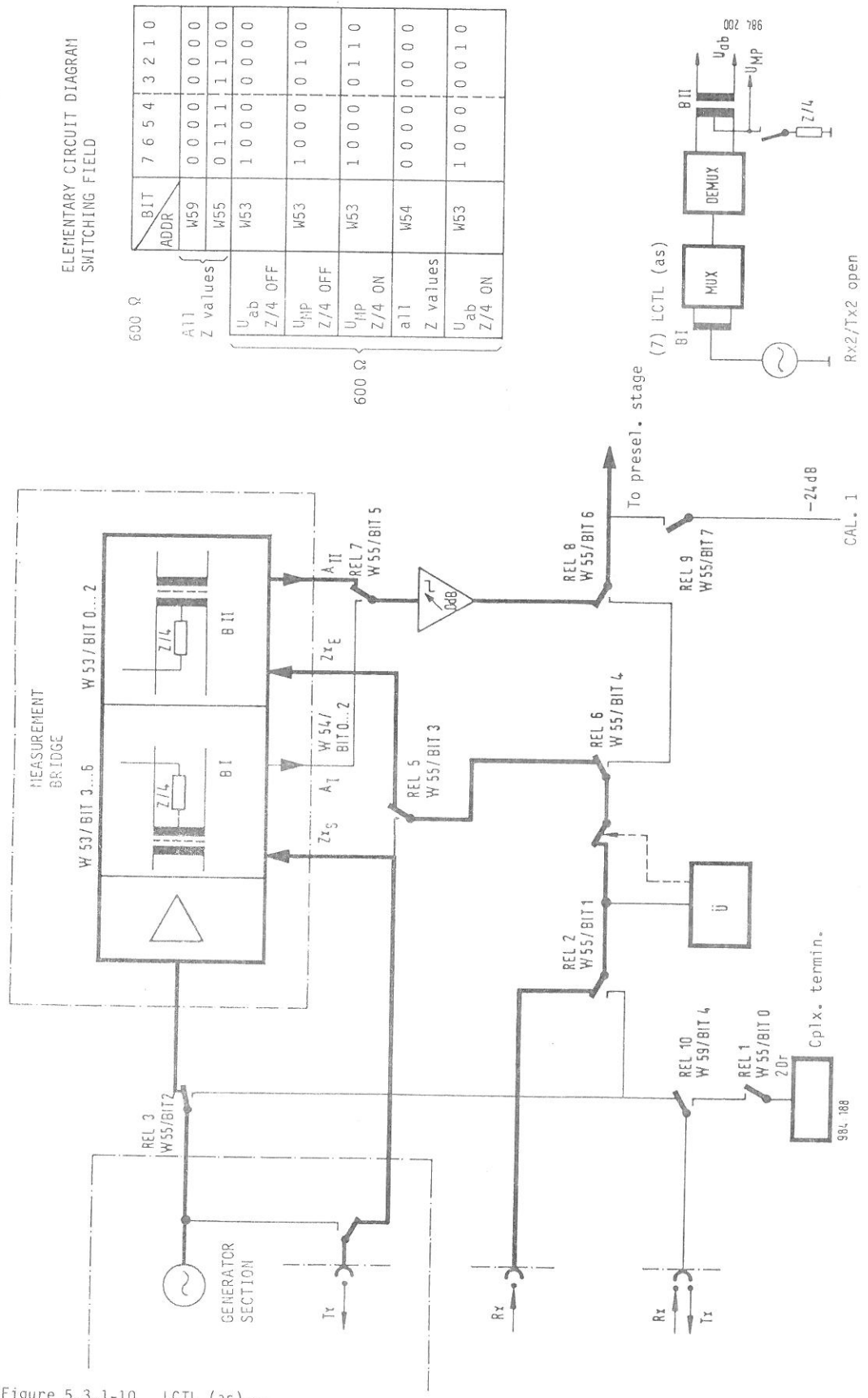


Figure 5.3.1-10 LCTL $(as)_{BII}$

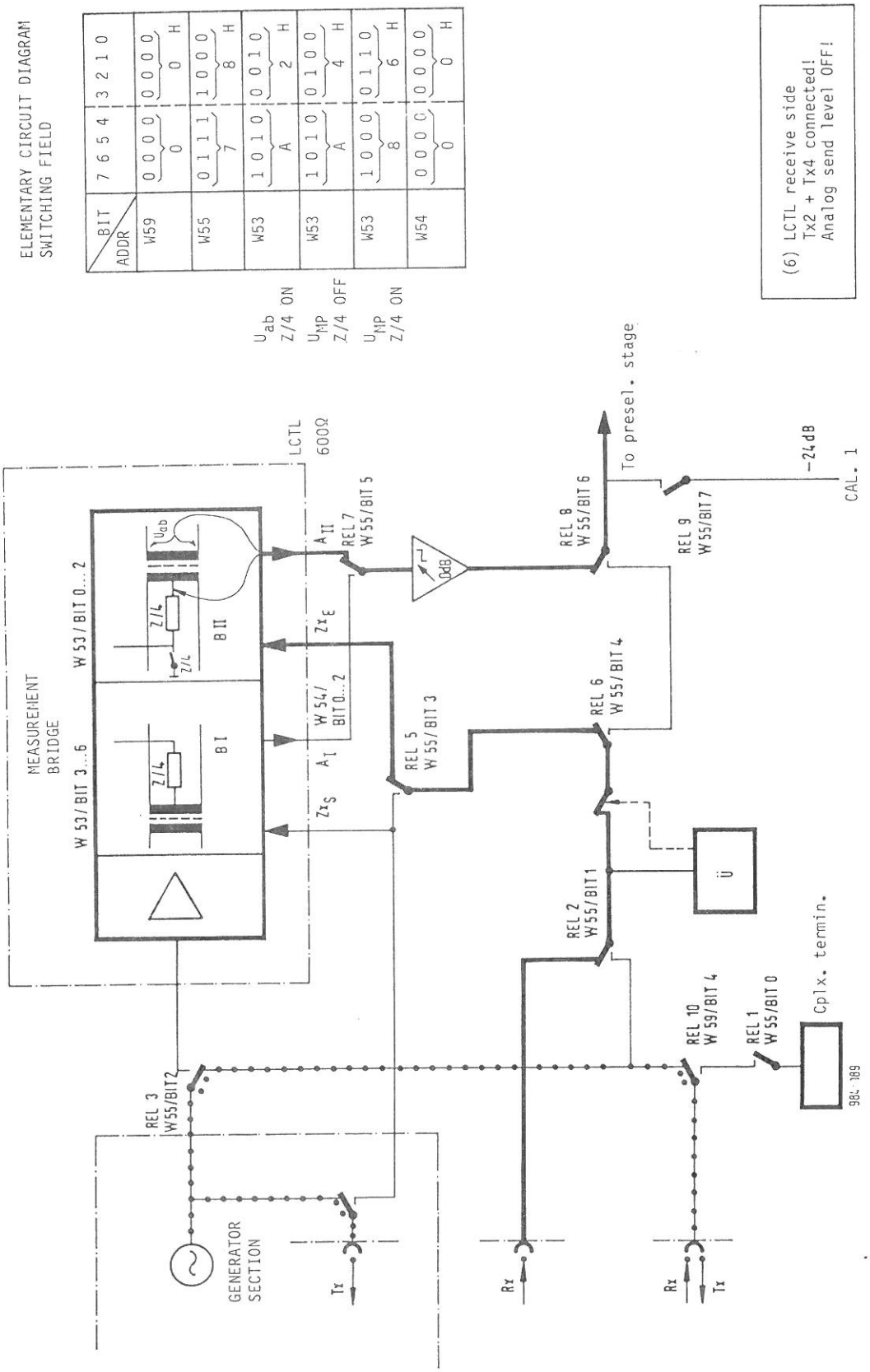


Figure 5.3.1-11 LCTL, receiver side

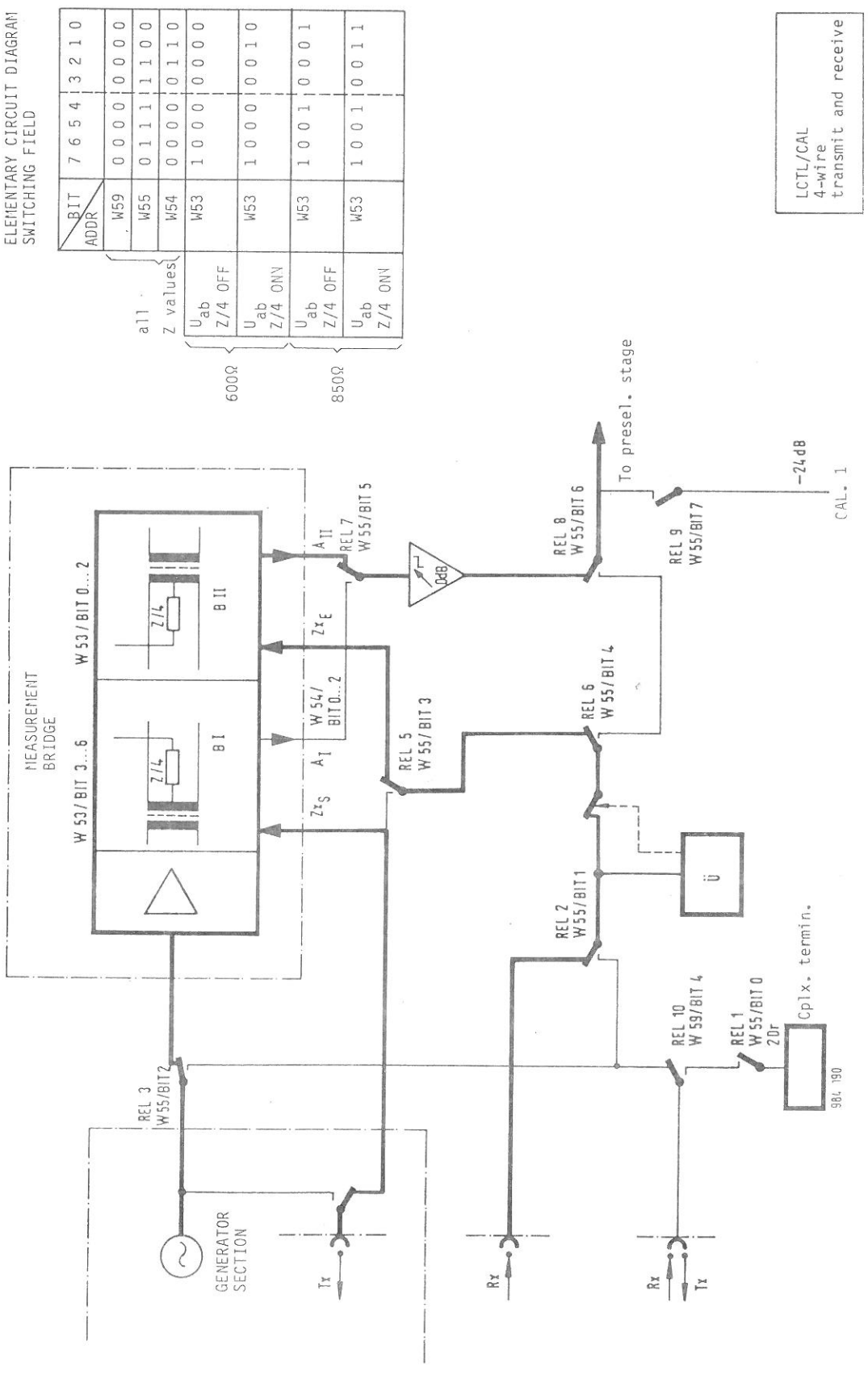


Figure 5.3.1-12 LCTL/KAL, 4-wire transmission and reception

6 TROUBLESHOOTING: LOCALIZATION TO FAULTY COMPONENT

6.1 TROUBLESHOOTING IN THE CONTROL SECTION

Cyclic self-tests

These tests are used for fault localization at the assembly level. Above all, they are designed for closer localization of RAM and ROM faults on CPUs. Such faults are usually detected roughly by the automatic self-test described in Section 4.2 and Fig. 10.5-1. This is achieved by indicating which tests are successful. If a fault occurs, the self-test stops. The faulty test is no longer displayed. The cyclic self-tests described below provide a strategy for further troubleshooting.

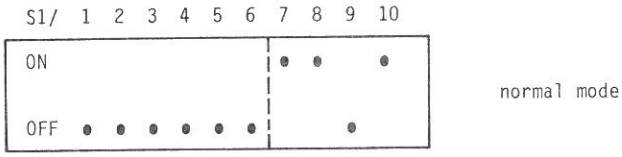
Preparation:

Switch on the instrument while holding the "0" key down. The monitor is switched on in this way and can then be used as described in Section 4.2, provided that a certain "minimum function" is still possible, i.e. if the RAM and/or ROM areas of the CPUs are at least still partially functional.

6.1.1 TROUBLESHOOTING THE CPU-2A BN 2036, CIRCUIT DIAGRAM (90)

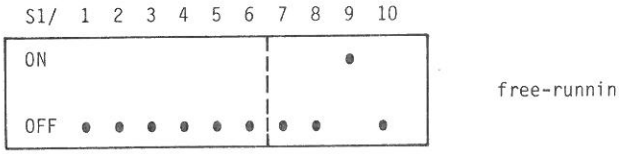
Service switches

The CPU-2A/BN 2036, contains a 10-pole DIL switch. Switches S 1/7 to 1/10 are required for the free-run function of the microprocessor, while switches S 1/1 to 1/6 are the actual service switches.



normal mode

service switch free-running switch



free-running mode

Note: The basic setting of switches S 1/1 to 1/6 may differ from that shown above, depending on the software used.

Figure 6.1-1 Settings of the service and free-run switch S 1

The free-run switch is only required for signature analysis on the CPU.

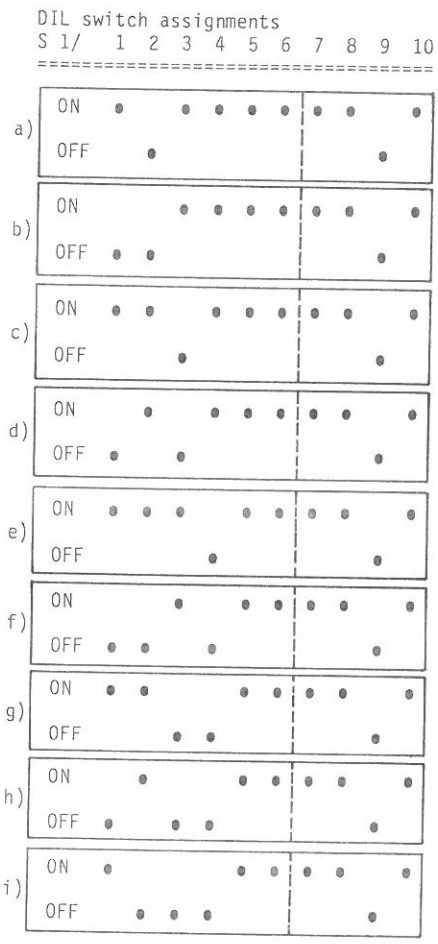
NOTE: The arithmetic processor must be disconnected for free-running mode.

Service programs, such as continuous tests, single tests and stimulus programs, can be called up with the aid of the service switch. The code set causes the processor to establish the program start address in a table during initialization (after mains power-up via the data save input or the CLEAR input). The selected test or stimulus program is then executed once or cyclically. The service switch can be used to represent a 6-bit word, this allowing 64 different combinations.

6.1.1.1 Troubleshooting with the aid of the self-test

(called up via DIL switch S 1)

Cyclic tests on the CPU-2



Test

- a) cyclic ROM test
- b) cyclic RAM test
- c) cyclic I/O test
- d) cyclic AMD test
- e) cyclic RAM test destructive
- f) Switch on bank 1 (switching only, no signalling on SOD line)
- g) Switch on bank 2 (switching only, no signalling on SOD line)
- h) Switch on bank 3 (switching only, no signalling on SOD line)
- i) Switch on bank 4 (switching only, no signalling on SOD line)

(Switching only detectable at corresponding output of 90 IC 52)

Figure 6.1-2 DIL switch assignments

Test result: With oscilloscope at TP 2 (SO... Frequency = Ø -> Faulty
Frequency ≠ Ø -> OK

Description of test programs

a) Cyclic ROM test

In the EPROM test, a 16-bit linear sum is formed across the memory contents and compared with the associated checksums previously determined by the checksum program and stored in the description list, starting at address 8ØH. If the checksums are not identical, a fault has occurred.

Memory content	Addition sequence		
D end	2	End address	(End)
D end-1	4	End address - 1	(End-1)
D sta+2	5	Start address + 2	(Start+2)
D sta+1	3	Start address + 1	(Start+1)
D sta	1	Start address	(Start)

Figure 6.1-3 ROM test procedure - Addition of memory contents

S = (D sta) + (D end) + (D sta+1) + (D end-1) + (D sta+2) .....
EPROM test algorithm

The memory contents are added upwards from the start address of the EPROM and downwards from the end address of the EPROM.
This type of address change tests the address decoder adequately, since the address bit changes approximately simulate the real program sequence.

b) Cyclic RAM test

A non-destructive test of the RAM contents is performed on the instrument. The operating data, such as level and frequency settings, is retained.

This RAM test consists of two parts:

- Cell test for examining the individual memory cells
- Address test for examining the addressing of these memory cells

In the cell test, various bit patterns are written and read in order to establish whether interlinks exist between the individual bits and/or cells. All bit interlinks are detected, even without a knowledge of the internal RAM topology.

NOTE: A far more stringent test of address decoding can be performed using the "destructive" RAM test programs (see Item f)).

c) Cyclic test of the slow I/O bus

The I/O bus test checks the data lines of the slow I/O bus and detects short-circuits on the data lines (and on the device bus!).

The test function of the I/O bus is activated at the start of this program. This prevents further components connected to the I/O bus from writing data onto the I/O bus. The test consists of writing various data words onto the bus, reading them back in (IC 43) and comparing the written and read words. The write driver (IC 42) remains active during reading.

Path: Writing out -> IC 42 (I/O data latch)
Reading in via IC 44 (45) and IC 43

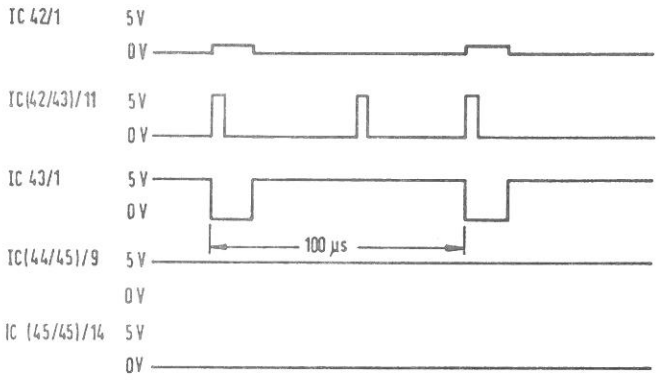


Figure 6.1-4 I/O module activation

d) Cyclic test of the arithmetic module Am 9511

The test of the arithmetic module Am 9511 is called up if the arithmetic module is fitted on the CPU card. The test performs a simple calculation. The test is based on the assumption that either all calculations will be performed correctly, or none at all.
In this test program, all interrupts are disabled during program execution, since an even number of bytes must always be read out of the module in order not to produce an unacceptable change in the internal pointer of the module.

e) Cyclic RAM test "destructive"

This RAM test uses three algorithms and is thus a far more stringent address test than the non-destructive RAM test. The test includes the following:

- Forward address interlinks
- Backward address interlinks
- Decoder
- Stuck address lines
- Chip select logic
- State-changing behaviour of the bit cells.

The scope of the individual test algorithms varies in relation to the different fault mechanisms. They also overlap in part.
For example, the switching of each bit cell to "zero" and "one" is tested by three algorithms, but with different degrees of severity.
The complete performance of the non-destructive RAM test and the three test algorithms of the "destructive" RAM test provide all the testing necessary.
The "destructive" RAM test can be used for troubleshooting and repair purposes, since the operating data do not have to be retained.

f) Bank switching

(Applies for fixed points f to i)

After selecting the corresponding "bank" and starting the instrument, the corresponding output of 90 IC 52 must switch to "HIGH".

k) Free-running

Switch S 1 can be used to disconnect data lines AD0, AD6 and AD7 of the processor from the data bus. Thus, not all data bits output from the EPROM are passed to the processor.
During each read operation, the command code of a command triggering no activity is passed to the processor.
A more detailed explanation can be found in the next section "troubleshooting with the aid of signature analysis".

6.1.1.2 Troubleshooting with the aid of signature analysis

The principle of signature analysis is described in Section 2.3 of this Service Manual. The CPU board has a free-running switch (S 1/7 to S 1/10) for this purpose. If the settings of S 1/7 to S 1/10 are inverted, the processor addresses the entire memory area by incrementing the address by 1 each time and performing this operation cyclically after a RESET. In order to record ROM signatures, the associated ROM select (test point) must be used as the START/STOP signal. The use of the free-running switch, in conjunction with the pull-up resistors of the data bus and the RD2 signal via G1 2 to AD6, ensures that only a subset of the 8085 command set is executed.

Bit number :	7	6	5	4	3	2	1	0	
Logic level :	H	L	X	X	X	X	X	H	
Machine code:	1	0	X	X	X	X	X	1	= 81H..BFH

X = any, data line not disconnected.

Note: The free-running switch only affects data lines 0, 6 and 7.

Figure 6.1-5 Value of the data bits for free-running

The commands involved are one-byte commands for arithmetic or logic operations which increment the program counter reading by one and thus yield a "program" with consecutive memory addressing.

If the most-significant bit A15 is used as the START/STOP frame, and if the processor increments the entire address range (from 0000H to FFFFH), each address line yields an unambiguous signature.

The free-running operation tests the heart of the microcomputer, namely

- a number of functions of the microprocessor and the circuits required for its operation, such as the clock generator circuitry,
- the address bus with drivers and decoders,
- the EPROM contents (including data bus), if the START/STOP frame is selected accordingly.

The I/O area and the RAMs cannot be tested in free-running mode.
The WORIS functions of the monitor program offer further testing capabilities.

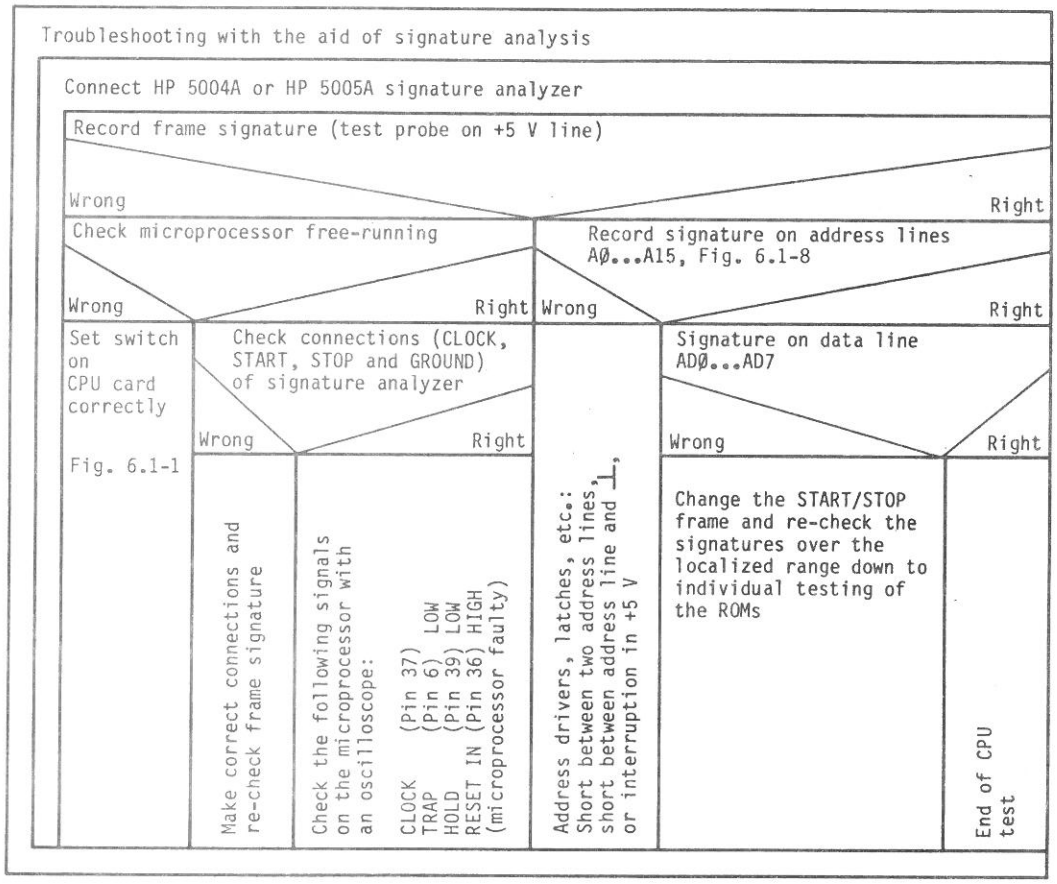


Figure 6.1-6 Structural diagram of troubleshooting

Troubleshooting in the event of a ROM fault

Troubleshooting is performed with the aid of the Hewlett-Packard signature analyzer 5004A or 5006A*. Switches S 1/1 to S 1/10 on the CPU board must be set appropriately to activate the free-running mode (refer to CPU circuitry description for details). With the instrument switched off, set switch S 1 as shown in Fig. 6.1-1.

Measuring the data signatures:

Connect the signature analyzer:
Clock (⎍) at $\overline{RD}$: TP OE, GND to -pole C5

The signatures are checked at the outputs of the ROMs on the CPU board.

EPROM TP	IC	B.V.	START Connection	START Edge	STOP Connection	STOP Edge
ROMØØ	PL3	--	TP ROM ØØ	⎍	TP ROM ØØ	⎍

Figure 6.1-7 Edge assignment of the START/STOP frame

Checking the frame:

The signature 0000 must be obtained at Pin 20 (CE) of the EPROM in question, since this signal is always LOW during the selected frame. The frame signature must appear at Pin 20 of all other EPROMs, since these are not addressed and Pin 20 is thus constantly HIGH. The frame signature corresponds to the signature on the +5 V line.
Since minor software modifications, even if they only affect 1 bit, result in a different signature on the data lines, make sure that the correct signature list is consulted.
The signature list is attached to the instrument. The exact location of the list is described in Section 3 under the heading "Instrument data".
If none of the 8 signatures is correct, there is most probably a fault on the address side, in which case the signatures of the address lines must be checked.

* Instruments from other manufacturers will not always produce the same signatures.

Address signatures

The address line signatures must be identical at all points. The signature on the CPU board, upstream and downstream of the address drivers and the address latches must be identical.
If the signatures on ADØ...AD7 are to be checked, the trailing edge of the ALE signal must be used as the CLOCK. However, ADØ, AD6 and AD7 are only valid directly on the microprocessor in free-running mode. In addition to the signatures of the address lines, the signatures of the chip select signals = decoded addresses and of the enable signals must also be checked.
The Table shown in Fig. 6.1-8 must be used for this purpose.

Test point	Signature
AØ (ADØ)*	UUUU
A1 (AD1)	5555
A2 (AD2)	CCCC
A3 (AD3)	7F7F
A4 (AD4)	5H21
A5 (AD5)	OAFA
A6 (AD6)*	UPFH
A7 (AD7)*	52F8
A8	HC89
A9	2H7O
A1Ø	HPPO
A11	1293
A12	HAP7
A13	3C96
A14	3827
A15	755U
$\overline{V}_{Ø}$	5FU8
$\overline{V}_{1}$	29A6
$\overline{V}_{2}$	64HP
$\overline{V}_{3}$	1181
IC 35 PIN 7 = IC 15 PIN 6	P255

Test point TP	Signature
ROMØ	4POA
ROM1	12U3
ROM2	PCO1
ROM3	F2A6
ROM4	6H49
ROM5	0996
ROM6	U3H5

Test point TP	Signature
ROMØØ	755U
ROMØ1	0001
ROMØ2	0001
ROMØ3	0001
ROMØ4	0001

Test point TP	Signature
RAMØ	PF2P
RAM1	8F14
RAM2	U81U
RAM3**	3UP7
IC 36 PIN 7	7A71

Decoded addresses

Notes:

START: ⌞	TP ROMØ
STOP: ⌞	TP ROMØ
CLOCK: ⌞⌝	TP OE (ALE, connector Pin C12, ⌞)*
GROUND:	TP M
Stimulus:	Free-running
Frame signatures:	0001

Figure 6.1-8 Address signatures (CPU board)

* ADØ, AD6 and AD7 only valid when measured directly on the microprocessor pins.
** Only applicable if the arithmetic processor is installed.

Troubleshooting in the event of a RAM fault

If a RAM fault occurs, address lines AØ to A7 should first be checked using signature analysis. Subsequently check the signatures at the chip enable inputs of the RAMs. Refer to the Section on "Address signatures".

Once this has been done, the data lines can be checked (see Fig. 6.1-9).

Test point	Signature	Remarks
The signature on lines DØ...D7 must be the same as the signatures on lines ADØ...AD7. (As the signature is dependent on the RAM contents, a check can only be made here as to whether the signature is identical over the entire signal path.)		↘ START: TP RAMØ...3 ↗ STOP: TP same as START ↗ CLOCK: TP OE Stimulus: Free-running

Figure 6.1-9 RAM signatures (data lines)

The following is a compilation of the cyclic tests desribed above. They can be called up via DIL switches or the start address in the monitor program.

A) Overview

1. Cyclic tests on master CPU-2A/1

a. Jump to monitor program
b. Cyclic ROM test
c. Cyclic RAM test (non-destructive)
d. Cyclic I/O test
e. Cyclic AMD test
f. Cyclic IEC test
g. Cyclic RAM test (destructive)
h. Cyclic calibration
i. Switch on bank 1
j. Switch on bank 2
k. Switch on bank 3
l. Switch on bank 4

2. Cyclic tests on display circuit CPU-2A/2 (from software Series G ...)

a. Jump to monitor program
b. Cyclic ROM test
c. Cyclic RAM test (non-destructive)
d. Cyclic I/O test
e. Cyclic AMD test
f. Cyclic BSK test
g. Cyclic RAM test (destructive)
h. Switch on bank 1
i. Switch on bank 2
j. Switch on bank 3
k. Switch on bank 4

3. Cyclic tests on measuring circuit CPU-2/3 (with evaluation circuit)

a. Run test, microprocessor
b. Cyclic ROM test
c. Cyclic RAM test (non-destructive)
d. Cyclic I/O test
e. Cyclic AMD test
f. Cyclic RAM test (destructive)
g. Cyclic evaluation circuit test (overall)
h. Cyclic evaluation circuit RAM test (destructive)
i. Cyclic evaluation circuit RAM test (non-destructive)
j. Cyclic evaluation circuit ROM test

B) Assignment to DIL switches

DIL switch setting No. 1234567890	Start address Monitor	MASTER test 2A/1	DISP. CIRC. test 2A/2	MEAS. CIRC. test 2/3
on 11 1 off 000000 0	0H	Normal state	Normal state	Normal state
on 11111111 1 off 0	D7H	Monitor program	Monitor program	Monitor program
on 1111111 1 off 0 0	DDH	Not used	Not used	Run test, meas. circuit (proc.)
on 1 111111 1 off 0 0	E3H	Cyclic ROM test	Cyclic ROM test	Cyclic ROM test
on 111111 1 off 00 0	E9H	Cyclic RAM test	Cyclic RAM test	Cyclic RAM test
on 11 11111 1 off 0 0	EFH	Cyclic I/O test	Cyclic I/O test	Cyclic I/O test
on 1 11111 1 off 0 0 0	F5H	Cyclic AMD test	Cyclic AMD test	Cyclic AMD test
on 1 11111 1 off 00 0	FBH	Not used	Cyclic BSK test	Not used
on 11111 1 off 000 0	101H	Cyclic IEC test	Not used	Not used
on 111 1111 1 off 0 0	107H	Cyclic RAM test (destr.)	Cyclic RAM test (destr.)	Cyclic RAM test (destr.)
on 11 1111 1 off 0 0 0	10DH	Cyclic cali- bration (only via monitor)	Not used	Cyclic overall test of evalua- tion circuit
on 1 1 1111 1 off 0 0 0	113H	Cyclic printer test (cont. test)	Not used	Cyclic I/O test of evalua- tion circuit

Figure 6.1-10 Test overview

DIL switch setting No. 1234567890	Start address Monitor	MASTER test	DISP. CIRC. test	Meas. CIRC. test
on 1 1111 1 off 00 0 0	119H	Switch on bank 1 (switching only, no signalling on SOD line)	Switch on bank 1 (switching only, no signalling on SOD line)	Cyclic RAM test (destr.) eval. circ.
on 11 1111 1 off 00 0	11FH	Switch on bank 2 (switching only, no signalling on SOD line)	Switch on bank 2 (switching only, no signalling on SOD line)	Cyclic RAM test eval. circ.
on 1 1111 1 off 0 00 0	125H	Switch on bank 3 (switching only, no signalling on SOD line)	Switch on bank 3 (switching only, no signalling on SOD line)	Cyclic ROM test eval. circ.
on 1 1111 1 off 000 0	12BH	Switch on bank 4 (switching only, no signalling on SOD line)	Switch on bank 4 (switching only, no signalling on SOD line)	Not used

Figure 6.1-11 Test overview (contd.)

DISPLAY CICRUIT SELF-TEST (from Series G)

FAULT IN	REACTION			
CPU-2	Beep	Screen	LEDs	Comments
EPROM 0	4 x long	--	All ON	No self-test possible
EPROM 1	--	--	LOCAL flashes	--
EPROM 2	--	--	LOCAL flashes	--
EPROM 3	--	--	LOCAL flashes	--
EPROM 4	--	--	LOCAL flashes	--
RAM 0	2 x long	--	All ON	No retransmission
RAM 1	--	--	LOCAL flashes	--
RAM 2	--	--	LOCAL flashes	--
RAM 3	--	--	LOCAL flashes	--
Arith. pr.	--	--	LOCAL flashes	--
CPU 2A/2	2 x short 2 x long	--	All ON	No self-test possible
Coup. card 1	Beep	Screen	LEDs	Comments
RAM	4 x long	Dark	All ON	No retransmission
EPROM 1	4 x long	--	All ON	No retransmission
EPROM 2	--	--	REMOTE flashes	--
EPROM 3	4 x long		All ON	No retransmission
BSK	Beep	Screen	LEDs	Comments
	--	Dark	LOCAL+REMOTE flash	--

Figure 6.1-12 Error messages, display circuit self-test

C) Description of the individual tests

a) Common features of all tests

Test of the SOD line on the measuring circuit or master (see Fig. 6.1-13):
SOD line frequency = 0: Fault
SOD line frequency ≠ 0: OK
The test program in question also stores the "fault" in the variables TFEHLR and TFEHLR+1.
OK : TFEHLR contains "0" "K"
Fault: TFEHLR contains the error variable of the test (see description).*

NOTE: Correct storage of the "fault" in TFEHLER and TFEHLER+1 presupposes correct operation of the master CPU, display circuit CPU, measuring circuit CPU and their coupling!

This fault detection works with all test programs, but not with the following programs:
Run test: SOD line functions, no fault detection in TFEHLR
Monitor : No fault detection
Calibration: No fault detection
Exception: Tests on the master for bank-switching.
Here, no frequency is output on the SOD line; only static switching to the BANK in question takes place (only observable at the outputs of 90 IC 52!).

* Also applies to CPU 2A/2 (display ciruit CPU)

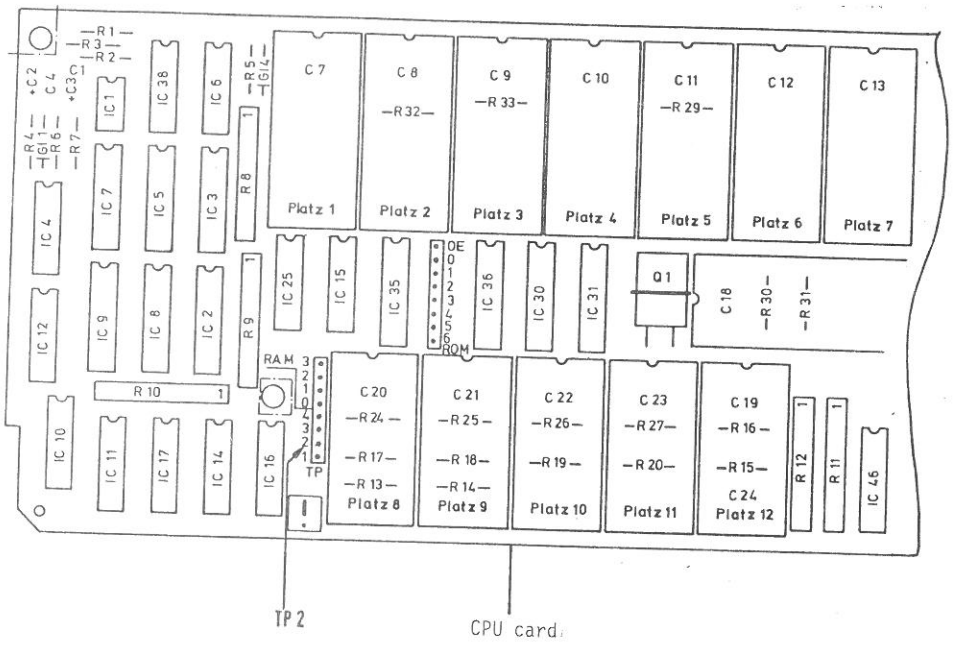


Figure 6.1-13 "SOD" connection

If a slender test clip of approx. 7 cm length is used, the CPU card to be tested need not be removed from the instrument and fitted on an adapter. Removal of the rear cover will suffice.

D) Fault identifications of the tests

ROM faults: TFEHLR = 1
TFEHLR+1 = Number of the faulty ROM
00H - Fault in ROM0
01H - Fault in ROM1
02H - Fault in ROM2
03H - Fault in ROM3
04H - Fault in ROM4
05H - Fault in ROM5
06H - Fault in ROM6

RAM faults: TFEHLR = 2
(non-destructive) TFEHLR+1 = Number of the faulty RAM
00H - Fault in cell test, RAM0
01H - Fault in cell test, RAM1
02H - Fault in cell test, RAM2
03H - Fault in cell test, RAM3

10H - Addressing error, RAM0
11H - Addressing error, RAM1
12H - Addressing error, RAM2
13H - Addressing error, RAM3

20H - RAM addressing error (A11, A12)

I/O faults: TFEHLR = 3
TFEHLR+1 = 0

APU faults: TFEHLR = 4
TFEHLR+1 = 0

BSK faults: TFEHLR = 5
TFEHLR+1 = Detailed fault description

IEC card : TFEHLR = 6
TFEHLR+1 = 0 

RAM faults: TFEHLR = 07H
(destr.) TFEHLR+1 = Number of faulty RAM
00H - Fault in RAM0
01H - Fault in RAM1
02H - Fault in RAM2
03H - Fault in RAM3

Note : TFEHLER is not used for CPU-2A/2 in Series A-F.

Run test : The program stops in the event of a fault. The faulty hardware can now be tested. Once the fault is eliminated, the CPU starts up again immediately. The test is merely intended to establish whether the processor starts up at all and has no other function, as there had been cases where the processor was unable to start up because of WAIT, etc.

E) Fault identifications in the tests of the evaluation circuit

All tests are started and analysed by the measuring circuit. In the evaluation circuit tests, the contents of the variables TFEHLR and TFEHLR+1 are always identical (in contrast to CPU-2 tests).

Cyclic overall test of evaluation circuit: TFEHLR = Bit 0 = HIGH -> LSB ROM faulty
Bit 1 = HIGH -> MSB ROM faulty
Bit 2 = HIGH -> LSB RAM faulty
Bit 3 = HIGH -> MSB RAM faulty

Cyclic I/O test of evaluation circuit : TFEHLR = 1 -> No interrupt from evaluation circuit
2 -> Program cannot be started
80H -> Gate 80H fault
81H -> Gate 81H fault
82H -> Gate 82H fault
83H -> Gate 83H fault

Cyclic RAM tests: See Overall test for analysis evaluation circuit
Cyclic ROM tests:

Note : The test can only be analysed directly with MONITOR version V003. For V002, refer to the "Table of evaluation circuit modes" E0 to E4 and the "Table of mode-dependent results of the evaluation circuit" in Section 10.3.

Sequence : Hold down the "0" key when switching on. This switches over to MONITOR mode. At the same time, the evaluation circuit is re-initialized, this including an internal RAM/ROM test, whose results can be polled:

I : 80. (ENTER) -> F0

According to Section 10.3.2, Addr. E5H means
"F0H" = "initialized; RAM/ROM O.K."
"F1H" = "initialized; RAM/ROM faulty"

By entering

I : 81. (ENTER) -> 0X

the position of the faulty RAM or ROM can be localized; the meanings are as follows:
00 ≙ O.K.
01 ≙ LSB ROM faulty
02 ≙ MSB ROM faulty
04 ≙ LSB RAM faulty
08 ≙ MSB RAM faulty

A more detailed breakdown of the fault can be obtained either by emulation or, to a limited extent, by manipulating input of output gates via the monitor.
The starting address of TFEHLR (see C) can be found under the addresses 9AH, 9BH in all instrument versions. In monitor version V003, it is easily possible to find the corresponding starting addresses either for the master "CPU 2/1" or for the measuring circuit "CPU 2/3". Monitor version V002 only allows this for the master "CPU 2/1".

Reading out the fault variables "TFEHLR" and TFEHLR+1"

- Enter the monitor via key "0" and "Mains ON" or from the measurement display with the "VAR MODE" key and softkey 1 (5 sec.).
- Select CPU 2/1 or 2/2 or 2/3.
- READ: 9A ENTER -> LSB of TFEHLR address
  ENTER -> MSB of TFEHLR address
- READ: MSB LSB ENTER
  Displayed byte = "TFEHLR"
  ENTER
  Displayed byte = "TFEHLR+1"

Example: - CPU 2/3 selected
- READ: 9A ENTER -> 009A.4D (LSB)
ENTER -> 009B.E9 (MSB)
- READ: E94D ENTER
-> E94D.4F (≙ ASCII O)
ENTER
E94E.4B (≙ ASCII K)

NOTE: Correct storage of the "fault" in TFEHLR and TFEHLR+1 presupposes correct functioning of the CPUs and their coupling!

Hex. equiv.	b_6 b_5 b_4 / b_3 b_2 b_1 b_0	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0 0 0 0	NUL	DLE	SP	0	@	P	`	p
1	0 0 0 1	SOH	DC1	!	1	A	Q	a	q
2	0 0 1 0	STX	DC2	"	2	B	R	b	r
3	0 0 1 1	ETX	DC3	#	3	C	S	c	s
4	0 1 0 0	EOT	DC4	$	4	D	T	d	t
5	0 1 0 1	ENQ	NAK	%	5	E	U	e	u
6	0 1 1 0	ACK	SYN	&	6	F	V	f	v
7	0 1 1 1	BEL	ETB	'	7	G	W	g	w
8	1 0 0 0	BS	CAN	(	8	H	X	h	x
9	1 0 0 1	HT	EM	)	9	I	Y	i	y
A	1 0 1 0	LF	SUB	*	:	J	Z	j	z
B	1 0 1 1	VT	ESC	+	;	K	[	k	{
C	1 1 0 0	FF	FS	,	<	L	\	l	¦
D	1 1 0 1	CR	GS	-	=	M	]	m	}
E	1 1 1 0	SO	RS	.	>	N	↑	n	~
F	1 1 1 1	SI	US	/	?	O	←	o	DEL

Figure 6.1-14 Table of ASCII codes

6.1.1.3 Troubleshooting with the aid of signature analysis

The principle of signature analysis is described in Section 2.3 of this Service Manual. The CPU board has a free-running switch (S 1/7 to S 1/10) for this purpose. If the settings of S 1/7 to S 1/10 are inverted, the processor addresses the entire memory area by incrementing the address by 1 each time and performing this operation cyclically after a RESET. In order to record ROM signatures, the associated ROM select (test point) must be used as the START/STOP signal. The use of the free-running switch, in conjunction with the pull-up resistors of the data bus and the RD2 signal via G1 2 to AD6, ensures that only a subset of the 8085 command set is executed.

Bit number :	7	6	5	4	3	2	1	Ø
Logic level :	H	L	X	X	X	X	X	H
Machine code:	1	Ø	X	X	X	X	X	1 = 81H..BFH

X = any, data line not disconnected.

Note: The free-running switch only affects data lines Ø, 6 and 7.

Figure 6.1-15 Value of the data bits for free-running

The commands involved are one-byte commands for arithmetic or logic operations which increment the program counter reading by one and thus yield a "program" with consecutive memory addressing.

If the most-significant bit A15 is used as the START/STOP frame, and if the processor increments the entire address range (from ØØØØH to FFFFH), each address line yields an unambiguous signature.

The free-running operation tests the heart of the microcomputer, namely

- a number of functions of the microprocessor and the circuits required for its operation, such as the clock generator circuitry,
- the address bus with drivers and decoders,
- the EPROM contents (including data bus), if the START/STOP frame is selected accordingly.

The I/O area and the RAMs cannot be tested in free-running mode.
The WORIS functions of the monitor program offer further testing capabilities.

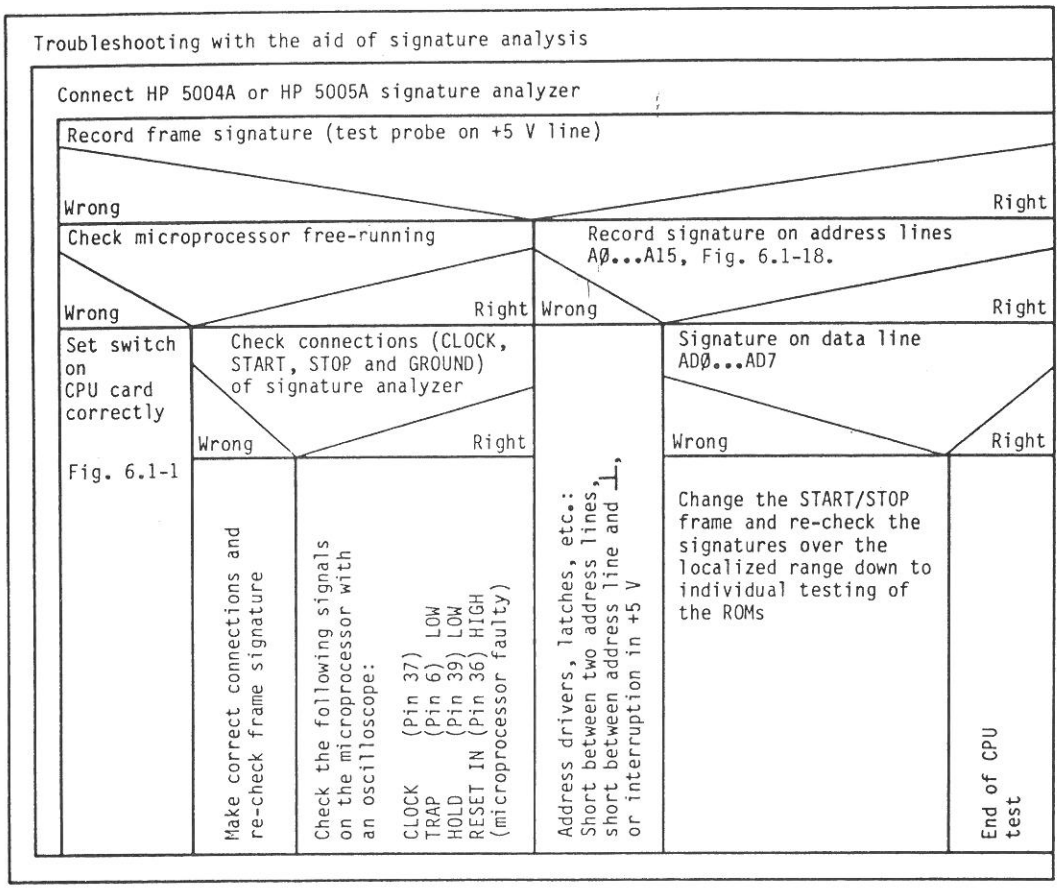


Figure 6.1-16 Structural diagram of troubleshooting

a) Troubleshooting in the event of a ROM fault

Troubleshooting is performed with the aid of the Hewlett-packard signature analyzer 5004A or 5006A*. Switches S 1/1 to S 1/10 on the CPU board must be set appropriately to activate the free-running mode (refer to CPU circuitry description for details). With the instrument switched off, set switch S 1 as shown in Fig. 6.1-1.

Measuring the data signatures:

Connect the signature analyzer:
Clock (⎍) at $\overline{RD}$: TP OE, GND to -pole C5

The signatures are checked at the outputs of the ROMs on the CPU board.

EPROM TP	IC	B.V.	START Connection	START Edge	STOP Connection	STOP Edge	
ROMØ	18		TP ROMØ	⎍	TP ROMØ	⎍	CPU card
ROM1	19		TP ROM1	⎍	TP ROM1	⎍	
ROM2	20		TP ROM2	⎍	TP ROM2	⎍	
ROM3	21		TP ROM3	⎍	TP ROM3	⎍	
ROM4	22		TP ROM4	⎍	TP ROM4	⎍	
ROM5	23		TP ROM5	⎍	TP ROM5	⎍	
ROM6	24		TP ROM6	⎍	TP ROM6	⎍	

Figure 6.1-17 Edge assignment of the START/STOP frame

Checking the frame:

The signature 0000 must be obtained at Pin 20 (CE) of the EPROM in question, since this signal is always LOW during the selected frame. The characteristic signature must appear at Pin 20 of all other EPROMs, since these are not addressed and Pin 20 is thus constantly HIGH. The frame signature corresponds to the signature on the +5 V line.
Since minor software modifications, even if they only affect 1 bit, result in a different signature on the data lines, make sure that the correct signature list is consulted.
The signature list is attached to the instrument. The exact location of the list is described in Section 3 under the heading "Instrument data".
If none of the 8 signatures is correct, there is most probably a fault on the address side, in which case the signatures of the address lines must be checked.

---

* Instruments from other manufacturers will not always produce the same signatures.

Address signatures

The address line signatures must be identical at all points. The signature on the CPU board, upstream and downstream of the address drivers and the address latches must be identical.
If the signatures on ADØ...AD7 are to be checked, the trailing edge of the ALE signal must be used as the CLOCK. However, ADØ, AD6 and AD7 are only valid directly on the microprocessor in free-running mode. In addition to the signatures of the address lines, the signatures of the chip select signals = decoded addresses and of the enable signals must also be checked.
The Table shown in Fig. 6.1-18 must be used for this purpose.

Test point	Signature
AØ (ADØ)*	UUUU
A1 (AD1)	5555
A2 (AD2)	CCCC
A3 (AD3)	7F7F
A4 (AD4)	5H21
A5 (AD5)	ØAFA
A6 (AD6)*	UPFH
A7 (AD7)*	52F8
A8	HC89
A9	2H7Ø
A1Ø	HPPØ
A11	1293
A12	HAP7
A13	3C96
A14	3827
A15	755U

Test point TP	Signature
ROMØ	4PØA
ROM1	12U3
ROM2	PCØ1
ROM3	F2A6
ROM4	6H49
ROM5	Ø996
ROM6	U3H5
RAMØ	PF2P
RAM1	8F14
RAM2	U81U
RAM3**	3UP7
IC 36 PIN 7	7A71
$\overline{V}_Ø$	5FU8
$\overline{V}_1$	29A6
$\overline{V}_2$	64HP
$\overline{V}_3$	1181
IC 35 PIN 7 = IC 15 PIN 6	P255

Notes:

START: ⌝	TP ROMØ
STOP: ⌝	TP ROMØ
CLOCK: ⌐	TP OE (ALE, connector Pin C12, ⌝)*
Stimulus:	Free-running
Characteristic signature:	0001

Figure 6.1-18 Address signatures (CPU board)

* ADØ, AD6 and AD7: only valid when measured directly on the microprocessor pins.

** Only applicable if the arithmetic processor is installed.

b) Troubleshooting in the event of a RAM fault

If a RAM fault occurs, address lines AØ to A7 should first be checked using signature analysis. Subsequently check the signatures at the chip enable inputs of the RAMs. Refer to the Section on "Address signatures".

Once this has been done, the data lines can be checked (see Fig. 6.1-19).

Test point	Signature	Remarks
The signature on lines DØ...D7 must be the same as the signatures on lines ADØ...AD7. (As the signature is dependent on the RAM contents, a check can only be made here as to whether the signature is identical over the entire signal path.)		↘ START: TP RAMØ...3 ↗ STOP: TP same as START ↗ CLOCK: TP OE Stimulus: Free-running

Figure 6.1-19 RAM signatures (data lines)

6.1.2 PCM-4 SELF-CALIBRATION

The PCM-4 calibrates itself after being switched on, at preselected regular intervals or almost every two hours (selectable with GEN. PAR 936). The essential sequence of this basic calibration is explained below.

This calibration process can be checked at the NF/VF output, socket [36]. The following signals (Figs. 6.1-20, 6.1-21) were recorded with a transient recorder and show the typical voltage profiles at the NF/VF output.

The elementary functions (System not complete, Clock missing, Meas. via Int. Dig. loop not possible) leading to an Error messages are tested before the actual calibration sequence.

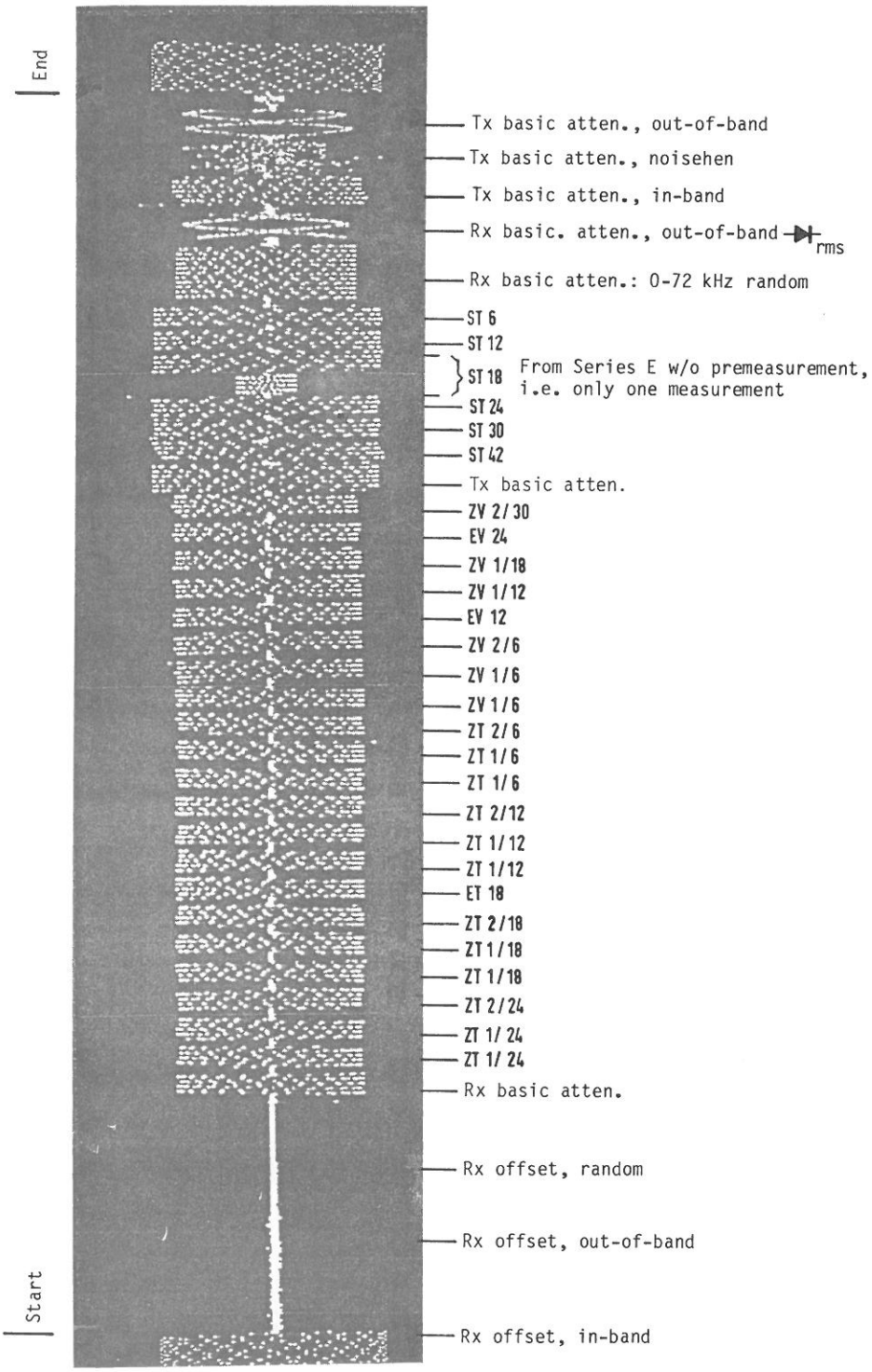


Figure 6.1-20 Calibration sequence up to and including Series D

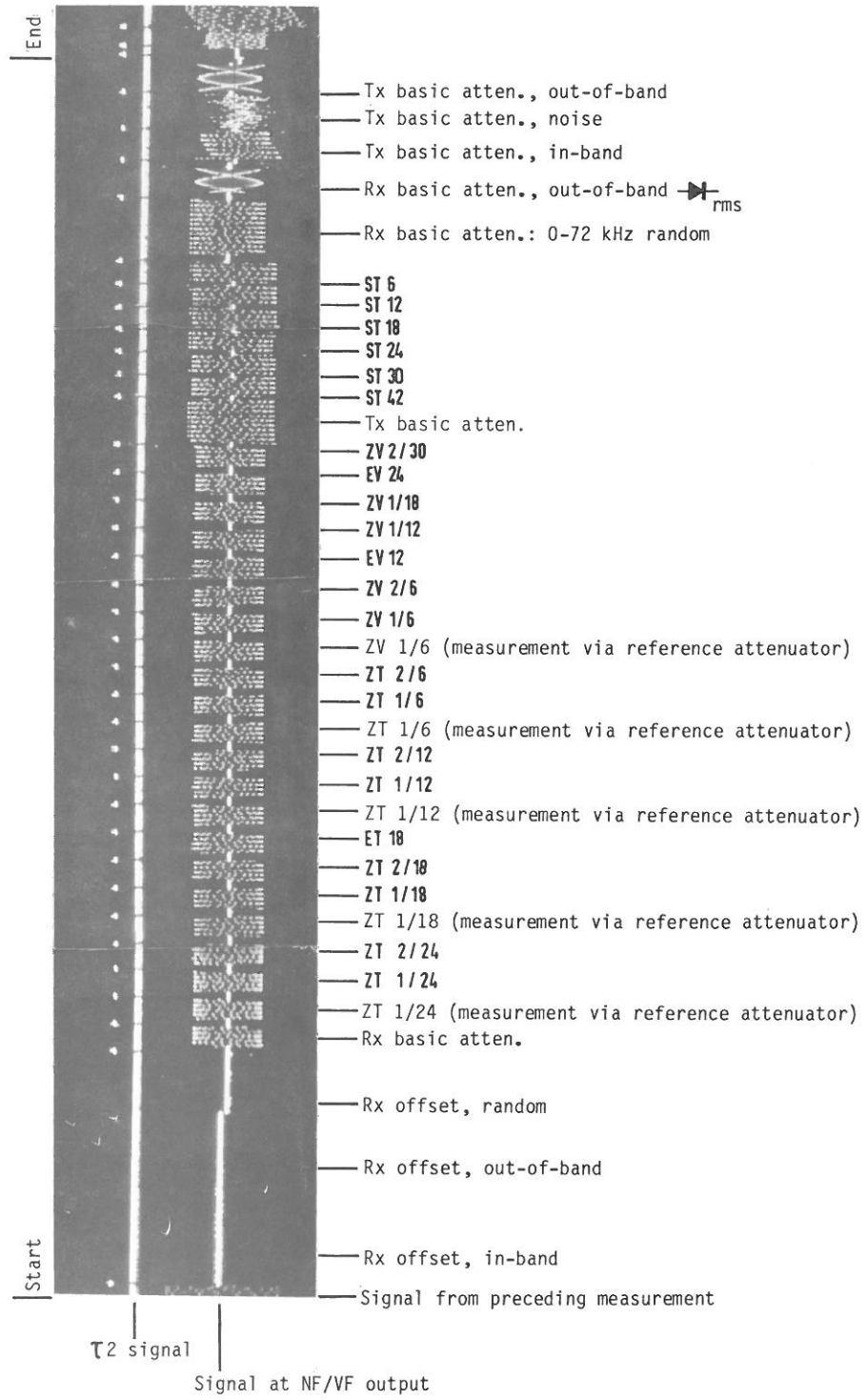


Figure 6.1-21 Calibration sequence from Series E onwards

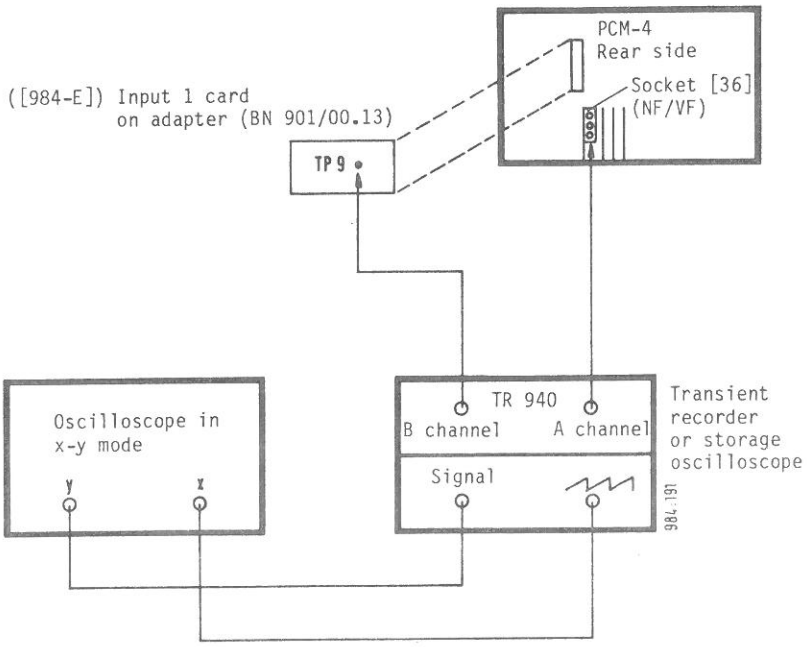


Figure 6.1-22 Test set-up

Key to Fig. 6.1-20:

ST 12 = Generator divider set to 12 dB
ZV 2/30 = Intermediate amplifier 2 set to 30 dB
EV 24 = Input amplifier set to 24 dB
ET 18 = Input divider set to 18 dB
ZT 2/18 = Intermediate divider 2 set to 18 dB

- Tap the $\tau 2$ signal at TP 9 of Input 1 card.
- The first $\tau 2$ signal (before the Rx offset in-band measurement) switches off the generator.
- The first 3 calibration measurements (Rx offset measurements) do not generate a $\tau 2$ signal.

Basic calibration sequence (origin of the absolute error)

The following diagram (Fig. 6.1-23) schematically shows the basic calibration performed automatically while the screen displays the word "CALIBRATING".
For explanation, interval numbers are shown at the top edge to divide the diagram into sections.
The "Internal coupling" block circuit diagram (Fig. 6.1-24) illustrates the switching of signals between the functional blocks.

Basic calibration is initiated by applying -24.08 dB to the receiver (Rx) from the calibration voltage source in the generator section. This level (1) is used by the receiver unit as a defined level. The true measured receiver level (error level) (dark, broad bar) must thus be corrected to the defined calibration level. This correction "a" (dark, narrow bar) is made by software-linked computation and specification of a software correction value in the level evaluation unit.

(2) In the second step, the send level derived from the calibration level is measured. The amplifier and divider errors in the generator (Tx) yield the Tx error bar "b". In order to calibrate the generator output to the correct value, the generator output is connected directly to the Rx unit, i.e. the Rx unit calibrated in (1) is now used as the calibration measuring point (thin horizontal line "C1"). The output level of the Tx unit is changed by adjusting the "fine divider" downstream of the calibration voltage source until the reference level of the Rx unit ("C1", thin line) is reached. This setting of the fine divider is then used as the reference setting for the send level until the next CAL operation. It compensates for the attenuation, amplification and divider errors of the generator section.

(3) When the Tx calibration in (2) has been completed, the level passed through the calibration source is - as described - present at the generator output. (The attenuation, amplification and divider errors of generator and receiver have been corrected out by calibration.)
When the instrument is tested by the manufacturer, this level is measured with an external milliwatt power meter (EPM-1) -> Actual-value check "d1".

(4) If this level does not match the required value (reference level), the value of the calibration level of the calibration voltage source must be changed. It is based on a digital control word predefined by the switch setting of a DIP switch (10 S 1/3), i.e. a change in the switch combination changes the calibration level. If the calibration operation is re-started after manual switching of 10 S 1/3, this change is adopted and taken into account for the calibration operations (1) - (2).

Adjustment and calibration are repeated until the "ACTUAL value" of the Tx output level in checking stage (3) corresponds to the reference level. The last calibration operation of this type is shown in sections (7) (6) (5).
The Tx output now supplies a level which only deviates from the reference level by the quantization errors of the fine divider, the DIP switch and the reading error on the EPM-1.

(5) The "correct" level at the output is nevertheless still subject to the following uncertainties:

- Quantization error FINE DIVIDER	0.2 ... 0.4 mB
- Quantization error DIP SWITCH *	0.2 mB
- Absolute error, EPM-1	1.2 mB
- Reading uncertainty, EPM-1	≈0.2 mB
Accuracy of manufacturer's calibration	± 2.0 mB

This does not include the error resulting from ageing of the calibration voltage source and its TC, whereas the ageing and TC of the other gain and attenuation-determining components are eliminated with each CAL operation. This can be estimated at approximately another ± 2 mB.

* Also see Section 7.3 "Setting of 10 S 1/3"

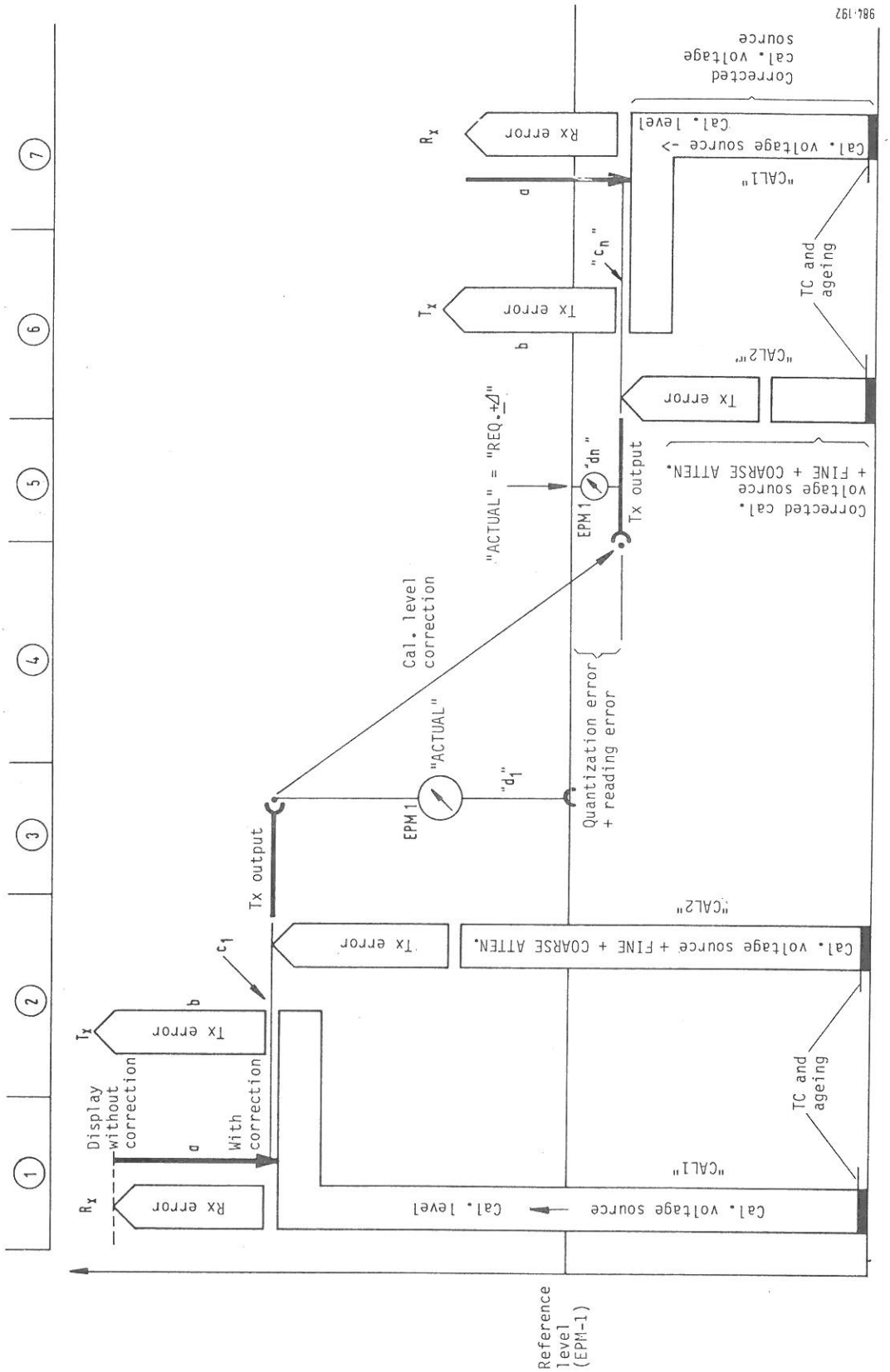
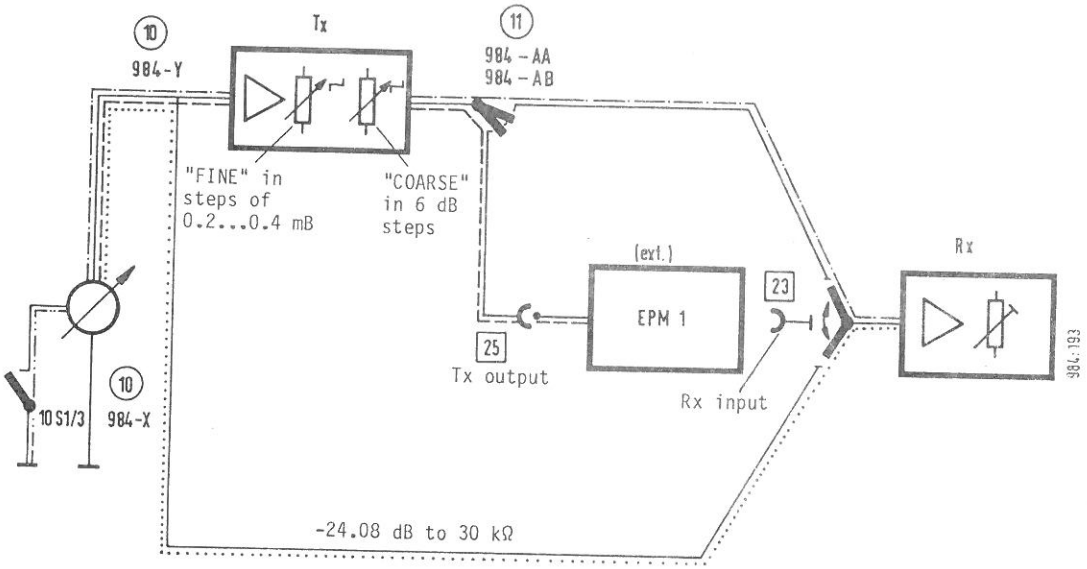


Figure 6.1-23 Basic calibration sequence

Internal coupling between - Calibration voltage source
- Tx (generator)
- Rx (receiver)
- EPM-1 (external)



1 Rx calibration.....
2 Tx calibration_._._._._
3 Check of Tx level (visual on EPM-1)_ _ _ _ _ _ _ _
4 Calibration level correction (manual with DIP switch)_ _ . _ _ _ _ _ _ _ _ . _ _ _ _ _ _ _ _ . _ _

Figure 6.1-24 "Internal coupling" block circuit diagram

Path of calibration voltages CAL 1 and CAL 2

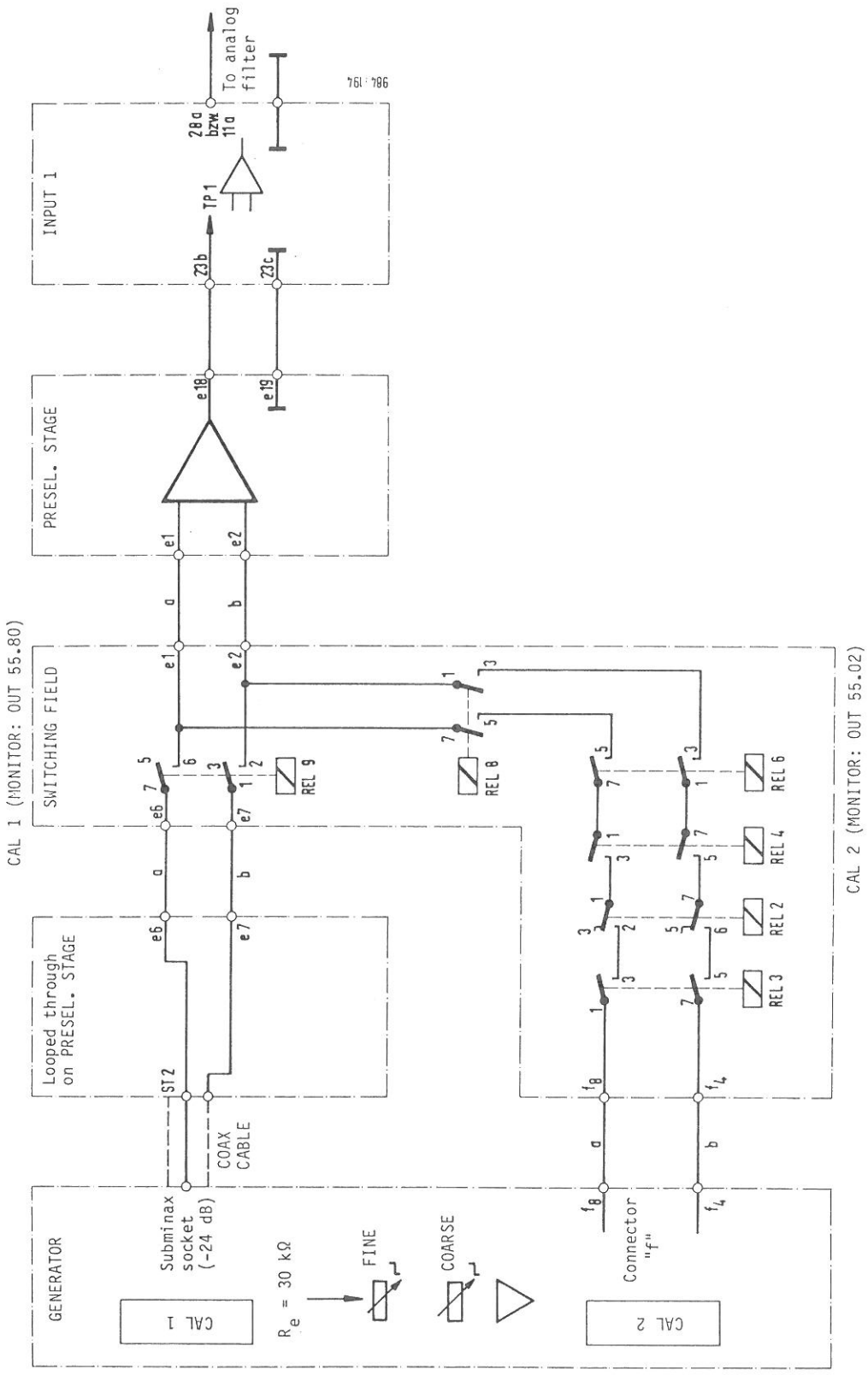


Figure 6.1-25 Path of CAL 1 and CAL 2

Switching the CAL loops via the monitor

If calibration does not work faultlessly, first use an external level generator/level meter to establish whether the analog receiver and/or analog generator is working.
Hold down key [9] during "Mains ON" to skip calibration. Then proceed as follows:

Entry	Display
[GENRL RESET]	MODE A list
[1] [1]	A11 display
[MAN/R]	A11 display

Connect external level meter to socket [25] -> Display approx. -10 dBm
Connect external level meter to socket [23] -> Press [START] key -> Display on PCM-4 matches the level set on the level generator

If the analog generator and receiver are working, the fault lies in one of the calibration loops CAL 1 or CAL 2.

The procedure for adjusting the calibration loops via the MONITOR is described below. The signal flow can then be tracked on the basis of the circuit diagram and with the oscilloscope.

Entry	Display
[GENRL RESET]	MODE A list
[1] [1] [ENTER]	Display A11
[VAR MODE] softkey 1 (hold down the top right key on the monitor for appr. 5 sec)	MONITOR V003
[DIGIT WORD] [DIGIT WORD]	CPU-2/3
* CAL 1: [OUT] [5] [5] [.] [8] [Ø] [ENTER]	0:55.80!
[RTN] [RTN] [START]	Display A11 (measurements approx. -31 dBm0)

If the measurements are wrong, check calibration loop CAL 1 (see Fig. 6.1-25).
To set calibration loop CAL 2 instead of *CAL 1, enter the following string (all other entries are the same):
CAL 2: [OUT] [5] [5] [.] [Ø] [2] [ENTER] 0:55.02!

The measurements should be approx. -10 dBm0.
If they are wrong, check calibration loop CAL 2 (see Fig. 6.1-25).

6.2 TROUBLESHOOTING IN THE ANALOG DIGITAL SECTIONS (MEASURING SECTION)

Faults in the analog section can be attributed to three fundamental circuit groups:

- Faults in the digital interfaces to the control section. The possible fault sources are multipoint connectors, contact combs, power supplies and buffer ICs.
- Faults in command implementation occur, for example, in relays or CMOS analog switches.
- Faults due to faulty analog components. These may be capacitors, resistors or operation amplifiers.

Wiring faults, such as faulty through-platings, interrupted conductors, broken cables and conductor shorts rank above all three fault groups.

Fault classification

If an assembly identified by troubleshooting cannot be replaced, further fault classification can be attempted, as indicated at the beginning of this Section.

The following Tables provide assistance in this context:
- Gate assignment plan (Section 10.2)
- Divider driving diagrams (Section 10.2)

Faults on the digital interfaces can be detected by checking data traffic on the basis of the "Input/output gate" Tables. It is always possible to ascertain whether a setting command has been given and whether it was given correctly. A list of the addresses can be found in Section 10.2.
The monitor offers the possibility of entering or polling data statically (see Section 4.4). The above Tables are used as a basis for comparison in this context.

Data from the data bus are in each case buffered at the time of address output.

The test probe can be used to check that the data present in the measuring section buffers are correct. Thus, it can be established whether the fault is located upstream or downstream of this interface. If the fault is upstream of the interface, i.e. in the area of the data bus or address coder, the data bus could then be observed with an oscilloscope triggered by the individual decoded addresses.

In terms of time, a data change may only take place before the positive edge of the address pulse. In this respect, particular attention must be paid to the fact that, when the data bus drivers are under capacitive load, the edge rise is always delayed, with the result that the data become valid at a later time.

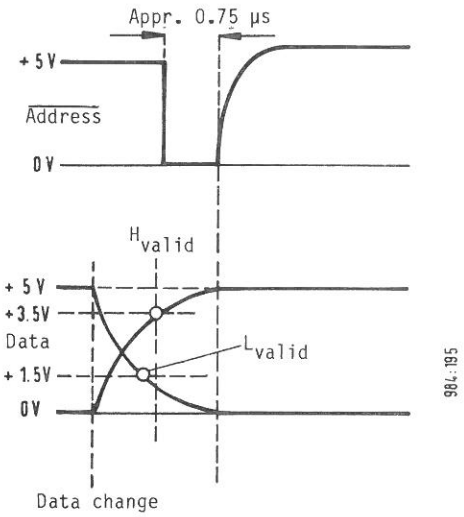


Figure 6.2-1 Data transfer between control section and measuring section

Example of the use of the gate assignment plan and divider driving diagrams (in Section 10.2)

The following example is intended to illustrate how to work with the Tables in Section 10.2. It describes the setting of the output divider of Analog generator 2 (see Tables 10.2-7 and 10.2-8):

Settings on the instrument:

- e.g. MODE A11, MAN/R, L = 0 dBm (≙ 12 dB divider setting)
- Call up monitor (see Sections 2 and 4)
- Select CPU 2/3
- OUT: 4B.04 ENTER (≙ Δa of 12 dB)
  - 04 — Attenuation as per Tables 10.2-7 and 10.2-8
  - 4B — Port address
- OUT: 46.00 ENTER (transfer to output latch)**
- RTN*
- RTN*

** Connect sockets [23] and [25], START -> Display: -12 dBm0
(If an external level meter is connected to socket [25], the settings made can be observed directly after this entry, meaning that the items marked * are superfluous.)

I/O timing control

In order to prevent I/O bus conflicts in an instrument due to the delay of the addresses decoders, the CPU cards generate not only the I/O data and address bus, but also special strobe signals $\overline{RD}$, $\overline{WR}$ and $\overline{LSS}$ (Low-Speed Strobe). $\overline{LSS}$ is (logically) combined with the two other strobe signals in an AND circuit:

Generation of the $\overline{LSS}$ signal:

Each I/O operation consists of three time steps:
1. Addresses valid: Settling time for peripheral decoders
2. Strobe signal LOW: Data transfer ($\overline{RD}$ and $\overline{WR}$)
3. Waiting time: Build-up period for peripheral decoders.

The three time steps can be varied (independently) by the three card inputs B 1-3. B 1-3 represents a 3-bit number in positive logic:

$n = \langle B3, B2, B1 \rangle$, $0 \leq n \leq 7$

The I/O bus drivers in the PCM-4 are set to maximum speed (by soldered bridges on the CPU cards).
This results in the following timing diagram for the I/O strobe signals and the I/O data and address bus:

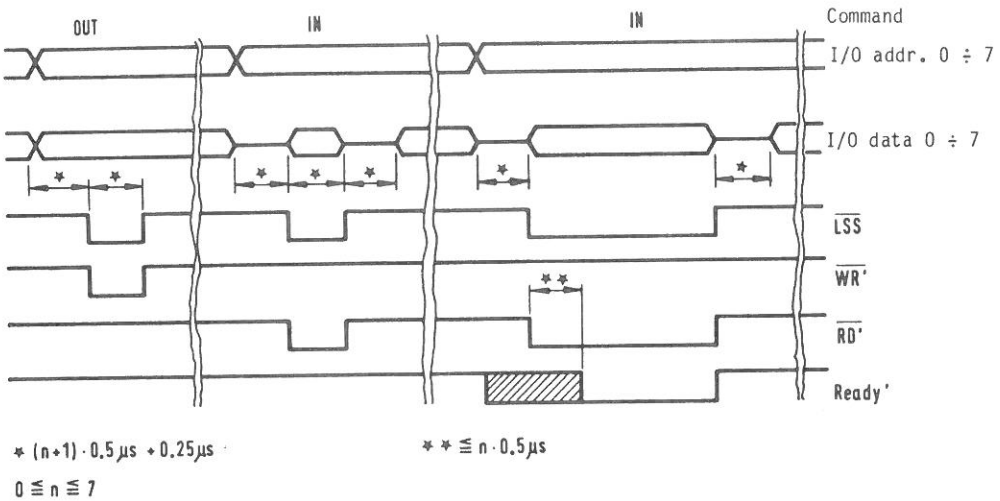


Figure 6.2-2 I/O timing

6.2.1 TEST OF THE DIGITAL INTERFACES

	Entry	Reaction
1	Connect Bu [21] Tx SIGNAL and Bu [20] Rx SIGNAL with CF cable. GENERAL RESET, MODE A 11, [D-D]	All LEDs to left of Bu [20] OFF.
2	Disconnect Bu [20] - Bu [21].	LED NO SIGN lights up.
3	Re-connect Bu [20] - Bu [21].	LED NO SIGN goes out.
4	Enter GEN. PAR. 612 AIS	LED AIS lights up.
5	GEN. PAR. 213 Tx FRAME TYPE G.732/TS 16 TELEPH. (GEN. PAR. 223 is autom. selected) GEN. PAR. 613 ERROR INSERTION ON GEN. PAR. 624 FRAME ALGNMT WORD ERRORS 3 IN 4	LED AIS goes out. LED NO FRM lights up.
6	GEN. PAR. 623 FRAME ALGNMT WORD ERRORS 2 IN 4	LED NO FRM goes out.
7	GEN. PAR. 211 Tx FRAME TYPE G.732/TS 16 INT. (GEN. PAR. 221 is autom. selected) GEN. PAR. 626 MULTIFRAME ALGNMT ERRORS 2 IN 2	LED NO MFRM lights up.
8	GEN. PAR. 625 MULTIFRAME ALGNMT ERRORS 1 IN 2	LED NO MFRM goes out.
	GEN. PAR. 611 INSERTION OFF GEN. PAR. 422 INPUT IMPEDANCE > 3 kΩ	LED Z > 3 kΩ lights up.
9	GEN. PAR. 421 INPUT IMPEDANCE 120/75 Ω	LED Z > 3 kΩ goes out.
10	Press [RTN] softkey Press key [11] DIGIT WORD Select <1> TELEPH. CHANNEL Press [RTN] softkey Enter VAR. MODE 263 8-BIT WORD 10101010.	The octet entered is displayed on light-emitting diodes 1 - 8.
11	Enter VAR. MODE 263 8-BIT WORD 01010101.	LED 1 - 8: 0 1 0 1 0 1 0 1
12	Press [RTN] softkey. Press key [11] DIGIT WORD. Select <2> FRAME ALIGNMENT SIGN.	LED 1 - 8: 1 0 0 1 1 0 1 1
13	Select <3> NOT FRM. ALIGNMENT SIGN.	LED 1 - 8: 1 1 0 1 1 1 1 1
14	<4> MULTIFR. ALIGNMENT SIGN. BIT 1 ... 4 NOT MULTIFR. ALIGN. SIGN. BIT 5 ... 8	LED 1 - 4: 0 0 0 0 LED 5 - 8: 1 0 1 1
15	<5> SIGNALLING CHANNEL Tx BIT 1 ... 4 Rx BIT 5 ... 8	LED 1 - 4: 1 1 1 1 LED 5 - 8: 1 1 1 1
16	Press [RTN] softkey Enter SEND CHAN. 8 Enter GEN. PAR. 517 FREE TS (MFRM): 1010 Enter GEN. PAR. 518 SIGNALLING: 0101	LED 5 - 8: 1 0 1 0 LED 1 - 4: 0 1 0 1
17	Enter GEN. PAR. 517 FREE TS (MFRM): 0101 Enter GEN. PAR. 518 SIGNALLING: 1010	LED 5 - 8: 0 1 0 1 LED 1 - 4: 1 0 1 0

Figure 6.2-3 Test of the digital interfaces

6.2.2 TROUBLESHOOTING IN THE EVALUATION CIRCUIT

a) Description

Communication with the evaluation circuit takes place via the two register files with the registers WØ - W3 and RØ - R3.

Definition:

Designation	WAR	RAR	IOA1	IOAØ	Use
WØ, W_8Ø	Ø	1	Ø	Ø	Mode entry with start
W1, W_81	Ø	1	Ø	1	Parameter entry
W2, W_82	Ø	1	1	Ø	
W3, W_83	Ø	1	1	1	
RØ, R_8Ø	1	Ø	Ø	Ø	Evaluation circuit status display, except for BA ØX, EØ, E1, E6-EA
R1, R_81	1	Ø	Ø	1	Result output
R2, R_82	1	Ø	1	Ø	
R3, R_83	1	Ø	1	1	

Figure 6.2-4 Function of the register files

The write and read address $\overline{WAR}$ and $\overline{RAR}$ pre-decoded from IOA4 - IOA7 is decoded with 8 in the PCM-4, i.e. RØ-R3 and WØ-W3 have the I/O addresses 8ØH-83H.

An evaluation circuit measuring cycle is implemented as follows:

1. Transfer parameters
2. Transfer mode and thus start
3. Wait for "finished" message
4. Fetch results

If necessary, parameters are first loaded into the 16 x 3 byte parameter buffer. Mode 1XH is used to load parameter No. X, which must be in W_81 - W_83, into the parameter buffer (X = Ø ... F).

Further parameters (e.g. number of samples) are then loaded into W_81 - W_83 in accordance with the mode.

The evaluation circuit is then started by loading the mode into W_8Ø.

The number of the mode and the required parameters can be found in the Mode Table.

As long as the evaluation circuit is busy, status register R_8Ø contains 2XH = busy with MODE X. When the mode has been completed, the "finished" message line FMAR is set to HIGH. R_81 - R_83 then contain ØØH and R_8Ø contains the status 3X = finished with MODE X or 4X = Fault No. X. The results are available in the 16 x 4 byte result buffer of the evaluation circuit. Mode ØXH (X = Ø ... F) transfers result No. X into output registers R_8Ø ... R_83. All results are fetched sequentially from the evaluation circuit in this way.

The mode-dependent meaning of the 16 results can be found in the Results Table.

Res. No. 14 and Res. No. 15 have the same meaning for all modes (exceptions E4, E5, FØ):
Res. No. 14 contains the input status before the measurement.
Res. No. 15 contains the input status after the measurement.
However, this is only required for test purposes.

The evaluation circuit can be interrupted with the command FØH or FFH while performing a mode!
The command FØH causes additional re-initialization and a RAM/ROM test (software reset). If FFH is used for interruption, the status in R_8Ø is: 5XH = interruption in mode X (exception: Mode 4, error measurement).

Manual control via monitor:

The evaluation circuit can be controlled manually with the PCM-4 monitor functions.
The commands OUT 8Ø.XX ... OUT 83.XX and IN 8Ø ... IN 83 are used to write and read the communication registers W_8Ø ... W_83 and R_8Ø ... R_83, as shown above.

Select CPU-2/3 beforehand, since communication with the evaluation circuit always takes place via CPU-2/3!

b) General structure of the evaluation circuit software

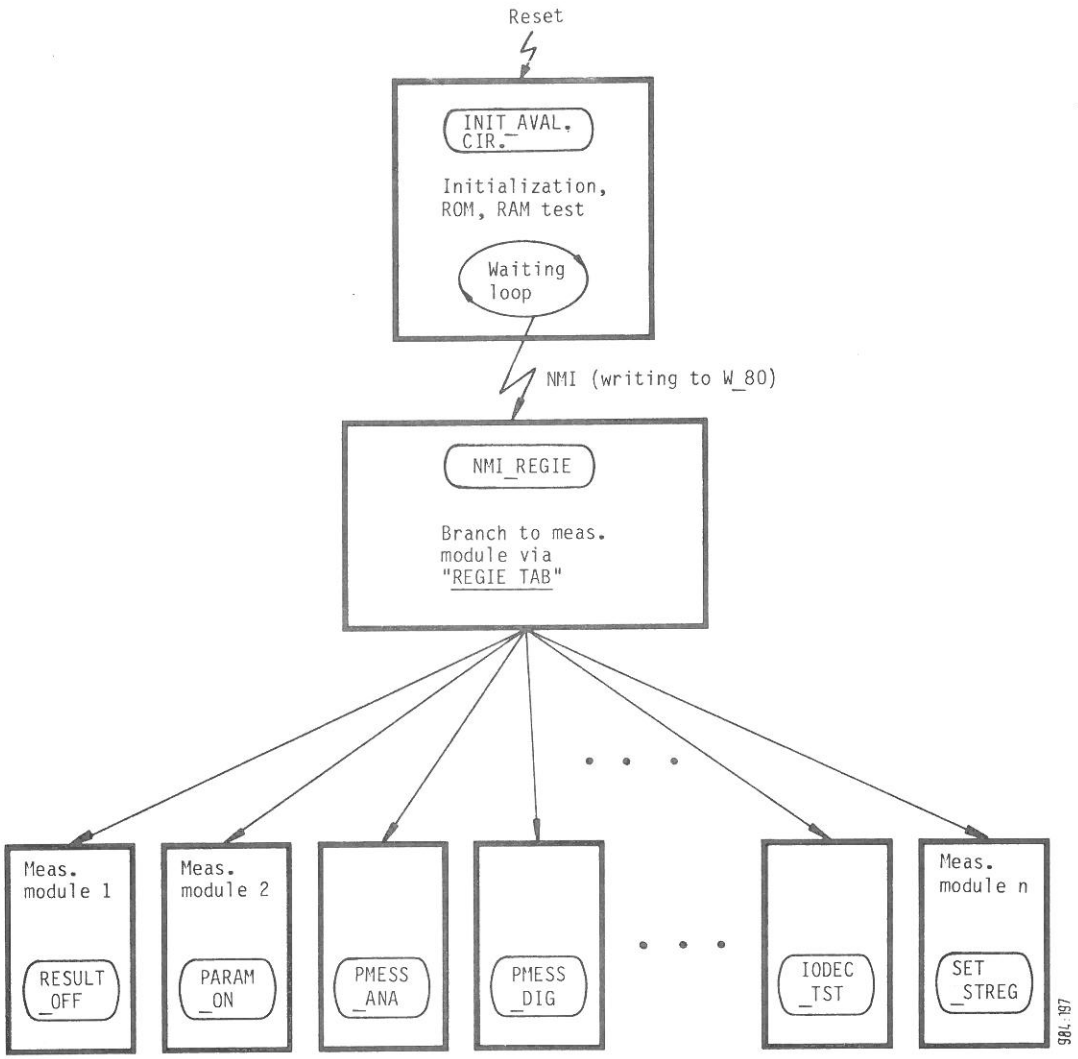


Figure 6.2-5 Structure of the evaluation circuit software

c) Test capabilities

Instruments required:

- PCM-4
- Signature analyzer
- Oscilloscope
- Frequency counter (possibly)

Evaluation circuit on adapter card [984-AC].
As-delivered settings of the evaluation circuit card:
S1/1 to S1/7: Closed
S8 : Open
S1/9 : Closed
S2 : Set to N

Summary

A free-running setting, RAM test, ROM test and other software tests are available for testing (see Mode Table of the evaluation circuit, Mode E).

When the evaluation circuit receives a reset pulse via PIN 13c of the multipoint connector, re-initialization is carried out with a ROM and RAM test. The test result is present in the status register.

When the PCM-4 is switched on, this result is polled and a test of the circuit coupling is also carried out. If a fault is detected at this time, the message "EVAL. CIRCUIT RAM/ROM O.K." is not displayed and the PCM-4 stops in this condition (in this case, see below for troubleshooting).
The overall check is divided into five tests:
Test 1: Computer core test 1: Free-running test
Test 2: Computer core test 2: RAM/ROM test
Test 3: Peripheral coupling test (I/O address decoder, transceiver, control register)
Test 4: Circuit coupling test
Test 5: Signal input test

Start-up:

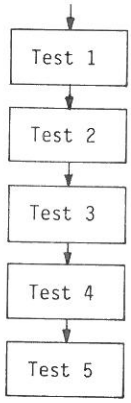


Figure 6.2-6 Test sequence

Display "Eval. circuit o.k." fails to appear after switching on the PCM-4

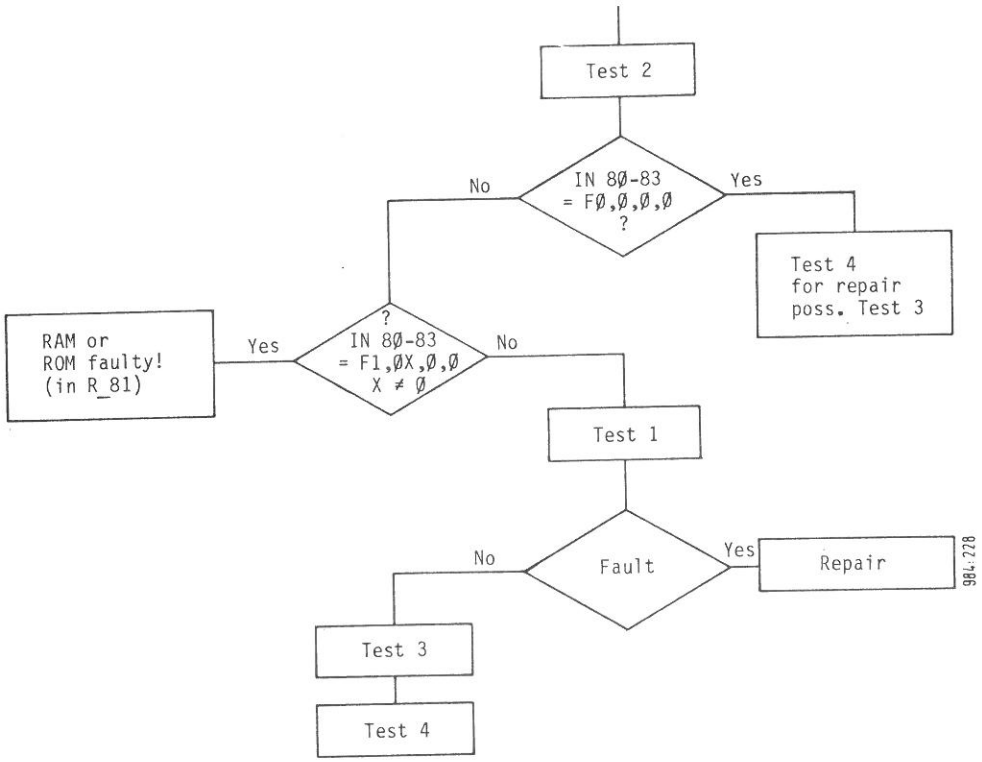


Figure 6.2-7 Test sequence

These tests presuppose that the tests with lower numbers revealed no faults!
Example: Test 3 presupposes that Test 1 and Test 2 revealed no faults!

Test 1: Free-running test (computer core test 1)

Check clock generator (IC 1).
An 8 MHz signal must be present at IC 1/Pin 8 and IC 4/Pin 19. Possibly align to 8 MHz with the frequency counter at C 1.
Fault sources: IC 1, Q 1, C 1, R 1, R 2.
Switch on free-running: S1/1 to S1/7: open
S1/8: closed
Check the basic function of the microprocessor (IC 1) and address latches (IC 5, IC 6).
The check is performed with the signatures below on address bus A1 - A15. They are independent of the software revision.
Fault sources: IC 4, IC 5, IC 6, IC 8/1, IC 9
Line interruption
Free-running circuit (S 1, GL 1)
Check IC 9: TP 7 ≅ A15
TP 8 ≅ A15

Free-running signatures on address bus A 1 - A 15:
Clock: ⌐ TP 4; Start: ¬ TP 7; Stop: ⌐ TP 7; Frame signature: 1180

A 1	0U7U	A 6	108P	A 11	0P0P
A 2	1180	A 7	A7A2	A 12	0F62
A 3	0108	A 8	4PCC	A 13	H6AA
A 4	1100	A 9	FF4F	A 14	P254
A 5	5342	A 10	5HC4	A 15	1180

Figure 6.2-8 Free-running signatures

Check EPROMs (IC 11, IC 12) and data bus

The signatures in signature list 984-0093.xxx are used for checking. The signatures depend on the software revision.
Fault sources: For faults on D Ø - D 7 : IC 11
For faults on D 8 - D 15: IC 12
Or: line interruption

Check peripheral data bus and IC 13, IC 14 (transceiver)

First ensure that $\overline{\text{IORD}}$ = HIGH (IC 13, IC 14, Pin 1). Then switch S 2 to "chassis" so that the data bus D Ø - D 15 is connected to the peripheral data bus, i.e. the data bus signatures must be present at all points of the peripheral data bus PD Ø - PD 15.
Fault sources: IC 13, IC 14 faulty, line interruption.

Return S 1 and S 2 to their normal settings!

Test 2: RAM and ROM test

A RAM and ROM test is always performed before re-initialization (started by a hardware or software reset). The test results are present in the status register and the output data registers:

RAM/ROM O.K.: R_80 = FØH, R_81 = ØØ
R_82 = ØØ , R_83 = ØØ

RAM and/or ROM faulty: R_80 = F1H, R_81 = ØXH* (X = 0!)
R_82 = ØØ , R_83 = ØØ

*: X = Bit 3, Bit 2, Bit 1, Bit 0
Bit 0 = 1: LSB ROM (IC 11) faulty
Bit 1 = 1: MSB ROM (IC 12) faulty
Bit 2 = 1: LSB RAM (IC 7) faulty
Bit 3 = 1: MSB RAM (IC 10) faulty

Test implementation:

Switch on the PCM-4 while holding down the "0" key. The PCM-4 is then immediately in the monitor status. Read the test result with IN 80 to IN 83. This presupposes that the output direction of the circuit coupler is working. This may be assumed as highly probable if the result in R_80 - R_83 is FØ,Ø,Ø,Ø or F1,ØX,Ø,Ø, where X ≠ Ø! If this is not the case, although Test 1 was completed without revealing faults, first check the circuit coupling with Test 3 and Test 4 before subsequently repeating Test 2.

Test_3: Peripheral_coupling test

The PCM-4 must be in the monitor state. First disable the "Digital signal trigger", "Analog signal trigger" and "$\overline{F1}$/F2" signals, so that no interrupt (NMI) is generated.
This is set by OUT 9Ø.1
OUT 4Ø.1
OUT 71.Ø.

Execution of OUT 8Ø.EB starts the following test program:

A block of 4 pulses is emitted at each of the 8 outputs of IC 18 (I/O address decoder) at intervals of approx. 43 µs. The pulses in the block are 1.25 µs apart. The pulses are output in the order Pin 4, 5, 6, 7, 12, 11, 10, 9.

Control register IC 25 is loaded with the value incremented by 1 at each write operation, with the result that outputs Q Ø - Q 5 act as a 6-bit counter.

The following signatures must then be present:
START: ⌐ TP 11
STOP : ⌐ TP 11
CLOCK: ⌐ TP 4 ($\overline{RD}$) Frame signature: 3CA3

IC 18, Pin 2	U22P	IC 18, Pin 5	2242
IC 18, Pin 3	Ø4FA	IC 18, Pin 6	94CA
IC 18, Pin 4	HA17	IC 18, Pin 7	81OF

Figure 6.2-9 Signatures 1

START: ⌐ TP 11
STOP : ⌐ TP 11
CLOCK: ⌐ TP 5 ($\overline{WR}$) Frame signature: 4596

IC 18, Pin 9	4PH2	IC 18, Pin 12	3522
IC 18, Pin 10	U1HU	IC 18, Pin 13	CUOH
IC 18, Pin 11	FUC9	IC 18, Pin 14	816C
IC 25, Pin 2	8C36	IC 25, Pin 10	HF87
IC 25, Pin 5	FA11	IC 25, Pin 12	CC34
IC 25, Pin 7	41F7	IC 25, Pin 15	4596

Figure 6.2-10 Signatures 2

This checks the address decoders (IC 8, IC 18) and the control register (IC 25).

The above tests presuppose that the evaluation circuit executes the appropriate task in accordance with the mode written into the mode register (W_80)!

If the aforementioned signals are not generated, the following must be checked first:

1. Is an interrupt pulse (NMI) generated at IC 4, Pin 17, when OUT 80.00 is executed?
   Examine path IC 22/2 -> IC 21/2 -> IC 21/3 -> IC 3/2.

2. NMI Impuls present!
   Is the input register file read? In other words: are several pulses generated at IC 18, Pin 1 ($\overline{IORD}$) and IC 15, Pin 11, IC 17, Pin 11 when OUT 80.00 is executed?
   If yes:
   Examine path IC 16 -> IC 15, IC 17 -> IC 14.
   If no:
   I/O address decoder (IC 8, IC 18) or CPU (IC 4) faulty.

Test_4: Circuit_coupling_test

Execution of OUT 80.E1 starts a test program in the evaluation circuit which dynamically transfers the contents of the input register file (IC 15, IC 17; W_80 - W_83) to the output register file (IC 19, IC 20; R_80 - R_83). The test program is terminated with OUT 80.FF.

```
E.g.: OUT 80.E1     ; Start test program
      OUT 80.AA   ⎫
      OUT 81.55   ⎬ Output test pattern
      OUT 82.FF   ⎪
      OUT 83.00   ⎭
      IN 80~.AA   ⎫
      IN 81~.55   ⎬ Read test pattern
      IN 82~.FF   ⎪
      IN 83~.00   ⎭
```

Test with further test patterns!

```
      OUT 80.FF     -> Terminate program
```

If a fault occurs, modes E6 to E9 can be used to establish whether the fault is in the input register file or the output register file.

OUT 80.E6 -> IN 80 to IN 83 $\stackrel{!}{=}$ ØØ
OUT 80.E7 -> IN 80 to IN 83 $\stackrel{!}{=}$ FF
OUT 80.E8 -> IN 80 to IN 83 $\stackrel{!}{=}$ AA
OUT 80.E9 -> IN 80 to IN 83 $\stackrel{!}{=}$ 55

```
E.g.: OUT 80.E1     (Start I/O test)
      OUT 82.55     (Test pattern 55)
      IN 82 ~ 54    => Fault
      OUT 80.FF     (Interrupt evaluation circuit)
      OUT 80.E9     (Output test with pattern 55)
  a) IN 82 ~ 55     -> Input path faulty
  b) IN 82 ~ 54     -> Output path faulty
```

Test_5: Signal_input_test

PCM-4 setting: Mode A 11, [D-D]
Connect 2 Mbit output and 2 Mbit input

Test of filter signal input (IC 23, IC 24) and octet input (IC 26, IC 27):

Execution of OUT 80.EA starts a test program in the evaluation circuit which dynamically (sampling frequency ≈ 87 kHz) transfers the filter signal to R_80, R_81 (LSB, MSB), the octet signal to R_82 and the signals at the signal gate (IC 22/1) to R_83.

1. Setting: VAR. MODE 263:00000000 (const. octet)
   Monitor: OUT 70.1E
   OUT 80.EA

The following must then be read:
IN 80 ≙ E0; IN 81 ≙ EF; IN 82 ≙ 55

2. Setting: VAR. MODE 263:11111111
   ⇝ IN 80 ≙ 7C; IN 81 ≙ 02; IN 82 ≙ AA

3. Setting: VAR. MODE 263:10101010
   ⇝ IN 80 ≙ 80; IN 81 ≙ 5E; IN 82 ≙ FF

4. Setting: VAR. MODE 263:01010101
   ⇝ IN 80 ≙ FA; IN 81 ≙ FF; IN 82 ≙ 00

Test of the signal gate (IC 22/1):

(Same setting as before)
IN 83 = 03H and ØBH alternately, but not regularly!
OUT 71.0 (switch F1/F2 signal = Ø)
Connect Pin 5C of the multipoint connector to chassis.
⇝ IN 83 ≙ Ø1H; remove connection.
Connect Pin 6C to chassis.
⇝ IN 83 ≙ Ø2H; remove connection.
Switch on general parameters 613 and 623 (frame errors).
⇝ IN 83 ≙ Ø3H and Ø7H alternately (Ø7H less often).
OUT 80.FF (terminate test program on evaluation circuit).

Test of group delay synchronization (IC 3/1, IC 28, IC 21/1):

Setting: VAR. MODE 111
VAR. MODE 211
Monitor: OUT 90.1 (dig. sig. trigger off)
OUT 40.1 (ana. sig. trigger off)
OUT 71.0 ($\overline{F1}$/F2 off)

Enable flipflop for dig. signal trigger:
OUT 81.04
OUT 80.EC
IN 80 ≙ 2 E ⇝ No interrupt yet triggered.

Generate "Dig. signal trigger" signal:
OUT 90.00
OUT 90.01
IN 80 ≙ 5 E ⇝ Interrupt triggered

Enable flipflop for analog signal trigger:
OUT 81.02
OUT 80.EC
IN 80 $\stackrel{!}{=}$ 2 E ~ No interrupt yet triggered.

Generate "Anal. signal trigger" signal:
OUT 40.00
OUT 40.01
IN 80 $\stackrel{!}{=}$ 5 E ~ Interrupt triggered

Enable flipflop for $\overline{F1}$/F2 signal:
OUT 81.01
OUT 80.EC
IN 80 $\stackrel{!}{=}$ 2 E

Generate $\overline{F1}$/F2 signal:
OUT 71.01
OUT 71.00
IN 80 $\stackrel{!}{=}$ 5 E ~ Interrupt generated

6.2.3 SIGNATURES OF THE PDG-64 [984-H]

A number of signatures are given below for a few certain instrument settings.
(See Fig. 9.2.7-6 for signature analyzer connection.)

PCM-4 settings:

Mode A 51, L = -55 dB, MAN/R, [D-D], -> START:

IC/PIN	Signature
37/3 (= 29 b)	44A5
31/3	44A5
31/9	3301
31/10	0000
23/20	2281

MA 51, L = -35 dB, MAN/R, [D-D], -> START:

IC/PIN	Signature	IC/PIN	Signature
37/3 (29 b)	4CAO	24/2	0000
31/3	4CAO	24/4	1180
31/9	3301	24/6	0000
31/10	0000	24/8	1180
23/20	2281	24/11	0000
31/1	F7UA	24/13	1180
31/4	U3H2	24/15	0000
31/5	APIU	24/17	0000
31/6	560U		
31/7	F7HP	22/11	0734
31/13	648C	22/12	U284
31/14	2725	22/13	AFA3
31/15	1180		

IC/PIN	Signature
23/3	4A7A
23/4	31H7
23/5	9874
23/6	8714
23/7	89FH
23/8	U613
23/9	PP4A
23/10	8H4C
23/21	CF4F
23/23	FA5H
23/24	0734
23/25	3214
23/26	0000
19/1	1180
19/2	6206
19/3	1180
19/4	A178
19/5	1180
19/6	4H43
19/7	0000
19/10	3214
19/11	AFA3
19/12	H032
19/13	8893
19/15	AP69

6.3 FURTHER NOTES ON TROUBLESHOOTING

The following is a description of supplementary measurements which may prove useful in troubleshooting (e.g. A-D, D-A simulation, transient response).

6.3.1 SIMULATION OF A-D/D-A MEASUREMENTS VIA CODEC

a) A-D measurements

Test set-up:

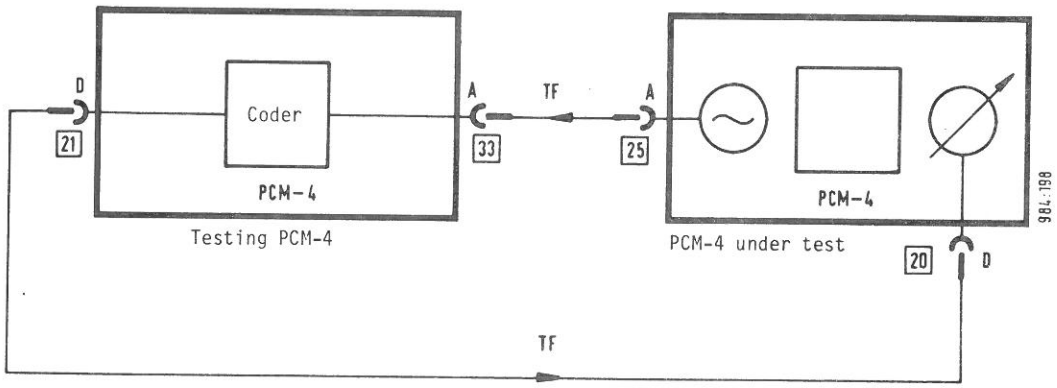


Figure 6.3-1 A-D measurement set-up with two 2 PCM-4s

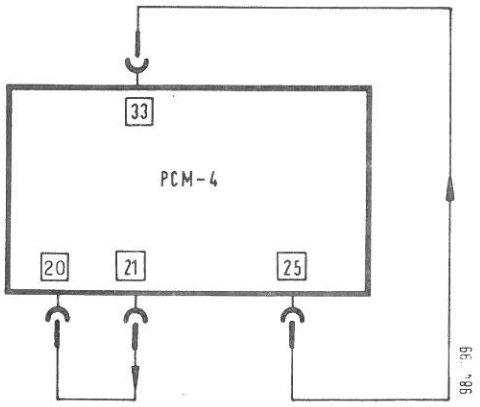
Input on PCM-4 under test:

{MA 31 / MA 41 / MA 51} E; VAR. MODE 2, ↑ , <45> E, RTN

Input on testing PCM-4:

- described below

Technical measuring notes on simulation of A-D/D-A measurements via CODEC in manual mode

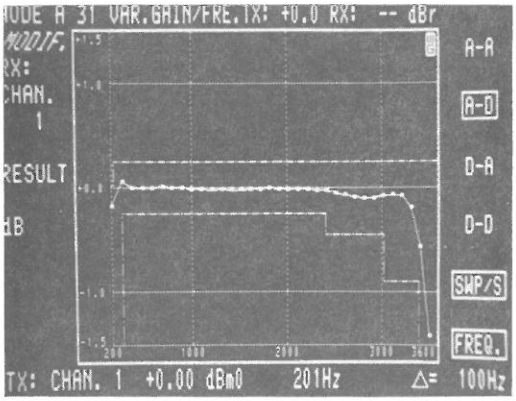


Test setup if no second PCM-4 available

Figure 6.3-2 A-D measurements with one PCM-4

Re 6.3.1 a):

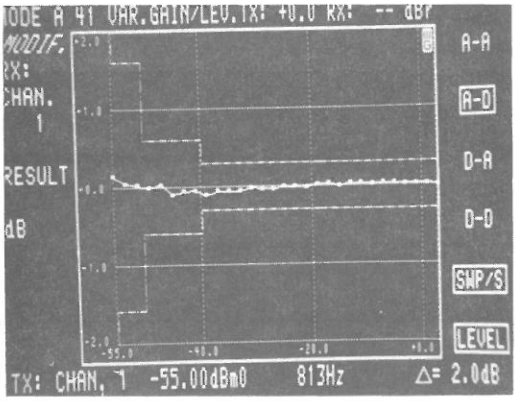
Input on PCM-4:
MODE A 31 E, [A-D], SWP/S
If measuring with a single instrument, then VAR. MODE 2, ↑, 45, E, RTN
START -> Wait for measurements until STOP, then LINK



The trace shown alongside should result. It shows the frequency response of the PCM-4-internal coder.

Figure 6.3-3 Coder frequency response

Input on PCM-4:
MODE A 41 E, [A-D], SWP/S
If measuring with a single instrument, then VAR. MODE 2, ↑, 45, E, RTN
START -> Wait for measurements until STOP, then LINK

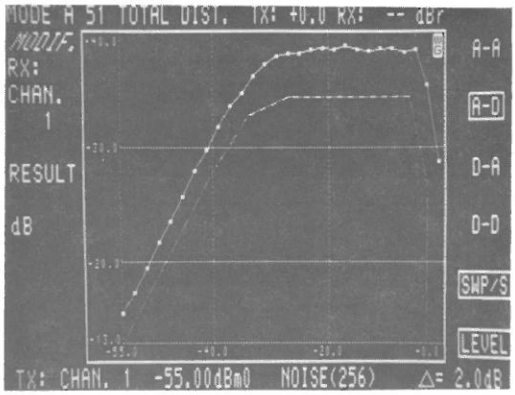


The trace shown alongside should result. It shows the level-dependent residual attenuation (linearity) of the PCM-4-internal coder.

Figure 6.3-4 Coder linearity

Re 6.3.1 a):

Input on PCM-4:
MODE A 51 E, [A-D], SWP/S
If measuring with a single instrument, then VAR. MODE 2, ↑ , 45, E, RTN
START -> Wait for measurements until STOP, then LINK

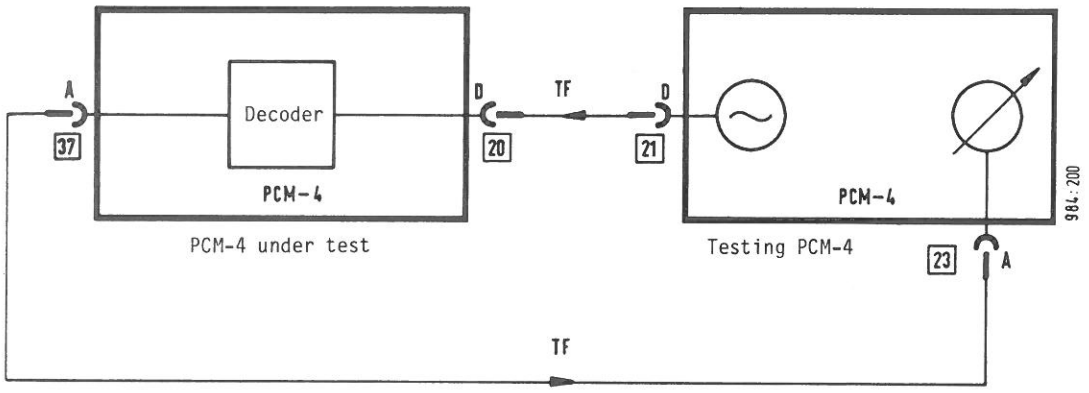


The trace shown alongside should result. It shows the natural S/Q ratio of the PCM-4-internal coder, measured with narrow-band noise.

Figure 6.3-5 Coder S/Q ratio

b) D-A measurements

Test set-up:

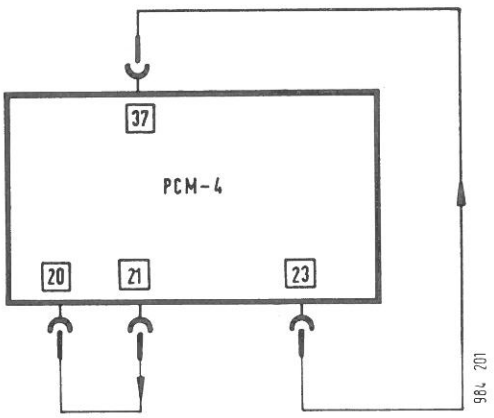


PCM-4 under test

Figure 6.3-6 D-A measurements with two PCM-4s

Input on PCM-4 under test:
Entry on testing PCM-4:
- described below.

Re 6.3.1 b):

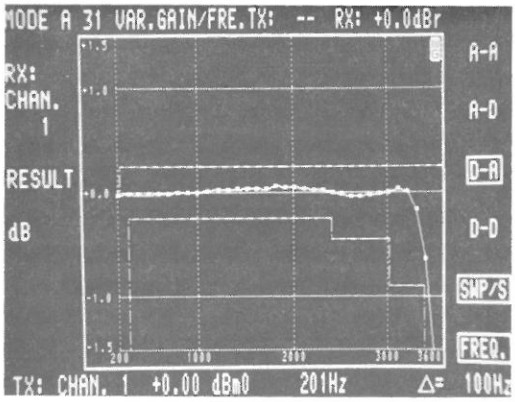


Test setup if no second PCM-4 available

Figure 6.3-7 D-A measurements with one PCM-4

Re 6.3.1 b):

Input on PCM-4:
MODE A 31 E, [D-A], SWP/S
START -> Wait for measurements until STOP, then LINK

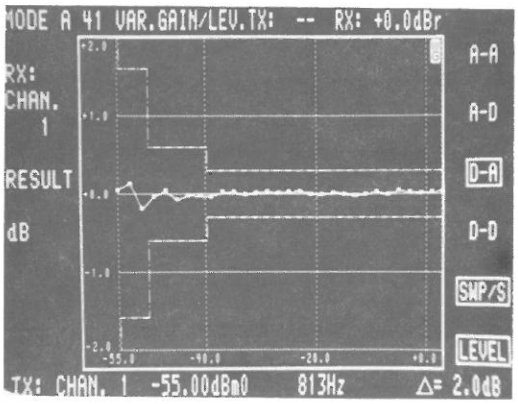


The trace shown alongside should result. It shows the frequency response of the PCM-4-internal decoder.

Figure 6.3-8 Decoder frequency response

Re 6.3.1 b):

Input on PCM-4:
MODE A 41 E, [D-A], SWP/S
START -> Wait for measurements until STOP, then LINK

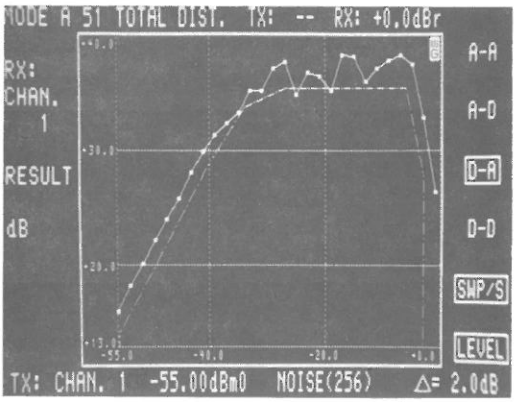


The trace shown alongside should result. It shows the level-dependent residual attenuation (linearity) of the PCM-4-internal decoder.

Figure 6.3-9 Decoder linearity

Re 6.3.1 b):

Input on PCM-4:
MODE A 51 E, [D-A], SWP/S
START -> Wait for measurements until STOP, then LINK



The trace shown alongside should result. It shows the natural S/Q ratio of the PCM-4-internal decoder, measured with narrow-band noise. Due to the nature of the circuitry, fluctuations of the S/Q ratio of up to ± 3 dB may occur in this "D-A" configuration.

Figure 6.3-10 Decoder S/Q

6.3.2 MENU INPUT VIA KEYBOARD (CONNECT GENERATOR [25] AND RECEIVER [23]

a) Input on PCM-4 (1):

MODE A 11 ENTER

The following are set automatically:

[A-A], Tx: 0.0 Rx: 0.0 dBr

[SWP/S], [FREQ], f = 201 Hz

p_a = -10 dBm0, CHAN = 01 (Rx and Tx)

[LEVEL]

Δ = 1 dB

Input:

START

The following screen display must appear after the automatic STOP:

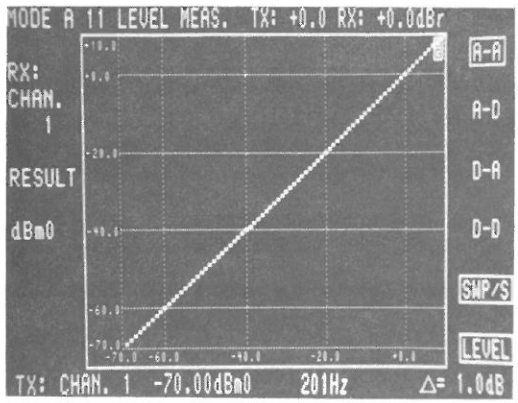


Figure 6.3-11 Level measurement

- Unsteadiness in the curve rise indicate that incorrect divider corrections were stored during the CAL. operation.
- A curve rise with level offset indicates incorrect stored basic attenuation values.

Note:

Example of the effects of

- incorrectly stored divider corrections and/or
- incorrectly stored basic attenuations

⇩

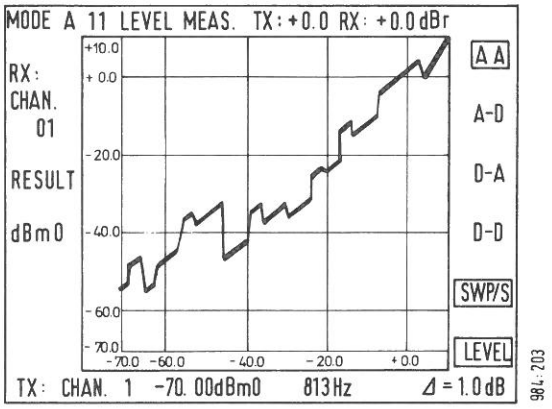


Figure 6.3-12 Faulty level measurement

The cause could be an incorrect transient response (e.g. no offset compensation, etc., incorrect timing of $\tau 1/\tau 2$, etc.). Proceed as follows to ascertain beyond doubt whether incorrect values have been stored or whether genuine wiring faults exist:

- Switch off instrument
- Switch on instrument and hold down the "9" key at the same time -> CALIBRATING is skipped, all correction and basic attenuation values are set to zero.
- Repeat the test in Section 6.3.2: Now, only the absolute divider errors (< 0.2 dB) and basic attenuations (< 0.5 dB) are effective.

b) Input on PCM-4 (2)

MODE A 41 ENTER
The following are set automatically:
[A-A], Tx: 0.0 Rx: 0.0 dBr, [SWP/S], [LEVEL], f = 813 Hz
p_a = -55 dBm0, CHAN = 01 (Rx and Tx), Δ = 2 dB
Input:
Scale Y top 0.1 dB, Y bottom -0.2 dB (ENTER), [RTN]
START
The following screen display must appear after the automatic STOP (typical profile):

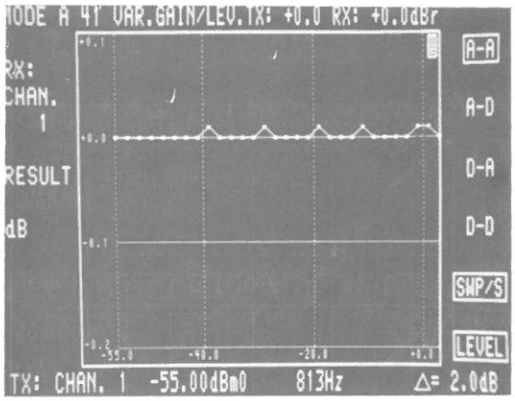


Figure 6.3-13 Gain as a function of level

- Deviations exceeding 0 $\pm$ 1 mB indicate incorrectly stored divider correction values.

c) Input on PCM-4 (3)

MODE A 31 ENTER

The following are set automatically:

[A-A], Tx: 0.0 Rx: 0.0 dBr, [SWP/S], [FREQ], f_a = 201 Hz

p = 0.0 dBm0, CHAN = 01 (Rx and Tx), Δ = 100 Hz

Input:

Scale Y top 0.1 dB, Y bottom -0.2 dB (ENTER!)

START

The following screen display must appear after the automatic STOP (similar profile):

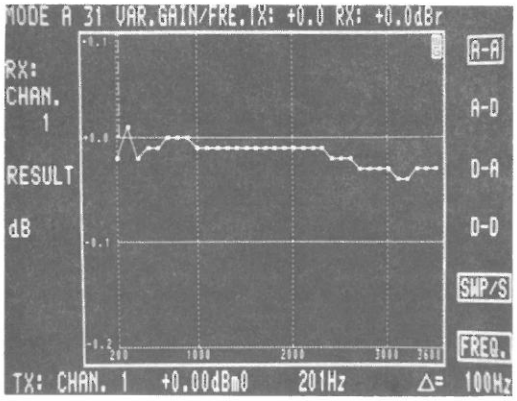


Figure 6.3-14 Gain as a function of frequency

- Deviations exceeding 0 ± 2 mB indicate faulty ripples of the two 4.5 kHz and 4 kHz low-pass filters in the analog generator or receiver.
- The low-pass filters mentioned include active and passive components.

d) Check of the transient response of the amplifiers and dividers

- [23] connected to [25], [36] terminated with 600 Ω.
- Input on PCM-4:
  MODE A 11 E, MAN/S, L = 0dB, ENTER
- Transient recorder (or storage scope): Beam A at [984-E] TP 9, Trigger A
  Beam B at termination of [36]

Settings of transient recorder TR-940:

- Turn [25] X-OFFSET to 0
- Set [26] X-MAGN. to 1; red LED [24] does not light up.

Oscilloscope settings:

- Signal input on DC coupling
- Sensitivity 0.5 V/DIV
- Time-base 0.5 ms/DIV
- Triggering on EXTERNAL
- Trigger input on DC coupling
- Positive trigger edge
- Adjust trigger level until display present

Screen calibration:

- Press key [23] "MIN" on the TR-940
- Use the vertical shift ↕ on the oscilloscope to set the calibration line to the bottom screen edge and the horizontal shift <-> to set it to full screen width.
- Press key [23] "MAX" on the TR-940
- Set the calibration line to the top screen edge on the oscilloscope
- Check the screen calibration and, if necessary, correct with the fine control for sensitivity and time-base
- Press key [1] "A" and "B"
- Press key [23] "A and B"
- Set [6] Record to "1 o'clock" position
- Press [5] [ARM] -> Ready for recording

(Press the "ARM" key again before a new recording)
Now press the "START" key on the PCM-4 ->

- 1 x start -> Display 0 +0.01 dB, -0.02 dB
- Required oscillogram:

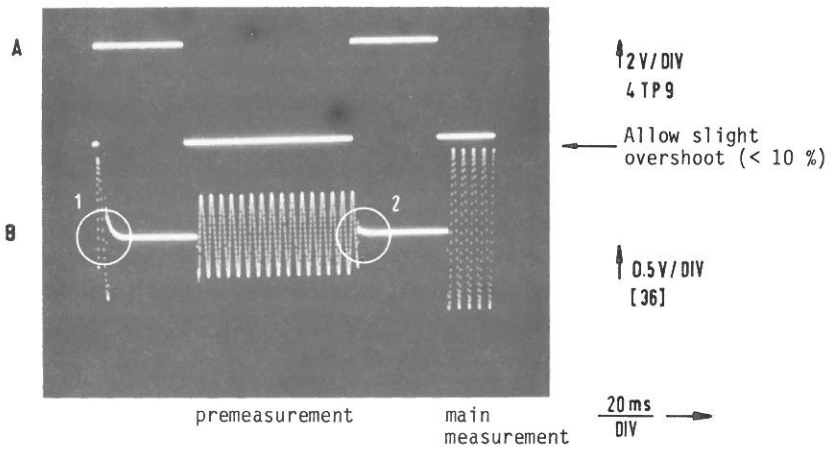


Figure 6.3-15 Transient response 1

- Disconnect [23] - [25]
- Set rec. beam B ↕ 0.2 V/DIV
- 1 x start -> Display -99.99 dB
- Required oscillogram:

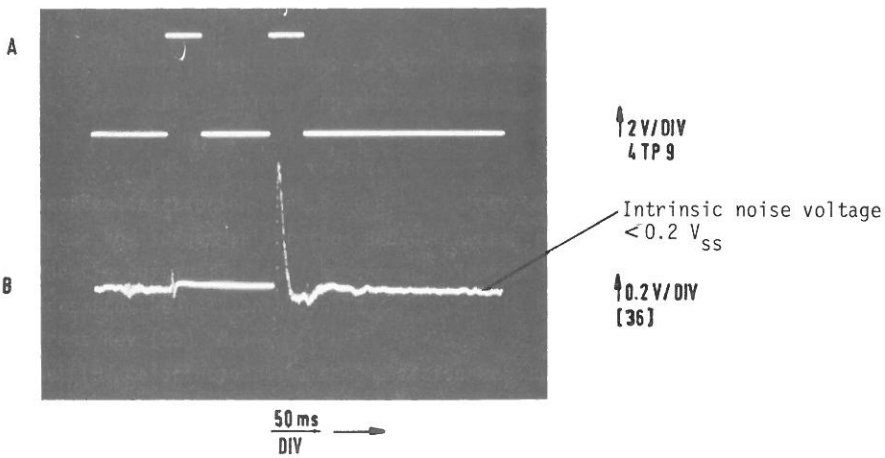


Figure 6.3-16 Transient response 2

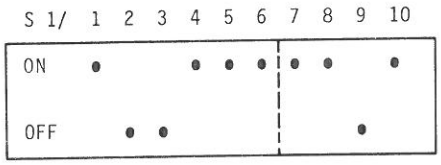
6.4 TROUBLESHOOTING ON THE SCREEN CONTROL CARD BSK-1, BN 962, CIRCUIT DIAGRAM (92)

Troubleshooting by way of signature analysis is not carried out on this card.
It should be replaced in the event of a fault.

6.4.1 EXTRA DEVICE-SPECIFIC TEST

Screen control card test

The interface between the CPU-2 card and the screen control card is tested (address bus, data bus and control lines).
Some of the basic functions of the GDP (Graphic Display Processor) are also checked, e.g. bit set/reset function of the GDP register.



cyclic BSK bus test

Figure 6.4-1 DIL switch settings for BSK test

Calling up the test:

Set DIL switch S 1 on the connected CPU-2 as shown above and switch on the instrument.

Test result:

Connect an oscilloscope to TP 2 (SOD) of the CPU card: Frequency = Ø -> faulty
Frequency ≠ Ø -> OK

6.5 TROUBLESHOOTING THE 7" MONITOR, BN 980

Refer to the circuitry description in Section 9 and the pulse diagrams in the appendix (monitor circuit diagram when troubleshooting the monitor card.

As the CRTs used conform to IEC, DIN and VDE safety requirements, there is no risk of implosion of the CRT is used and handled correctly.

Be careful not to

- knock the CRT sharply or drop it - expose the CRT to extremes of heat and cold
- scratch the CRT
- damage or remove the metal frames, as this provides extra protection against implosion.

The CRT cannot be adjusted until after it has been fitted in the instrument.
Each time the monitor card, deflector unit or CRT is replaced, the complete unit must be readjusted.

6.6 TROUBLESHOOTING THE IEEE 488/<IEC 625> INTERFACE BUS CARD BN 958, CIRCUIT DIAGRAM (91)

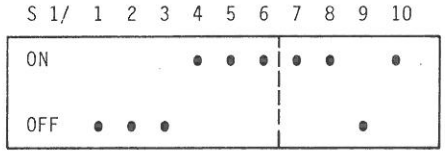
6.6.1 INTRODUCTION

The bus interface BN 958 is used to adapt microprocessor-controlled instruments to the IEEE 488 or <IEC 625> interface bus.
For the purposes of this test, it is assumed that the device is operating correctly as regards the program sequence and control of the device- to IEC-625-interface.
Since the card cannot be tested completely when fitted in the instrument, it is advisable to replace it in the event of a fault.

6.6.2 EXTRA DEVICE-SPECIFIC TEST

IEC bus interface card test

The signal path (address bus, data bus, control bus) to the IEC bus module is checked in relation to the gate address.
The bus interface card is optional. It is not possible to use a software routine to check whether it is fitted or not should the instrument not respond to IEC bus commands, since no signal line is provided for this purpose.



cyclic IEC bus test

Figure 6.6-1 DIL switch settings for IEC bus test

Calling up the test:

Set DIL switch S 1 on the connected CPU-2 (2A) as shown above and switch on the instrument.

Test result:

Connect an oscilloscope to TP 2 (SOD) of the CPU card:

Frequency = Ø -> Faulty
Frequency ≠ Ø -> OK

7 ALIGNMENT INSTRUCTIONS

This Section describes the alignment operations and the corresponding test setups.
The location of the invididual alignment elements can be seen either on the fold-out photographs in Section 10 or from the component layout drawings in the Appendix (see Figs. 10.7-1, 10.7-2, 10.7-3).

7.1 ALIGNMENT OPERATIONS IN THE ANALOG SECTION

Analog receiver section

Circuit diagram; circuit board or assembly	Alignment element	Comments	Section in the alignment instructions	Alignment after circuit board or assembly replacement
(2) Preselector stage and controller [984-AE1]	C 2	Transformer balance	7.3.1	x
	C 3	Frequency response, input attenuator	7.3.2	
	C 6	Frequency response, input attenuator		x
[984-BC]	P 100	Offset setting, controller	7.3.3	x
(3) Switch panel [984-AF]	P 1	Common mode, balanced amplifier	7.3.4	
	P 2	Offset, unbalanced amplifier	7.3.5	
(4) Input 1 [984-E]	P 1	Signal separation	7.3.6	
	P 2	Offset controller	7.3.7	
	P 3	Buffer amplifier	7.3.8	
(17) ADC-1 [984-K] [984-K1]	P 2	A-D converter	7.3.14	
	P 3	Voltage controller, +18 V	7.3.15	
	P 4	Voltage controller, -18 V		
	P 5	RMS rectifier offset	7.3.14a	
	P 11	Sample & hold offset	7.3.14b	
(17) ADC-2 [984-AR]	P 3	Voltage controller, +18 V	7.3.15	
	P 4	Voltage controller, -18 V		
(18) Analog filter [984-J] [984-J1]	P 1	Pole alignment, 4 kHz LP	7.3.16	
	P 2	Pole alignment, 4 kHz LP		
	P 3	Pole alignment, 4 kHz LP		

Figure 7.1-1 List of all alignment elements

Circuit diagram; circuit board or assembly	Alignment element	Comments	Section in the alignment instructions	Alignment after circuit board or assembly replacement
	P 4	Offset ...	7.3.17	
	L 1	Pole alignment, 4.6 kHz HP	7.3.18	
	L 2	Pole alignment, 4.6 kHz HP		
	L 3	Pole alignment, 4.6 kHz HP		
	L 4	Pole alignment, 4.6 kHz HP		
	L 5	Pole alignment, 130 kHz LP	7.3.19	
	L 6	Pole alignment, 130 kHz LP		
(21) Evaluation circuit [984-M]	C 1	Clock generator	7.3.25	
(1) Data protection [959-AV]	P 21	Threshold setting	7.3.21	x
(92) Screen control card [962-A]	P 1	Brightness	7.3.22	x
(93) 7" monitor [980-A]	P 1	Frame height	7.3.23	x
	P 2,	Vertical frequency	7.3.24a	
	P 4,	Horizontal frequency	7.3.24b	
	P 5	Background brightness	7.3.22	x
	P 6	Focus		
	P 7	Brightness		
	L 5	Frame width	7.3.24	x
	S 2			
	C 48	Compensation, complete test screen video signal	7.3.24c	
	C 49	Compensation, monitor test signal video signal	7.3.24d	

Figure 7.1-1 List of all alignment elements (contd.)

Analog generator section

Circuit diagram; circuit board or assembly	Alignment element	Comments	Section in the alignment instructions	Alignment after circuit board or assembly replacement
(10) Analog generator [984-X, X1]	P 1	Offset, buffer amplifier 7 75 kHz LP	7.3.9	
	P 8	Offset, buffer amplifier 4.5 kHz LP/1.76 kHz LP		
	L 5	Pole alignment, 75 kHz LP	7.3.10	
	L 6	Pole alignment, 75 kHz LP		
	L 7	Pole alignment, 75 kHz LP		
	S 1	Basic calibration	7.3.11	x
(11) Output stage [984-AA]	P 11	Frequency response Transformer	7.3.13	
	P 12	Offset, buffer amplifier	7.3.12	
	P 13	Offset, bal. amplifier		
	P 14	Offset, bal. amplifier		
(1) Power supply unit C 15 A	R 217	+5V/10A supply rail	7.3.26-1	x
	R 225	Current limiting		
	R 309	+12V/1.1A supply rail	7.3.26-2	x
	R 319	+15V/0.8A supply rail	7.3.26-3	x
	R 322	-15V/0.8A supply rail	7.3.26-4	x
	R 325	+18V/0.15A supply rail	7.3.26-5	x
	R 328	-18V/0.15A supply rail	7.3.26-6	x
	R 303	+15V/0.45A supply rail	7.3.26-7	x
	R 305	-15V/0.45A supply rail	7.3.26-8	x

Figure 7.1-1 List of all alignment elements (contd.)

Alignment operations in the digital section

Circuit diagram; circuit board or assembly	Alignment element	Comments	Section in the alignment instructions	Alignment after circuit board or assembly replacement
(14) PCM-30 input [984-R]	P 1 P 2 P 3 P 4	Offset, input amplifier Offset, peak-resp. rectifier Offset, phase-inv. amplifier Threshold setting "NO SIGNAL"	7.4.3.1 7.4.3.2 7.4.3.3	
(16) PCM-30 output [984-S]	P 1 P 2	Voltage controller $-U_{ref}$ Voltage controller $+U_{ref}$	7.4.2	
(25) Clock circuit [984-V]	P 1 P 2 Series A + B: C 31 Series C ...: P 3 C 104	Active time, monoflop Active time, monoflop Oscillator frequency Free-running freq., PCC	7.4.1.1 7.4.1.2 7.4.1.3 7.4.1.3	
(22) PDG-64 [984-H]	P 1	Analog encoder	7.4.4.1	
(27) Coupling card 2 [984-AD]	C 23	Oscillator circuit	7.3.20	

Figure 7.1-1 List of all alignment instructions (contd.)

7.2 LOCATION OF TEST AND MEASURING POINTS

Assembly	Test and measuring point designation	Brief description, comments
(1) Data protection [959-AV]	TP 1 TP 2 TP 3 TP 4 TP 5 TP 6	Battery voltage Ground +12 V +5 V High-end voltage, 5 ... 25 V Mains OFF signal
(2) Presel. stage [984-AE1] [984-BC]	TP 1 TP 2 TP 3	Input attenuator output Input amplifier output Ground
(4) Input 1 [984-E]	TP 1 TP 2 TP 3 TP 4 TP 5 TP 6 TP 7 TP 8 TP 9 TP 10 TP 11 TP 12 Bridge C - D	Input signal Reference attenuator input Intermediate attenuator 2 input Intermediate amplifier 1 output Intermediate amplifier 2 output Output amplifier output Ground "Overloaded" signal τ2 signal (signal identification) τ1 signal (offset correction) "Signal identification" Intermediate attenuator 1 input
(10) Analog generator [984-X,X1]	TP 0 TP 1 TP 2 TP 3 TP 4 TP 5 TP 6 TP 7 TP 9 TP 11 TP 12	Ground 8 kHz ext. clock Addressing unit "Enter" Addressing unit "Clock Out" Addressing unit "Reset Out" 200 kHz clock (Clock 1) 20 kHz clock (Clock 2) Oscillator output (8.026 MHz) Test point for signature analysis SA 3 Test point for signature analysis SA 2 Test point for signature analysis SA 1

Figure 7.2-1 Location of test and measuring points

Assembly	Test and measuring point designation	Brief description, comments
	TP 14	CE signal for addressing unit
	TP 15	$\overline{\text{WSEN}}$ (Write Select Enable) for decoder circuit
	TP 16	D/A converter 1 output (signal 1)
	TP 17	SA 4
	TP 18	SA 5
	TP 19	Reference signal U_{Ref} = -10 V
	TP 20	$\overline{\text{RSEN}}$ (Enable signal for polling the offset switches)
	TP 21	Ground
	TP 22	Auxiliary signal (H signal)
	TP 8	Test signal, addressing unit "Zero"
	TP 10	Test signal, addressing unit "Overflow"
	TP 13	Test signal, addressing unit "Enter Acknowledge"
(10) Analog generator [984-Y]	TP 30	Ground
	TP 31	Calib. 1 signal (unattenuated)
	TP 32	Calib. 1 signal (attenuation -24 dB)
	TP 33	H signal (bal. transformer input)
	TP 34	75 kHz LP filter output
	TP 35	4.5 kHz LP filter output
	TP 36	1.76 kHz LP filter output
	TP 37	Attenuator circuit input
	TP 38	Signal 2 output
	TP 40	Voltage supply, +15 V
	TP 41	Voltage supply, +5.6 V
	TP 42	Voltage supply, -5.6 V
	TP 43	Voltage supply, -15 V
	Bridge [A-B]-C	H signal (bal.) -> AUX signal
	A-[B-C]	Signal 1 (bal.) -> AUX signal
	Bridge [D-E]-F	H signal (bal.) -> AUX signal
	[E-F]	Signal 1 (bal.) -> AUX signal
(11) Output stage [984-AA] [984-AB]	TP 1	Frequency reponse compensation output
	TP 2	Bal. amplifier output } for offset alignment
	TP 3	Bal. amplifier output } for offset alignment
	TP 4	Alarm signal "OVERLOADED"
		Pulse length at least 75 ms

Figure 7.2-1 Location of test and measuring points (contd.)

Assembly	Test and measuring point designation	Brief description, comments
(12) Signalling distortion [984-N]	TP 1 TP 2 TP 3 TP 4 TP 5 TP 6 TP 7	Dialling bit Output transistor base Window comparator input Window comparator output 1 Window comparator output 2 Z monitor Received dialling signal
(14) PCM-30 input [984-R]	TP 1 TP 2 TP 3 TP 4 TP 5	Input signal Ground Output of input-amplifier PCM^+ switching threshold PCM^- switching threshold
(17) ADC-1 [984-K]	TP 1 TP 2 TP 3 TP 5 TP 6 TP 7 TP 8 TP 9 TP 10	Out-of-band input signal Input amplifier stage V = 12.02 dB Rectifier output Sample & Hold (offset compensation) Control voltage [-5 V ... +5 V] Sample trigger ADC status +15 V voltage supply -15 V voltage supply Ground
(18) Analog filter [984-J]	TP 1 TP 2	In-band signal Ground
(26) Coupling card 1 [984-G]	TP 1 TP 2 TP 3 TP 4 TP 5 TP 6 TP 8	SHOLD -> DMA request to display circuit SHOLDA -> DMA acknowledgement of display circuit RST 7.5 for display circuit MHOLD -> DMA request to measuring circuit MHOLDA -> DMA acknowledgement of measuring circuit RST 7.5 for measuring circuit "Memory disable" signal to display circuit

Figure 7.2-1 Location of test and measuring points (contd.)

Assembly	Test and measuring point designation	Brief description, comments
(26) Coupling card 1 [984-G]	TP 9 TP 10 TP 11 TP 12 TP 13	$\overline{CE}$ signal for ROM I (ØØØØH-3FFFH) $\overline{CE}$ signal for ROM II (4ØØØH-7FFFH) $\overline{CE}$ signal for ROM III (8ØØØH-BFFFH) $\overline{CS}$ signal RAM 0 (EØØØH-FFFFH) Ground
(27) Coupling card 2 [984-AD]	TP 1 TP 2 TP 3 TP 4 TP 5 TP 6 TP 7 TP 8 TP 9	RST 6.5 to master computer RST 5.5 to master computer Ground Clock 32.76800 kHz $\pm$ 0.0002 kHz Ground MSOD $\cong$ "Finished" message of measuring circuit SSOD $\cong$ "Finished" message of display circuit MES END $\cong$ "End of measurement" signal of meas. circ. TAS INT $\cong$ Keyboard interrupt signal
(35) Coupling card 3 [984-AT]	TP 1 TP 2 TP 3	MRST 6.5 $\cong$ RST 6.5 of measuring circuit MRST 5.5 $\cong$ RST 5.5 of measuring circuit Ground

Figure 7.2-1 Location of test and measuring points (contd.)

7.3 DESCRIPTION OF ALIGNMENT OPERATIONS

7.3.1 2 C 2

This alignment should only be carried out by the factory. In exceptional cases, e.g. after replacing input transformer 2 0 1, proceed as follows:

Up to Series D: Remove the input section (see Section 3.3.3)

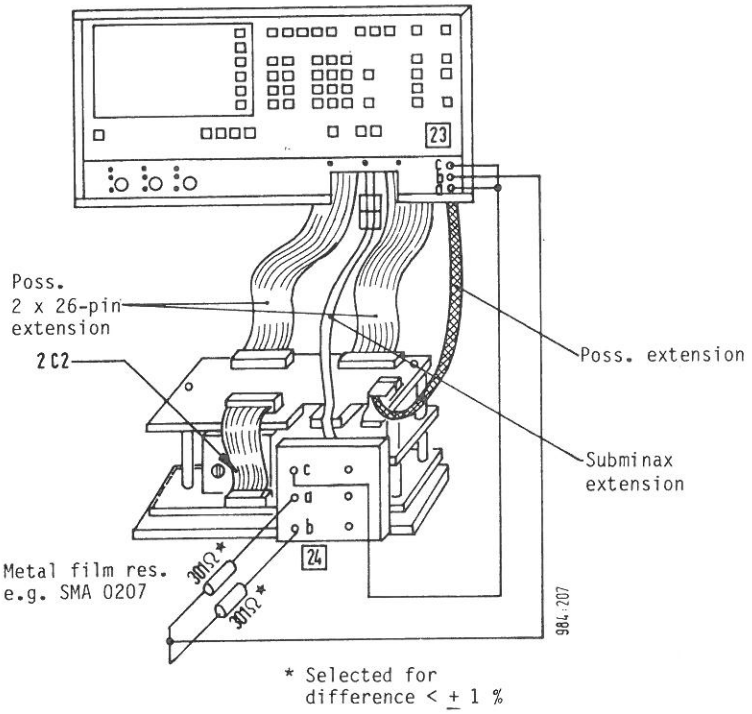


Figure 7.3.1-1 Location of 2 C 2

From Series E: The input section need no longer be removed (see Fig. 10.7-2).

Entry on PCM-4:
MODE A 13, ENTER, MAN/R, L = 0 dBm0 ENTER, F = 72 kHz ENTER, START.
Use 2 C 2 to align to minimum display.

7.3.2 2 C 3, C 6

Measuring instrument alignment : First record the frequency response of level generator and level meter.

Test setup : Connect the level generator to socket 23, the level meter to preselector stage [984-AE] TP 2, TP 3 (ground).

Entry on PCM-4 :
- MA 11 E
- VAR MODE
- Hold down the uppermost softkey for several seconds
  -> Monitor picture appears
- Select CPU 2/3 (DIGIT WORD key)
- OUT 52.01 E

Alignment :
- Measure the frequency response at the following frequencies:
  4 kHz, 10 kHz, 40 kHz, 50 kHz ... 130 kHz
- Tolerance ± 5 mB
- Align with C 6*

Entry on PCM-4 : OUT 52.00 E

Alignment :
- Measure the frequency response with the above frequencies and, if necesary, align with C 3*.

* Up to Series D:
C 6 and C 3 are accessible after carefully folding up the switch panel.

7.3.3 2 P 100

Test setup :
- Input 23 open
- Fit Input 1 card [984-E] on adapter [35-984]
- Connect oscilloscope to 23 b, 23 c [Ground]

Entry on PCM-4 :
- MA 11 E
- MAN/S
- START

Alignment :
- Align the required value of 0 V ± 5 mV with 2 P 100. Press "START" several times to do so.

Note: As the input stage has a very low cut-off frequency (< 0.1 Hz), a very-low-frequency noise voltage is superimposed on the offset voltage; it is later eliminated by a high-pass filter in the instrument. This noise voltage must be taken into account when taking readings from the oscilloscope.

7.3.4 3 P 1

Test setup : - Remove the (optional) measuring bridge
- Fit the adapter card
- Connect an ext. level generator (e.g. PS-19) to 16 a/16 c and 16 b [Ground]
- Frequency on level generator 15.6 kHz
- Level 0 dB
- Connect an ext. level meter (e.g. SPM-19) to socket [36] (VF/NF)
- Socket [23] (receiver analog input) open

Entry on PCM-4: - MA 11 E
- MAN/S, [A-A]
- START
- VAR MODE
- Hold down the uppermost softkey for several seconds
  -> The monitor picture appears
- Select CPU 2/3
- OUT 55.40 E

Alignment : - Use 3 P 1 to align common mode to minimum

7.3.5 3 P 2

Aux. equipment: - Socket for miniature coaxial cable
- S 830 (with Versacon insert)

Test setup : - Remove the (optional) measuring bridge
- Fit the adapter card in place of the measuring bridge
- Connect input signal Pins 16 a/16 c to 16 b [Ground]
- Unscrew the calibration cable at output stage connection ([984-W]) and connect to the socket (aux. equipment)
- Connect a DVM to the socket

Entry on PCM-4: - Switch on the instrument, pressing the "0" key at the same time
  -> The monitor picture appears
- Select CPU 2/3
- OUT 55.CØ E

Alignment : - Use 3 P 2 to align the offset to 0 V $\pm$ 2 mV

7.3.6 4 P 1

Test setup : - Connect socket [23] - socket [25] (PCM-4)
- Transient recorder
  or storage scope: beam A at 4 TP 9 ([984-E]) (T2)
  beam B at 4 TP 2 ([984-E9] (signal)
  Trigger on A; A = 2 V/DIV
  B = 50 mV/DIV
  Time-base on 10 ms/DIV

Settings : Transient recorder TR-940:
- Turn [25] X-OFFSET to 0
- Set [26] X-MAGN. to 1; red LED [24] does not light up

Settings : Oscilloscope:
- Signal input on DC coupling
- Sensitivity 0.5 V/DIV
- Time-base 0.5 ms/DIV
- Triggering on EXTERNAL
- Trigger input on DC coupling
- Positive trigger edge
- Adjust trigger level until picture appears

Screen calibration:
- Press key [23] "MIN" on the TR-940
- Use the vertical shift ↕ on the oscilloscope to set the calibration line to the bottom screen edge and the horizontal shift <-> to set it to full screen width.
- Press key [23] "MAX" on the TR-940
- Set the calibration line to the top screen edge on the oscilloscope.
- Check the screen calibration and, if necessary, correct it with the fine controller for sensitivity and time-base.
- Press key [2] "A" and "B"
- Press key [23] "A & B"
- Set [6] Record to 2 o'clock position
- Press key [5] "ARM" -> Ready to record

Entry on PCM-4: - MA 11 E
- Level 0 dB E
- MAN/S
- START -> Measuring result 0 $\pm$ 0.05 dB

Figure 7.3.6-1 appears. Before pressing "START" again, always press the "ARM" key on the TR-940.

Alignment : - The negative edge of "A" should appear on the oscillogram at least 3 ms before activation of signal "B".
- Use 4 P 1 to align to 5 ms (see Fig. 7.3.6-1)

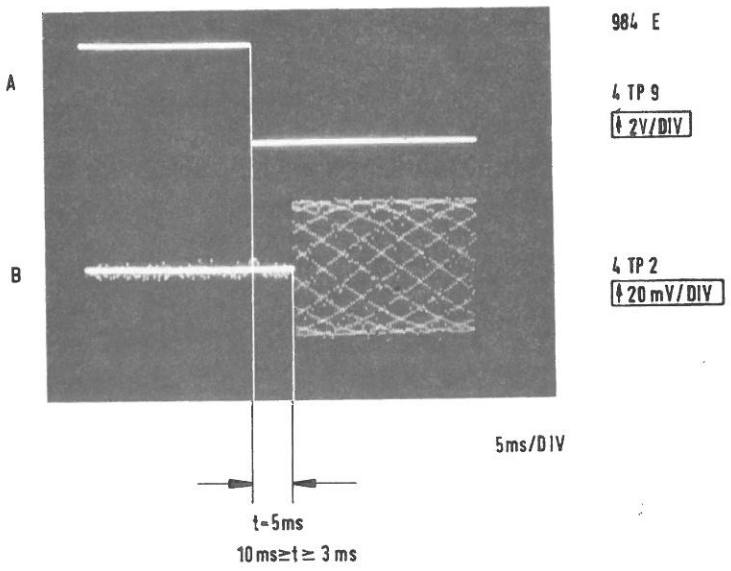


Figure 7.3.6-1 Alignment of 4 P 1 (signal separation)

7.3.7 4 P 2

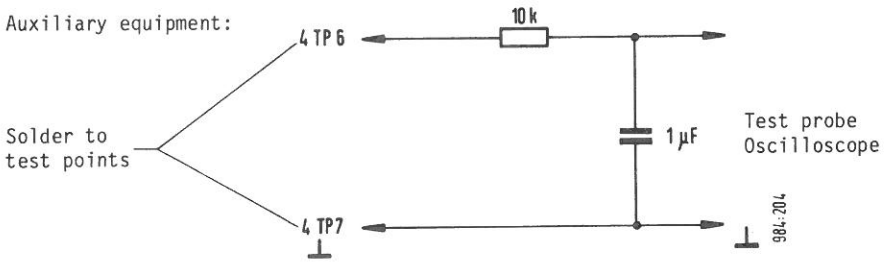


Figure 7.3.7-1 Alignment of 4 P 2 (offset controller)

Test setup : - Socket [23] (analog input) open
- Connect the oscilloscope to TP 6, TP 7 [Ground] (between oscilloscope and 4 TP 6 LP), as shown above.

Alignment : - Measure the offset voltage and correct with 4 P 2, if necessary (required value 0 V $\pm$ 100 mV, see Fig. 7.3.7-2).

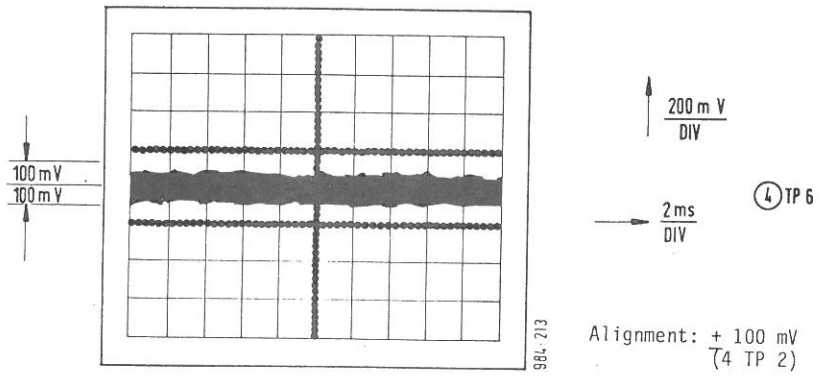


Figure 7.3.7-2 Offset voltage measurement

7.3.8 4 P 3

Auxiliary equipment: - Adapter card 901/00.11 or modified adapter card 901/00.13:

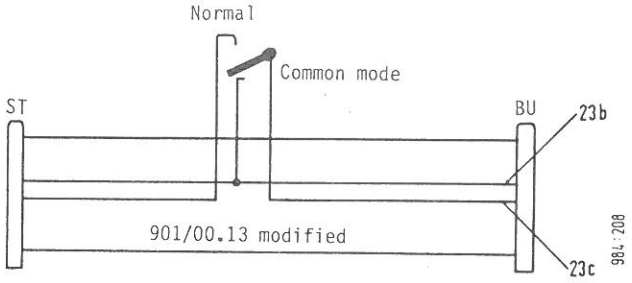


Figure 7.3.8-1 Alignment of 4 P 3 (buffer amplifier)

With adapter card 901/00.11: - Fit card "Input 1" [984-E] on adapter card. All bridges fitted
(≅ "normal")
- Switch on instrument

1. PCM-4 self-test
   - Connect socket [25] to socket [23]

Entry on PCM-4: - MA 13 E
- [A-A]
- MAN/R
- Level 0 dB E
- Frequency 15.6 kHz E
- VAR MODE 521 - 120 E
- RTN
- CHAN (channel measurement)
- X upper value 3 E
- Y lower value -99 E
- RTN
- START

Set "common mode" as follows:

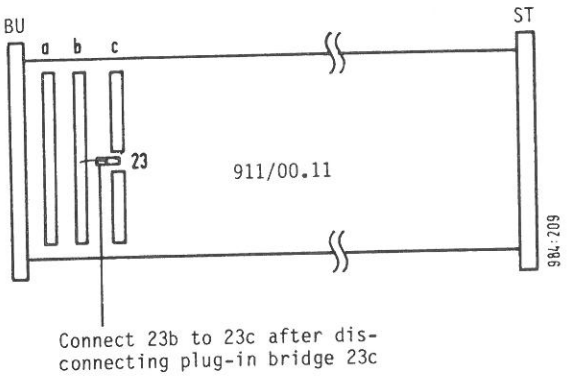


Figure 7.3.8-2 Common mode setting

2. Alignment with external measuring instruments

Test setup : - Connect ext. level generator (e.g. PS-19) to socket [23]
- Connect ext. level meter (e.g. SPM-19) to socket [36] (NF/VF)

Entry on PCM-4: - MA 13 E
- [A-A]
- MAN/S
- Level = Level of external generator (recommended: -24 dB)
- Frequency 15.6 kHz E
- START

Alignment : - (Adapter card switched to common mode)
- Use 4 P 3 to set to minimum

7.3.9 10 P 1, P 8

Test setup: - Remove analog generator 1

Alignment : - Switch on instrument (error page appears)
- Connect the DVM to TP 34 (analog generator 2)
- Use 10 P 1 to align to 0 V ± 1 mV
- Connect the DVM to TP 37 (analog generator 2)
- Use 10 P 8 to align to 0 V ± 1 mV

7.3.10 10 L 5, L 6, L 7

Alignment of the 75 kHz LP filter is only necessary after repairing the filter.

Test setup : - Remove analog generator 1
- Fit analog generator 2 in the upper slot
- Fit adapter card in the lower slot
- Connect the ext. level generator to the adapter card (Pin 4 a/5 a)
- Resolder or refit bridge A-B to C-B
- Resolder or refit bridge D-E to F-E
- Connect the selective level meter to socket [30]
- Switch on the instrument (error page appears)

Pole alignment: - At f = 119 kHz, use 10 L 6 to align low-pass filter to maximum attenuation
- At f = 142.25 kHz, use 10 L 7 to align low-pass filter to maximum attenuation
- At f = 242.5 kHz, use 10 L 5 to align low-pass filter to maximum attenuation
- Solder or fit bridges back in original positions

7.3.11 10 S 1

Test setup:

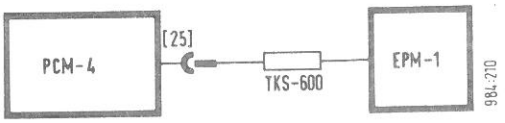


Figure 7.3.11-1 Alignment of 10 S 1 (basic calibration)

Switch assignments of DIP switch S 1 on analog generator 1

1 = LSB; 6 = MSB "6" OFF -> ON = ΔP 6 ≈ +14 mB
"5" OFF -> ON = ΔP 5 ≈ +7 mB
"4" OFF -> ON = ΔP 4 ≈ +3.5 mB
"3" OFF -> ON = ΔP 3 ≈ +1.5 mB
"2" OFF -> ON = ΔP 2 ≈ +0.7 mB
"1" OFF -> ON = ΔP 1 ≈ +0.4 mB

Entry on PCM-4: - Generator output impedance 600 Ω
- MA 11 E
- Frequency 813 Hz E
- Level 0.0 dBm0 E
- GEN PAR 936 00.01 E; set repeat calibration cycle to 1 minute

Alignment : In each calibration cycle, the calibration generator adopts the switch data and sets the calibration level accordingly. The individual switch settings cause a relative calibration level correction of the original level. The switch settings must be corrected repeatedly until the output voltage at socket [25], measured with the EPM-1, is 0 dBm0 ± 0.5 mB.

Entry on PCM-4: - GEN PAR 935 E; TIMER off

7.3.12 11 P 12, P 13, P 14

Aux. equipment: Adapter cable
(20-pin ribbon cable with plug and socket, length approx. 40 cm [984-102])

Test setup : - Remove the output stage and connect via the adapter cable (see Section 3.3.5)

Entry on PCM-4: - MA 11 E or MA 83 (-> Generator off)
- [A-A]
- Level = < -30 dB E; switch relays 1 and 7 to the output stage and output stage connection.

Alignment : - Connect the DVM to TP 1 and floating ground (contact spring)
- Use P 12 to align the offset to 0 V ± 0.5 mV
- Connect the DVM to TP 2 and floating ground (contact spring)
- Use P 13 to align the offset to 0 V ± 0.5 mV
- Connect the DVM to TP 3 and floating ground (contact spring)
- Use P 14 to align the offset to 0 V ± 0.5 mV

7.3.13 11 P 11

Aux. equipment: See test setup for alignment of 11 P 12, P 13, P 14

Test setup : - Connect the output stage to the adapter cable
- Connect a selective level meter (e.g. SPM-19) to socket [25]

Entry on PCM-4: - MA 13 E
- Level = < -30 dBm0; switch relays 1 and 7 to the output stage and output stage connection
- Set a frequency from 20 Hz to 72 kHz in appropriate steps (frequency response alignment)

Alignment : - Use the selective level meter to check the output level at the individual frequencies and correct with 11 P 11, if necessary
(Tolerance at f = 50 kHz -> -10 mB (align))
(Tolerance at f = 72 kHz -> +10 mB (check))

7.3.14 17 P 2

(ADC-1 card only)

Alignment is necessary after replacing ADC module HS9516 on ADC-1 card [984-K]

Test setup : - Connect a counter (with Time-Gate input) to TP 7, TP 10 [Ground]

Entry on PCM-4: - MA 11 E
- MAN/R
- START

Alignment : - Use P 2 to set the counter display to 70 µs ± 0.1 µs (see Fig. 7.3.14-1)
If setting is impossible, change alignment resistors R 25/R 26 -> Table

Alignment resistors (Ω) Conversion time tsc

R 25	R 26	
232	1100	↑ Smaller
511*	825	
866	464	
1240	100	↓ Greater

* Preferred values

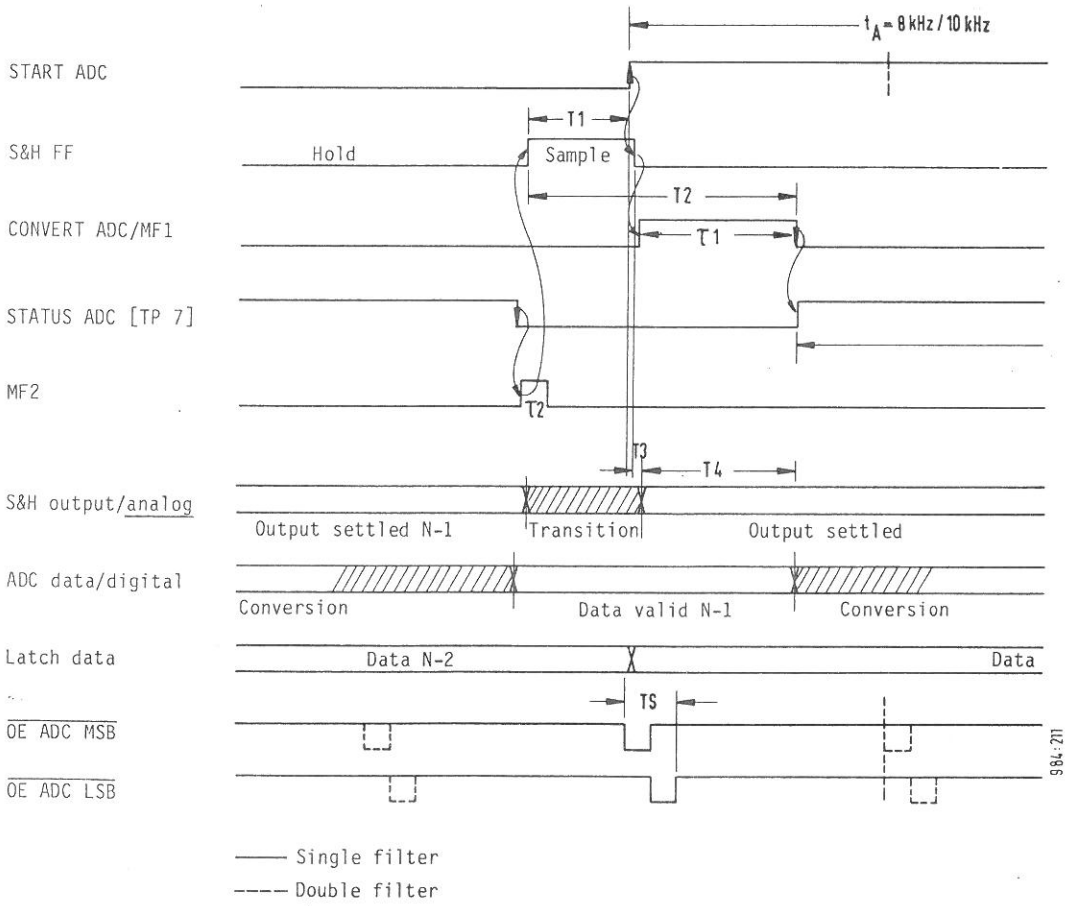


Figure 7.3.14-1 ADC-1 timing

7.3.14a RMS rectifier offset 17 P 5

PCM-4 settings:
- connect analog receiver Bu [23] to analog generator Bu [25]
- set MODE 82 E
- MAN/R
- frequency = 10 kHz

Adjustment:
- Make a reference measurement with TX level = 0 dBm; note the result.
- Increase the TX level to +4 dBm, run measurement and note the result.
- Reduce the TX level to -4 dBm, run measurement and note the result.
- Adjust 17 P 5 such that the difference between the reference value and the increased/decreased level results is not more than ± 5 mB.
  Difference = measured TX level - TX level - reference level
  e.g.: Reference level = +0.02 dB
  Measured TX level (-4 dBm) = -3.98 dB
  Difference = (-3.98 dB) - (-4 dB) - 0.02 dB = 0 mB
- After making the adjustment, repeat measurement procedure and check adjustment.

7.3.14b Sample & hold offset 17 P 11

Aux. equipment
- Digital voltmeter

PCM-4 settings:
- Leave analog receiver input Bu [23] open circuit
- Press and hold down key /9/ and at the same time switch on the PCM-4. When the BEEP sounds, release the /9/ key (indicates calibration not carried out)
- Allow the PCM-4 to warm up for about 3 minutes

Adjustment:
- Adjust the offset at the output of the S&H circuit (17 IC 32 pin 8) to 0.00 mV using 17 P 11.
- Switch the PCM-4 off and then on again.
- Check the offset is still 0 mV; if not, repeat the adjustment.

7.3.15 17 P 3, P 4

Test setup : - Connect the DVM to TP 8, TP 10 [Ground]
- Use P 3 to align to +15 V ± 0.1 V
- Connect the DVM to TP 9, TP 10 [Ground]
- Use P 4 to align to -15 V ± 0.1 V

7.3.16 18 P 1, P 2, P 3

This alignment is necessary only after repairs to the 4 kHz LP filter.

Test setup:

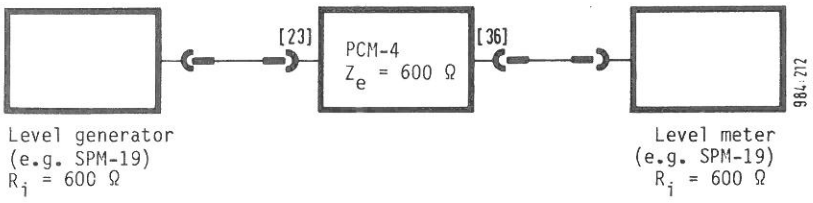


Figure 7.3.16-1 Test setup

Entry on PCM-4: - MA 11 E
- MAN/S and [A-A]
- VAR MODE 511 E RTN
- Level -24 dBm0 E (same setting as for ext. level generator)
- Input impedance 600 Ω
- START

Pole alignment: At f = 5.073 kHz, use P 2 to set maximum attenuation
At f = 5.836 kHz, use P 3 to set maximum attenuation
At f = 8.998 kHz, use P 1 to set maximum attenuation

7.3.17 18 P 4

Test setup : - Connect the oscilloscope to socket [36] (NF/VF)
- No input signal at socket [23] (analog input)

Entry on PCM-4: - MA 11 E
- [A-A]
- MAN/S
- START

Alignment : - Align the offset with 18 P 4. Required value 0 V ± -140 mV.
- When measuring on 18 TP 1, 18 TP 2, a required value of ± 50 mV is prescribed (see Fig. 7.3.17-1).

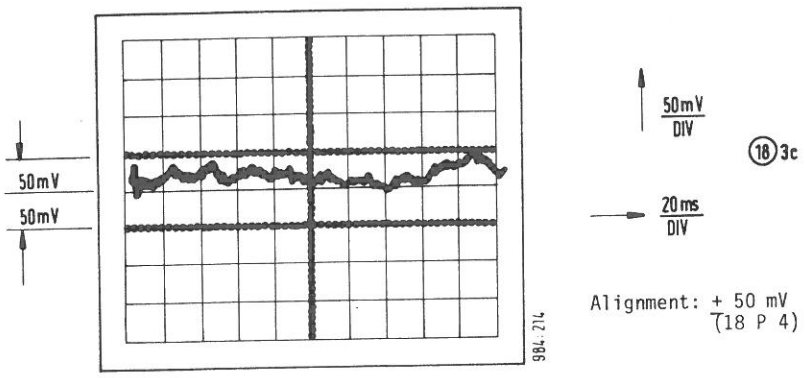


Figure 7.3.17-1 Measurement on 18 TP 1, 18 TP 2

7.3.18 18 L 1, L 2, L 3, L 4

This alignment is only necessary after repairing the 4.6 kHz LP filter

Test setup : - Same setup as for alignment of 18 P 1, P 2, P 3

Entry on PCM-4: - MA 82 E
- MAN/S, [A-A]
- VAR MODE 511 E RTN
- Level -42 dB (same setting as for ext. level generator)
- Ze = 600 Ω
- START

Alignment : At f = 1513 Hz, use 18 L 1 to set maximum attenuation
At f = 3147 Hz, use 18 L 2 to set maximum attenuation
At f = 3374 Hz, use 18 L 3 to set maximum attenuation
At f = 2579 Hz, use 18 L 4 to set maximum attenuation

7.3.19 18 L 5, L 6

This alignment is only necessary after repairs on the LP filter

Test setup : - Same as setup for 18 P 1, P 2, P 3

Entry on PCM-4: - MA 13 E
- MAN/S, [A-A]
- VAR MODE 511 E RTN
- Level -24 dB E (or same setting as for ext. level generator)
- Ze = 600 Ω
- START

Alignment : At f = 342 kHz, use 18 L 5 to set maximum attenuation
At f = 225 kHz, use 18 L 6 to set maximum attenuation

7.3.20 27 C 23

Test setup : - Fit coupling card 2 ([984-AD]) on the adapter
- Connect the frequency counter to 27 TP 4, 27 TP 5

Alignment : - Use 27 C 23 to align the frequency to 32.76800 kHz ± 0.0002 kHz

7.3.21 1 P 21

Test setup : - Remove the cover of the PCM-4
- Remove the instrument from the housing
- Do not disconnect from the power supply unit (load)
- The data retention board (38) [959-AV] is located on the power supply unit bolted onto the right-hand side element
- Connect the oscilloscope to 1 TP 6, 1 TP 2 [Ground]

Alignment : - Set potentiometer 1 P 21 so that a HIGH pulse of about 20 ms pulse width (at an instrument load of 10 A, 220 V) is produced when the ON/OFF switch is operated (Mains OFF) (see Fig. 7.3.21-2)
- Check the Mains ON pulse (see Fig. 7.3.21-1)

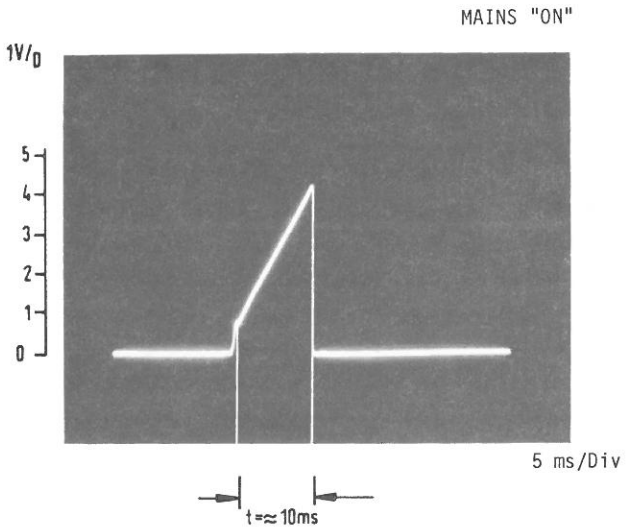


Figure 7.3.21-1 Mains "ON"

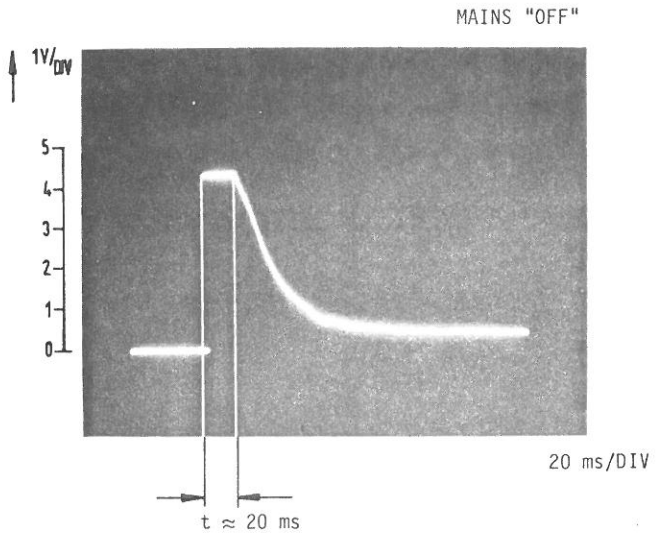


Figure 7.3.21-2 Mains "OFF"

7.3.22a) 92 P 1

Settings on the PCM-4: A 11, L = -30 dBm0, Channel, WOB/E

- Press the START key and wait for the measurement to end
- Use the "Brightness" potentiometer [34] on the rear of the instrument to set the brightness of the bars to a pleasant level.
- Use 92 P 1 on card [962-A]* to set the background brightness of the screen mask in such a way that the bars of the measurement results contrast slightly with the brightness of the screen mask.

* Depending on instrument version, it may be necessary to remove the rear instrument panel (cover plate) to make this adjustment.

7.3.22b) 93 P 5, P 6, P 7

PCM-4 setting : MODE A 11

Alignment : Turn the brightness potentiometer on the rear side of the instrument to about 1/5 away from the right-hand stop (max. brightness).

- Use 93 P 5 to set the maximum brightness in such a way that no line flyback traces can be seen, then turn back about another 1 mm.

Now turn the brightness potentiometer on the rear side of the instrument to about 1/5 away from the left-hand stop (min. brightness).

- Use 93 P 7 to set the monitor so that the test pattern just becomes visible.

Set the brightness potentiometer on the rear side to the middle position.

- Use 93 P 6 (focus) to set optimum picture definition.

7.3.23 93 P 1

PCM-4 setting : MODE A 11

Alignment : Adjust picture height with 93 P 1 so that a space of approx. 5 mm is left between the top or bottom lines of text and screen edge.

7.3.24 93 S 2

PCM-4 setting : MODE A 11

Alignment : Set the picture width wire links ac through ak so that a space of approx. 5 mm is left between the right-hand or left-hand texts and the edge of the screen. S 2 must be open when making this adjustment.

7.3.24a 93 P 2

PCM-4 setting : MODE A 11

Alignment : Turn 93 P 2 fully to the left (picture rolls down). Turn 93 P 2 to the left until the picture locks.

7.3.24b 93 P 4

PCM-4 setting : MODE A 11

Alignment : Short-circuit pin 9 of 93 IC 2 to ground (picture rolls horizontally and vertically). Set 93 P 4 so that the picture no longer or only just rolls horizontally.
Remove the short-circuit.

7.3.24c 93 C 48

PCM-4 setting : MODE A 11

Alignment : Adjust 93 C 48 to give maximum picture brightness.

7.3.24d 93 C 49

PCM-4 setting : MODE A 11

Alignment : There is no need to adjust 93 C 49, as the video signal input is only used for test purposes (monitor test [35]).

7.3.25 21 C 1

An 8 kHz clock signal must be present at IC 1/PIN 8 or IC 4/PIN 19. If the frequency deviates, alignment must be carried out with C 1 and a frequency counter connected to IC 1/PIN 8.

7.3.26 Alignment operations on the power supply unit C 15 A

See figure 10.4-4 for locations and layouts of Bu 1 and Bu 4.

Auxiliary equipment: Digital voltmeter, e.g. Fluke 8600A.

7.3.26-1 Adjustment of +5V/10A supply rail (R 217, R 225)

Test setup : Connect the DVM to Bu 1 pin 1, 2 or 3, ground to Bu 1 pin 4, 5 or 6.

Initial setting: Current limit I_A set to maximum (turn R 225 fully to the right).

Adjustment : Set R 217 so that the DVM reads +5.10 V $\pm$ 50 mV, then adjust R 225 so that the current limiting just does not operate. Check the voltage at the connector for the analog generator 1 [984-X], pins a, b and c (should be +5.10 V $\pm$ 50 mV).

7.3.26-2 Adjustment of +12V/1.1A supply rail (R 309)

Test setup : Connect the DVM to Bu 4 pin 6, ground to Bu 4 pin 9.

Adjustment : Adjust R 309 so that the DVM reads +12.00 V $\pm$ 50 mV.

7.3.26-3 Adjustment of +15V/0.8A supply rail (R 319)

Test setup : Connect the DVM to Bu 4 pin 10, ground to Bu 4 pin 11.

Adjustment : Adjust R 319 so that the DVM reads +15.00 V $\pm$ 50 mV.

7.3.26-4 Adjustment of -15V/0.8A supply rail (R 322)

Test setup : Connect the DVM to Bu 4 pin 12, ground to Bu 4 pin 11.

Adjustment : Adjust R 322 so that the DVM reads -15.00 V $\pm$ 50 mV.

7.3.26-5 Adjustment of +18V/0.15A supply rail (R 325)

Test setup : Connect the DVM to Bu 4 pin 5, ground to Bu 4 pin 11.

Adjustment : Adjust R 325 so that the DVM reads +18.00 V $\pm$ 50 mV.

7.3.26-6 Adjustment of -18V/0.15A supply rail (R 328)

Test setup : Connect the DVM to Bu 4 pin 8, ground to Bu 4 pin 11.

Adjustment : Adjust R 328 so that the DVM reads -18.00 V $\pm$ 50 mV.

7.3.26-7 Adjustment of +15V/0.45A supply rail (R 303)

Test setup : Connect the DVM to Bu 4 pin 1, ground to Bu 4 pin 4.

Adjustment : Adjust R 303 so that the DVM reads +15.00 V $\pm$ 50 mV.

7.3.26-8 Adjustment of -15V/0.45A supply rail (R 305)

Test setup : Connect the DVM to Bu 4 pin 7, ground to Bu 4 pin 4.

Adjustment : Adjust R 305 so that the DVM reads -15.00 V $\pm$ 50 mV.

7.4 ALIGNMENT OPERATIONS IN THE DIGITAL SECTION

7.4.1 ALIGNMENT OPERATIONS ON CLOCK CIRCUIT (25) [984-V]

7.4.1.1 8 kHz detector alignment

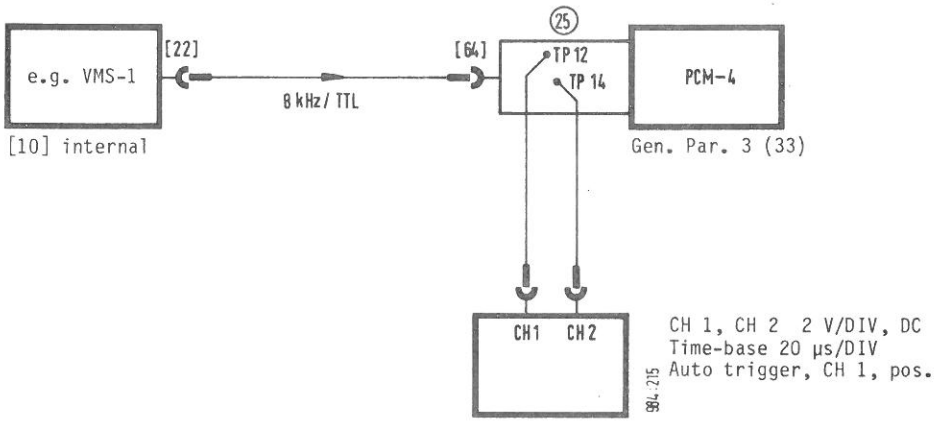


Figure 7.4.1-1 Test setup

Use P 1 to set the HIGH time at TP 12 to 110 µs.

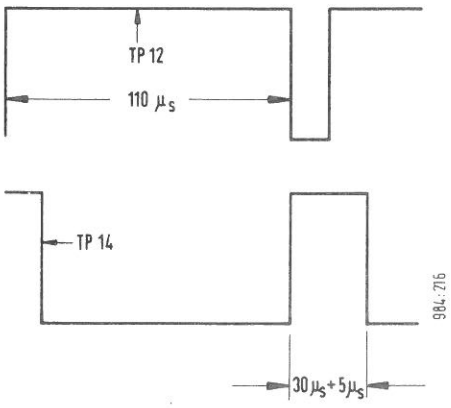


Figure 7.4.1-2 Timing

7.4.1.2 2.048 MHz detector alignment

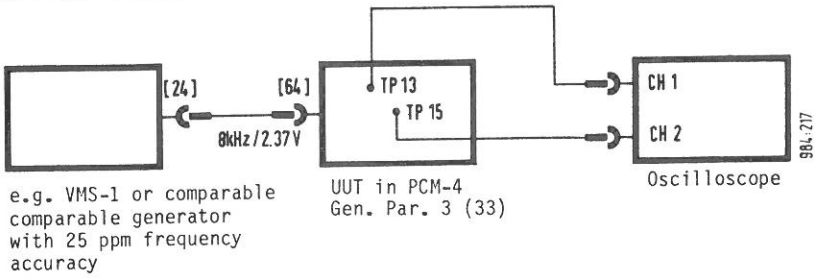


Figure 7.4.1-3 Test setup

Setting on the VMS-1 : [10] Internal

Setting on the oscilloscope: CH 1, CH 2 2 V/DIV
Time-base 0.1 µs/DIV
Trigger AUTO, CH 1 neg.

Alignment: Use P 2 to set the active time of IC 5/2 (Tp 13) so that the positive edge of the Tp 13 signal lies in the middle of the positive Tp 15 pulse.

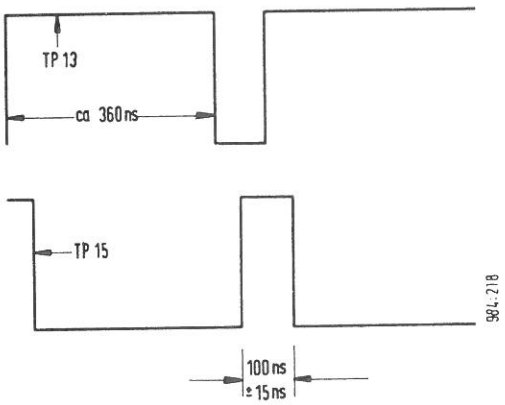


Figure 7.4.1-4 Timing

7.4.1.3 Oscillator alignment

Test setup:

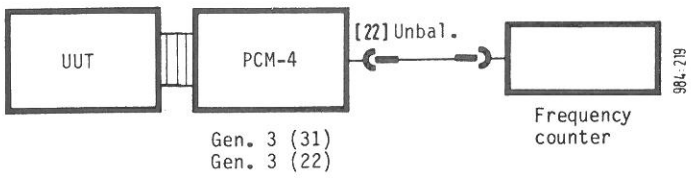


Figure 7.4.1-5 Test setup

Alignment: Use C 31 (Series A + B) or P 3 (Series C ...) to set the oscillator frequency (frequency counter display) to
2048,000 kHz ± 1 Hz.

7.4.1.4 PCC alignment [893-E]

The PCC circuit is aligned without applying an input signal.

Test setup:

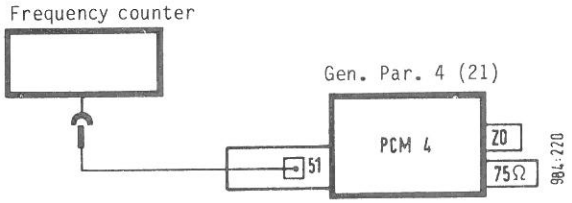


Figure 7.4.1-6 Test setup

Connect the frequency counter to Pt. 51 of board [893-E]; terminate PCM-4 input [20] with 75 Ω.

Use C 104 to set a frequency of 2048 kHz ± 40 Hz.

7.4.2 ALIGNMENT OPERATIONS ON PCM-30 OUTPUT (16) [984-S]

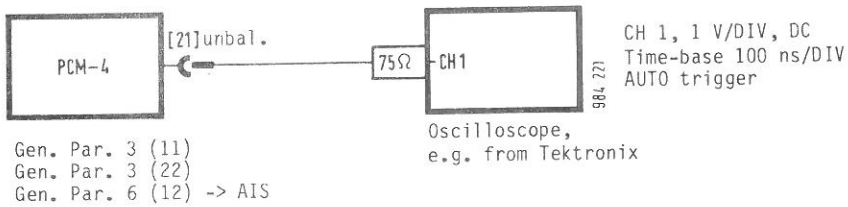


Figure 7.4.2-1 Test setup

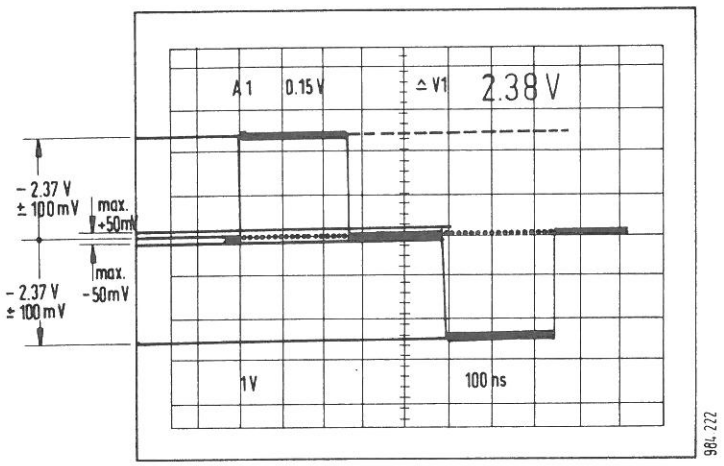


Figure 7.4.2-2 Oscillogram of the PCM-30 output

Use P 1 and P 2 to align in compliance with the above oscillogram. If necessary, use an iterative procedure.

7.4.3 ALIGNMENT OPERATIONS ON PCM-30 INPUT (14) [984-R]

7.4.3.1 IC 1 offset alignment

Test setup:

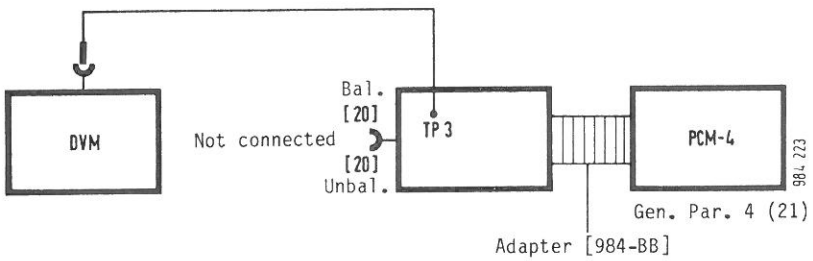


Figure 7.4.3-1 Test setup

Align with P 1 at Tp 3 to < ± 0.3 mV.

7.4.3.2 Switching threshold setting on Tp 4 and Tp 5

7.4.3.2.1 Setting the switching threshold on Tp 4 with P 2

Test setup:

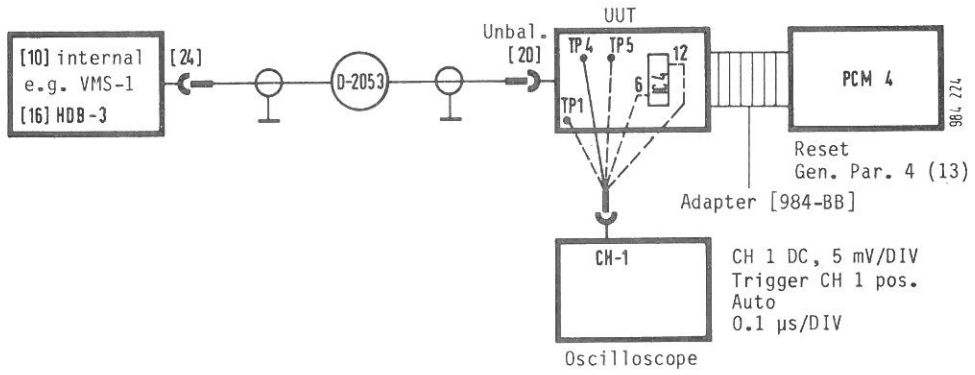


Figure 7.4.3-2 Test setup

Alignment: - Use D-2053 to set 40 mV_{pp} at IC 4, Pin 6.
Use the vertical position knob to bring the full oscillogram onto the screen. Then do not adjust the vertical position knob any more.
- Now connect CH 1 to Tp 4 and use P 2 to turn U_{TP4} to the middle of the bottom half of the screen.

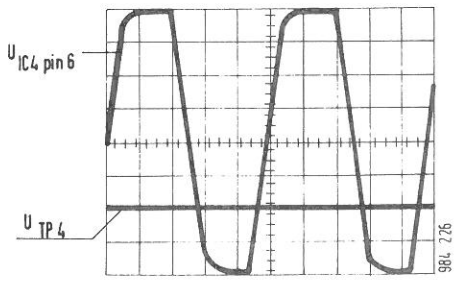


Figure 7.4.3-3 Oscillogram

7.4.3.2.2 Setting the switching threshold on Tp 5 with P 3

Test setup as under 7.4.3.2.1

Alignment: - Use D-2053 to set 40 ms V_{pp} at IC 4, Pin 12.
Use the vertical position knob to bring the full oscillogram onto the screen.
Then do not adjust the vertical position knob any more.
- Now connect CH 1 to Tp 5 and use P 3 to turn U_{TP5} to the middle of the top half of the screen.

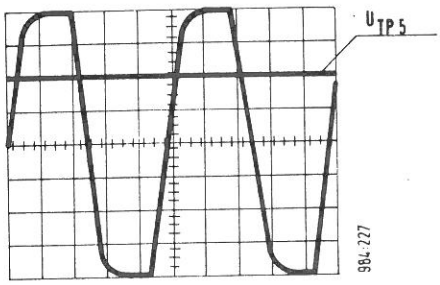


Figure 7.4.3-4 Oscillogram

7.4.3.3 Setting the "No Signal" threshold

Test setup as under 7.4.3.2.1

Alignment: 1. Use D-2053 to set 17 mV_p at Tp 1 and P 4 to make the NO SIGNAL LED just light up.
2. Use D-2053 to increase U_{TP1} slowly. The NO SIGNAL LED must go out when reaching U_{TP1} = 21 mV_p at the latest.
3. Use D-2053 to reduce U_{TP1} slowly. The NO SIGNAL LED must light up again when U_{TP1} has been reduced to 17 mV_p at the latest.

7.4.4 ALIGNMENT OPERATIONS ON THE PDG-64 (22) [984-H]

7.4.4.1 Alignment of the CODEC module IC 30 with (22) P 1

Test setup:

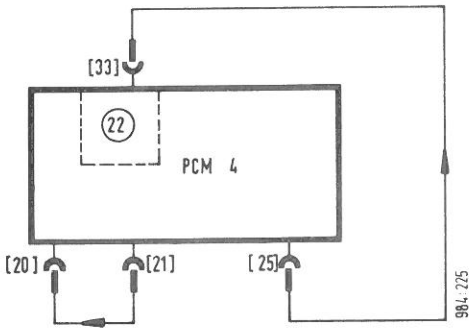


Figure 7.4.4-1 Test setup

PCM-4 setting: MA 11, [A-D], VAR MODE 2 (45)
MAN/R, f = 813 Hz, LEVEL = -10 dB
START

Alignment: Use (22) P 1 to set the repeating PCM-4 result display to -10 dB $\pm$ 0.1 dB.

8 SPECIFICATION CHECK

8.1 INTRODUCTION

The following describes techniques for checking the specifications of the instrument. As far as possible, commercially available test equipment is used. It is assumed that the instrument to be tested is fully operational.

Unless otherwise noted, the tests and any necessary adjustments should be carried out within the nominal range of use of ambient temperature and after the specified warm-up period has elapsed.

The specification checks will establish whether the display or output of a measured quantity lies within the specified error limits of the instrument. The test results are absolute only if the uncertainty in the test equipment used is negligible. Wherever the use of commercially available equipment is likely to lead to a distortion of the results, a further method will be indicated which makes use of test equipment produced in the factory for this purpose. Such tests are headed "Factory Test".

The error of the test equipment used is always assigned to the item under test (see IEC Publication 359) when deciding whether or not the error limits have been exceeded.

In the case where errors are symmetrical about the mean value, the following principle holds true: if the error of the test equipment used is $\pm$ m and the specified error limit of the item under test is given as $\pm$ e, then

if the limit $\pm$ (e + m) is exceeded, then the specified error limits have definitely been exceeded, and

if the limit $\pm$ (e - m) is not exceeded, then the specified error limits have definitely not been exceeded.

As far as possible, the values of e and m are quoted for each test. Since the value of m is dependent on the test equipment used, it must be determined if equipment other than that specified in the tests is used.

To ensure a systematic check of the specifications, we recommend that the tests be carried out in the order in which they are given.

Adjustment of the item under test need only be carried out when the total determined error is greater than $\pm$ (e + m).

8.2 RETURN LOSS

Test equipment required:

1 level generator	PS-19	from W & G
1 selective level meter	SPM-19	from W & G
1 return loss measuring attachment	RFZ-12	from W & G
with 1 CF adaptor for balanced measurements and 1 Versacon® 9 adaptor for unbalanced measurements		
1 standard impedance for RFZ-12	850 Ω $\pm$ 0.1%	
1 standard impedance for RFZ-12	900 Ω $\pm$ 0.1%	
1 standard impedance for RFZ-12	220 Ω + (820 Ω//115 nF) R: $\pm$ 0.1%; C: $\pm$ 1%	

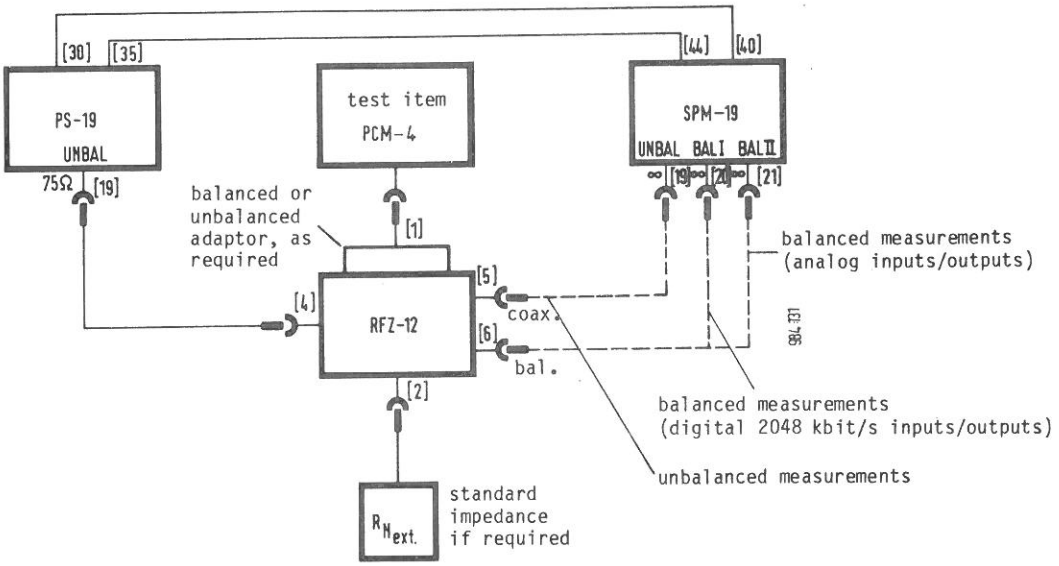


Figure 8.2-1 Test setup for measuring return loss

Initial instrument settings

PS-19:

Output	[15]	: UNBAL, Z_o = 75 Ω
Output level	[2], [3], [4]	: 0.0 dB
EXT.	[7]	: ON
dB/dBm switch	[31]	: dB

SPM-19:

Input	[15]	:
a) unbalanced/coaxial measurements:		UNBAL 75 Ω, Z_i = ∞
b) balanced measurements:		BAL II 150 Ω, Z_i = ∞
2048 kbit/s interface measurements:		BAL I 150 Ω, Z_i = ∞
Mode	[4]	: DGTL
Bandwidth	[16]	: 25 Hz
Test frequencies	[7], [12]	: as in table
dB/dBm switch	[46]	: dB

RFZ-12:

Operating mode	[7]	: bal. or unbal. depending on test point
R_N	[3]	: depending on test point

Calibrating the test setup

Set the calibration frequency of 10 kHz for the SPM-19 using [7] and [12]. Set the impedance value (R_N) required for the test with switch [3] on the RFZ-12, or connect a standard R_N to socket [2]. Disconnect the RFZ-12 from the item under test. Press /ABS/ and /REF/ simultaneously (SPM-19), then press /ABS-REF/. The display should read 0 dB, corresponding to a reflection coefficient of r = 1 (return loss a_r = 0 dB). This calibration procedure must be repeated if the value of R_N is changed, or if a different input is selected on the SPM-19.

8.2.1 4-WIRE INPUT RETURN LOSS [23]

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 13
Softkey 1	[9] : [A-A]
Receiver impedance	[13] : see R_n in figure 8.2.1-1

SPM-19:

Test frequency	[7], [12] : see f in figure 8.2.1-1

RFZ-12:

Operating mode	[7] : balanced
Standard impedance	[3] : see R_n in figure 8.2.1-1

Connection between RFZ-12 and SPM-19:

RFZ-12, Bu [6] ⟶ SPM-19, BAL II [21]

Measurement:

f / R_n	201 Hz			4015 Hz			128 kHz		
	e/dB	m_o/dB	m_u/dB	e/dB	m_o/dB	m_u/dB	e/dB	m_o/dB	m_u/dB
600 Ω	≥ 46	3.1	2.3	≥ 46	3.1	2.3	≥ 30	1.3	1.2
850 Ω	≥ 46	3.1	2.3	≥ 46	3.1	2.3	≥ 30	1.3	1.2
900 Ω	≥ 46	3.1	2.3	≥ 46	3.1	2.3	≥ 30	1.3	1.2
CPLX	≥ 30	1.9	1.6	≥ 30	1.9	1.6	—	—	

CPLX = 220 Ω + 820 // 115 nF
e = specified limit value
m = test setup error

Figure 8.2.1-1 Table for checking the 4-wire input return loss

Example for application of the measurement error:
The guaranteed error limit ≥ 46 dB has definitely been
- exceeded if $(e - m_u) \leq 43.7$ dB
- met if $(e + m_o) \geq 49.1$ dB

8.2.2 2-WIRE INPUT RETURN LOSS [24]

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 13
Softkey 3	[9] : [D-A]
Interface	[14] : 2-wire
Receiver impedance	[13] : 600 Ω

SPM-19:

Test frequency	[7], [12] : f = 3995 Hz

RFZ-12:

Operating mode	[7] : balanced
Standard impedance	[3] : R_n = 600 Ω

Connection between RFZ-12 and SPM-19:

RFZ-12, Bu [6] ⟶ SPM-19, BAL II [21]

Measurement:

Specified limit value (e): $\geq$ 46 dB

Test setup error (m): m_o = 3.1 dB

m_u = 2.3 dB

The same input circuit is used in the PCM-4 for sockets [23] and [24], so only the one value for socket [24] needs to be checked.

8.2.3 4-WIRE OUTPUT RETURN LOSS [25]

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 13
Softkey 1	[9] : [A-A]
Generator output impedance	[15] : see R_n in figure 8.2.1-1
Frequency	[5], [6] : 25 kHz
Output level	[5], [6] : -20 dB/-30 dB

SPM-19:

Test frequency	[7], [12] : 201 Hz, 4 015 Hz, 71 970 Hz

RFZ-12: (see section 8.2.1)

Operating mode	[7] : balanced
Standard impedance	[3] : see R_n in figure 8.2.1-1

Connection between RFZ-12 and SPM-19:

RFZ-12, Bu [6] —► SPM-19, BAL II [21]

Measurement:

Check the 4-wire output as per figure 8.2.1-1. Carry out the tests using two different output levels from the PCM-4 (-20 dBm0 and -30 dBm0). Use 71970 Hz instead of the 128 kHz frequency in figure 8.2.1-1.

8.2.4 2-WIRE OUTPUT RETURN LOSS [24]

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 81
Softkey 2	[9] : [A-D]
Interface	[14] : 2-wire
Generator output impedance	[15] : 600 Ω
Frequency	[5], [6] : 25 kHz
Output level	[5], [6] : -20 dBm0

SPM-19:

Test frequency	[7], [12] : f = 4015 Hz

RFZ-12:

Operating mode	[7] : balanced
Standard impedance	[3] : R_n = 600 Ω

Connection between RFZ-12 and SPM-19:

RFZ-12, Bu [6] —► SPM-19, BAL II [21]

Measurement:

Specified limit value (e): ≥ 46 dB

Test setup error (m): m_o = 3.1 dB

m_u = 2.3 dB

8.2.5 AUXILIARY SIGNAL OUTPUT RETURN LOSS [30], [31]

Instrument settings:

SPM-19:

Test frequency	[7], [12] : see f in figure 8.2.5-1

	bal. output [30]	unbal. output [31]
RFZ-12:		
Operating mode	[7] : balanced	coaxial
Standard impedance (R_n)	[3] : 600 Ω	600 Ω
Connection between RFZ-12 and SPM-19:	RFZ-12, Bu [6] —►SPM-19, BAL II [21]	RFZ-12, Bu [5] —►SPM-19, UNBAL [19]

Measurement:

test frequency (f)	specified limit value (e)	test setup error (m)	
		m_o	m_u
	balanced + unbalanced	bal. unbal.	bal. unbal.
351 Hz	$\geq$ 26 dB	1.2 dB	1.1 dB
552 Hz	$\geq$ 30 dB	1.3 dB	1.2 dB
3403 Hz	$\geq$ 30 dB	1.3 dB	1.2 dB

Figure 8.2.5-1 Table for checking the return losses of outputs [30] and [31]

Example for application of the measurement error:
The guaranteed limit value of $\geq$ 26 dB has definitely been
- exceeded if $(e - m_u) \leq 24.9$ dB
- met if $(e + m_o) \geq 27.2$ dB

8.2.6 RETURN LOSS OF THE 2048 kbit/s INTERFACE [20], [21], [22]

Connection:	balanced	unbalanced
Instrument settings:		
PCM-4:		
Measurement mode	[1], [6] : MODE LIST A 11	MODE LIST A 11
Gen. param.	[1], [6] : 4 11 ENTER	4 13 ENTER
Gen. param.	: 3 12 ENTER 21 ENTER	3 12 ENTER 22 ENTER
Gen. param.	: 6 12 ENTER	6 12 ENTER
SPM-19:		
Test frequency	[7], [12] : see measurement	see measurement
RFZ-12:		
Operating mode	[7] : balanced	coaxial
Standard impedance R_N	[3] : 124 Ω	75 Ω
Connection between RFZ-12 and SPM-19:	RFZ-12, Bu [6] —SPM-19, BAL I [20]	RFZ-12, Bu [5] —SPM-19, UNBAL [19]

Connection:	balanced		unbalanced	
Measurement:				
Test frequency (f)	40 kHz	2.5 MHz	40 kHz	2.5 MHz
Specified limit value (e)	> 20 dB	> 20 dB	> 20 dB	> 20 dB
Test setup error (m) m_o	2.5 dB*	2.6 dB*	1.1 dB	1.2 dB
m_u	2.6 dB	2.6 dB	1.0 dB	1.1 dB

* The impedance of the balanced input is 120 Ω. The use of a 124 Ω resistor causes an error in the measurement; this error is, however, taken into account in the figures given.

8.3 SIGNAL BALANCE RATIO

Test equipment required:

1 level generator	PS-19	from W & G
1 selective level meter	SPM-19	from W & G
1 signal balance ratio bridge	SDZ-12	from W & G

8.3.1 GENERATOR SIGNAL BALANCE RATIO

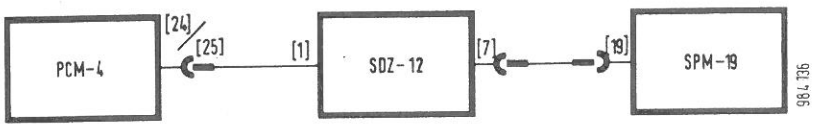


Figure 8.3.1-1 Test setup for measuring the generator signal balance ratio

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 81
Softkey 2	[9] : [A-D]
Interface	[14] : 4-wire (output [25])/2-wire (output [24])
Generator output impedance	[15] : 600 Ω
Frequency	[5], [6] : 71970 Hz
Output level	[5], [6] : 0 dBm0

SPM-19:

Input	[15] : UNBAL 75 Ω, Z_i =∞
Mode	[4] : DGTL
Bandwidth	[16] : 3.1 kHz
Frequency	[7], [12] : 71970 Hz
dB/dBm switch	[46] : dB

SDZ-12:

Test item	[2] : generator
Z switch	[4] : 600 Ω

Measurement:

The display on the SPM-19 equals the signal balance ratio with reversed sign.

Specified limit value (e): $\geq$ 46 dB

Test setup error (m): m_u = 1.6 dB

m_o = 2.0 dB

Example for application of the measurement error:

The guaranteed error limit $\geq$ 46 dB has definitely been

- exceeded if $(e - m_u) \leq 44.4$ dB
- met if $(e + m_o) \geq 48.0$ dB

8.3.2 RECEIVER SIGNAL BALANCE RATIO

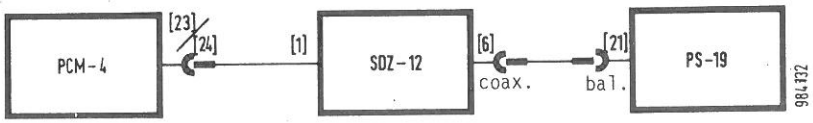


Figure 8.3.2-1 Test setup for measuring the receiver signal balance ratio

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 83
Softkey 3	[9] : [D-A]
Softkey 5	[9] : MAN/R
Interface	[14] : 4-wire (input [23])/2-wire (input [24])
Receiver input impedance	[13] : 600 Ω

PS-19:

Output	[15] : BAL II 600 Ω, Z_i = Ø
Output level	[2], [3], [4] : 0.0 dB
Frequency	[8], [13] : 120 kHz
dB/dBm switch	[31] : dB

SDZ-12:

Test item	[2] : receiver
Z switch	[4] : 600 Ω

Measurement:

Both the 2-wire- and 4-wire inputs are checked. The measurement is started by pressing /START/ on the PCM-4. The display on the PCM-4 equals the signal balance ratio with reversed sign.

Specified limit value (e): $\geq$ 46 dB

Test setup error (m): m_u = 1.7 dB

m_o = 2.0 dB

8.4 ANALOG SIGNAL GENERATOR ABSOLUTE ACCURACY

Notes on sections 8.4 to 8.6

- The tests in sections 8.4 to 8.6 are for determining important partial errors which make up the analog generator- and receiver level error limits. If the individual partial error limits are met, the instrument also meets the specified overall error limits.
- The absolute level and the linearity of the analog generator and receiver in the PCM-4 are calibrated automatically (correction values stored in memory). Hence, all errors can be traced back to the accuracy of the reference attenuator in the receiver. It is therefore sufficient to check level accuracy and linearity for this circuit.

Test equipment required:

1 milliwatt power meter with accessories	EPM-1	from W & G
1 test probe	TKS-10	from W & G
1 test probe adaptor	TKSA-600	from W & G
1 calibration adaptor	TKSE-600	from W & G

8.4.1 LF GENERATOR ABSOLUTE ACCURACY

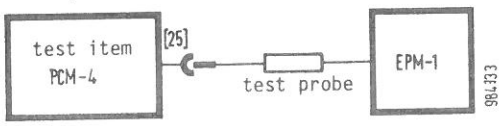


Figure 8.4.1-1 Test setup for measuring the absolute accuracy of the LF generator

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 11
Softkey 1	[9] : [A-A]
Generator output impedance	[15] : 600 Ω
Frequency	[5], [6] : 813 Hz
Output level	[5], [6] : 0 dBm0

EPM-1:

Calibration level switch	: 0 dB, R_i = 75 Ω
Measurement range	: 0 dBm ± 0.2 dBm

Calibrating the EPM-1

Connect the test probe TKS-10 + TKSA-600 to the TKSE-600 calibration adaptor, and adjust the instrument display to 0 using the calibration potentiometer.

Measurement:

Connect the test probe to output [25] of the PCM-4.

Specified limit value (e): ± 5 mB
Test setup error (m): ± 1.5 mB

8.4.2 AUXILIARY SIGNAL OUTPUT ABSOLUTE ACCURACY

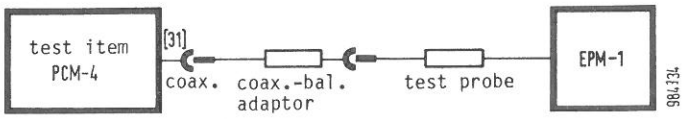


Figure 8.4.2-1 Test setup for measuring the absolute accuracy of the auxiliary signal output

Instrument settings:

PCM-4:

Measurement mode [1], [6]	: MODE LIST A 11
Special functions	[3] : VAR. MODE 1.53 ENTER 54 LEVEL -40 dBm0 ENTER[1)]

EPM-1:

Calibration level switch	: 0 dB, R_i = 75 Ω
Measurement range	: 0 dBm ± 0.2 dBm

Calibrating the EPM-1

Connect the test probe (TKS-10 + TKSA-600) to the calibration adaptor TKSE-600, and adjust the calibration potentiometer so that the display reads 0.

Measurement:

Connect the EPM-1 test probe to output [31] of the PCM-4 via an adaptor.

Specified limit value (e): ± 0.3 dB
Test setup error (m): ± 1.5 mB

8.5 LF INTERFACE FREQUENCY RESPONSE

Test equipment required:

1 milliwatt power meter with accessories:	EPM-1	from W & G
1 test probe	TKS-10	from W & G
1 test probe adaptor	TKSA-600	from W & G
1 level generator	PS-19	from W & G

8.5.1 LF GENERATOR FREQUENCY RESPONSE

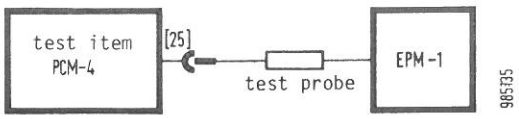


Figure 8.5.1-1 Test setup for measuring the LF generator frequency response

1) This setting produces an output level of 0 dBm0 at output [31]

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 13
Softkey 1	[9] : [A-A]
Softkey 5	[9] : MAN/R
Generator output impedance	[15] : 600 Ω
Receiver input impedance	[13] : 600 Ω
Frequency	[5], [6] : 813 Hz
Output level	[5], [6] : 0 dBm0

EPM-1:

Measurement range	: 0 dBm ± 0.2 dBm

Measurement:

- Setting the EPM-1 to 0 at the reference frequency of 813 Hz:
  Connect the test probe to output [25] of the PCM-4 and adjust the calibration potentiometer to give a display reading of 0.
- Make measurements at the frequencies listed in figure 8.5.1-2 and note the receiver frequency response results.
- Repeat the measurement at 201 Hz, 1997 Hz and 3995 Hz with the PCM-4 set to MODE LIST A 11. See figure 8.5.1-2 for nominal values.

Frequency (Hz)	Extra error limit information (e)*	test setup error (m)
813	Reference measurement	± 0.3 mB
20	-15 mB/+3 mB	
100	-10 mB/+3 mB	
201 1997 3995	± 3 mB	
10038 39950 71970	-11 mB/+15 mB	

Figure 8.5.1-2 Table for checking the LF generator frequency response

8.5.2 LF RECEIVER FREQUENCY RESPONSE

The PCM-4 makes use of three different sampling techniques, depending on the mode chosen. Therefore, three frequency response measurements need to be made.

8.5.2.1 PCM-4 frequency response in modes A 12 and A 13

Test setup: Connect PCM-4 output [25] to the receiver input [23].

Note: The measured values are corrected by subtracting the frequency response figures previously determined for the generator from the receiver frequency response.

---

* This information is not included in the technical data

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 13
Softkey 1	[9] : [A-A]
Softkey 5	[9] : MAN/R
Generator output impedance	[15] : 600 Ω
Receiver input impedance	[13] : 600 Ω
Frequency	[5], [6] : 813 Hz
Output level	[5], [6] : 0 dBm

Measurement:

- Set the reference frequency of 813 Hz for an output level of 0 dBm0 and start the measurement run by pressing /START/ [2].
- Take the average of the displayed level and set this level with reversed sign using [5], [6]. The measured result should now be approx. 0 dBm0.
- Check the frequency response using the settings shown in figure 8.5.2-1.

PCM-4 mode	Frequency (Hz)	Extra error limit information (e)*	Test setup error (m)
A 13	813	Reference measurement	± 0.1 dB
	20 201 3995 10038 39950 71970	+ 0.3 dB/-0.5 dB As a random evaluation procedure is used, the error limit has a statistical certainty of 95%	
A 12	813	Reference measurement	± 1.0 mB
	20 100	+9 mB/-29 mB	
	201 1997 3995	± 3 mB	

Figure 8.5.2-1 Table 1 for checking the LF receiver frequency response

* This information is not included in the technical data

8.5.2.2 Frequency response measurement in PCM-4 mode A 83

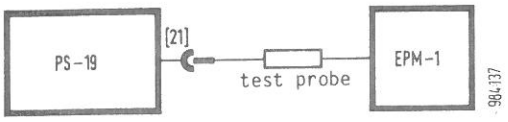


Figure 8.5.2-2 Test setup for measuring the frequency response of the PS-19

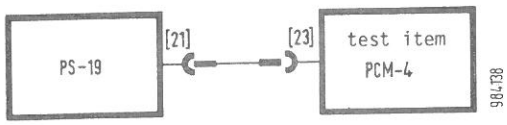


Figure 8.5.2-3 Test setup for measuring the LF receiver frequency response in PCM-4 mode A 83

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 83
Softkey 1	[9] : [A-A]
Softkey 5	[9] : MAN/R
Receiver input impedance	[13] : 600 Ω

PS-19:

Output	[15] : BAL. II, Z_o = 600 Ω
Output level	[2], [3], [4] : 0.0 dB

Recording the frequency response of the PS-19

Connect the generator output [21] of the PS-19 to the EPM-1 test probe. Set the PS-19 to the reference frequency of 10038 Hz and set the display on the EPM-1 to 0 using the calibration potentiometer. Set the frequencies listed in figure 8.5.2-4 and read off the value indicated by the EPM-1 in each case. Make a note of these values (FR).

PCM-4 measurement

Connect output [21] of the PS-19 to input [23] of the PCM-4. Set the PS-19 to the reference frequency of 10038 Hz and start the PCM-4 measurement run. Determine the average value of the result displayed by the PCM-4 (AV) and note this down. Then make measurements at all the other frequencies in the table in figure 8.5.2-4 and note the value displayed by the PCM-4 (DL). The corrected value (CV) can then be determined as follows:

CV = DV - AV - FR

CV = corrected value
DV = displayed value (PCM-4)
AV = average value displayed (PCM-4) at reference frequency
FR = PS-19 frequency response

Frequency (Hz)	Extra error limit information (e)*	Test setup error (m)
10038	Reference measurement	
4617 5521	-0.5 dB/+0.3 dB	± 1.5 mB
39950 71970 128000	± 0.3 dB	

Figure 8.5.2-4 Table 2 for checking the LF receiver frequency response

8.6 ACCURACY OF THE LF INTERFACE REFERENCE ATTENUATOR

Test equipment required:

1 level generator	PS-19	from W & G
1 transformer attenuator	Mod. 1011	Gertsch/Ailtech
1 digital multimeter	HP 3478 A	Hewlett-Packard

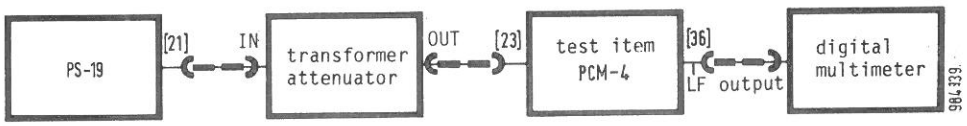


Figure 8.6-1 Test setup for measuring the accuracy of the reference attenuator

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 11
Softkey 1	[9] : [A-A]
Softkey 5	[9] : MAN/S
Receiver input impedance	[13] : > 30 kΩ

PS-19:

Output level	[2], [3], [4] : 0,0 dB
Output	[15] : BAL II, 600 Ω, Z_0 = 0 Ω
Frequency	[8], [13] : 813 Hz

Transformer attenuator:

Attenuation 0 dB	: FACTOR .X000 000

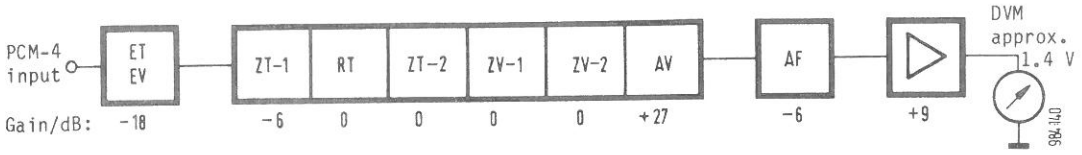
Digital multimeter:

Mode	: AC V, 5 digit
Range	: 3 V

* This information is not included in the technical data

Measurement:

- With an input level of 0 dB to the PCM-4, trigger a measurement by pressing /START/ [2]. This causes the attenuators in the PCM-4 to be set in the following way:



ET: Input attenuator
EV: Input amplifier
ZT-1: Intermediate attenuator 1
RT: Reference attenuator
ZT-2: Intermediate attenuator 2
ZV-1: Intermediate amplifier 1
ZV-2: Intermediate amplifier 2
AV: Output amplifier
AF: Analog filter
▷: LF/VF amplifier

- Set the transformer attenuator to 24 dB (FACTOR = .0625000
- PCM-4 settings: Special function [3] : MODE VAR.
  Softkey 1 [9] : press until the monitor menu is displayed
  CPU [11]: select CPU 2/3 with the "DIGIT WORD" key
  Softkey 2 [9], [6] : OUT 52.5C ENTER
  └Gen. PARAM key [1].
- Note the value displayed on the DVM (reference voltage, V_b).
- Set the attenuators as shown in the following table and read off the value on the DVM (V_1) (appr. 1.4 V):

transformer atten. setting atten./dB	factor	reference atten. setting via monitor	attenuator setting/dB RT	ZT-1	
18.06	.125	OUT 50.11 ENTER	6.02	6.02	
12.04	.25	OUT 50.21 ENTER	12.04	6.02	
6.02	.5	OUT 50.31 ENTER	18.06	6.02	
0	.1	OUT 50.41 ENTER	24.08	6.02	
24.08	.0625	OUT 50.01 ENTER	0	6.02	<basic setting (reference)

Figure 8.6-2 Table for checking the reference attenuator accuracy

- Calculate the reference attenuator accuracy as follows: $\Delta a/mB = 2000 \log \frac{V_1}{V_b}$

  Specified error limits (e): ± 0.5 mB
  Test setup error (m): ± 0.1 mB

8.7 FREQUENCY ACCURACY

Test equipment required:

1 universal counter/timer 5316 A Hewlett-Packard

Test setup:

Connect the LF generator output [25] or the generator clock output [22] (balanced) to input A of the counter/timer.

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 11
Softkey 3	[9] : [A-A]
Generator output impedance	[15] : 600 Ω
Frequency	[5], [6] : 813 Hz
Output level	[5], [6] : 0 dBm0

hp 5316 A:

Measurement mode	: FREQ. A
GATE TIME	: approx. 1 sec
Filter	: 100 kHz (only LF-generator output)

Measurement:

Read off the frequency displayed on the counter and determine the difference from the nominal value.

PCM-4 output	NF generator output [25]	Generator clock output [22]
Nominal value	813.039 Hz	2048 kHz
Specified error limits (e):	± 50 ppm ≅ ± 0.041 Hz	± 25 ppm ≅ ± 51 Hz
Test setup error (m):	± 5 ppm ≅ ± 0.004 Hz	± 5 ppm ≅ ± 10 Hz

8.8 ANALOG SIGNAL GENERATOR HARMONIC DISTORTION

Test equipment required:

1 selective level meter SPM-19 from W & G

Test setup:

Connect the PCM-4 generator output [25] to the SPM-19 receiver input [21].

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 13
Softkey 1	[9] : [A-A]
Generator output impedance	[15] : 600 Ω
Frequency	[5], [6] : 3995 Hz
Output level	[5], [6] : 0 dBm0

SPM-19:

Input	[15] : BAL II, Z = 600 Ω
Mode	[4] : DGTL
Bandwidth	[16] : 25 Hz
Frequency	[7], [12] : 3995 Hz

Calibrating the test setup:

Connect the PCM-4 to the SPM-19. Set the frequencies of the PCM-4 and the SPM-19 to the fundamental frequency. Press /ABS/ and /REF/ simultaneously (SPM-19), followed by /ABS-REF/. The SPM-19 display should read 0 dB.

Measurement:

Fundamental (PCM-4 setting)	Harmonic (SPM-19 setting)	Specified limit value (e)	Test setup error (m)
3995 Hz	K2: 7990 Hz K3: 11985 Hz	$\geq$ 63 dB $\geq$ 63 dB	$\pm$ 1.4 dB
10 038 Hz	K2: 20 076 Hz K3: 30 114 Hz	$\geq$ 43 dB $\geq$ 43 dB	$\pm$ 0.5 dB

8.9 RECEIVE FILTER (HARDWARE COMPONENT)

Test equipment required:

1 level generator PS-19 from W & G

Test setup:

Connect the PS-19 generator output [21] to the PCM-4 receiver input [23]

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 11 (4 kHz lowpass) MODE LIST A 82 (4.6 kHz highpass)
Softkey 1	[9] : [A-A]
Softkey 2	[9] : MAN/R
Receiver input impedance	[15] : 600 Ω

PS-19:

Output level	[2], [3], [4] : 0.0 dB
Output	[15] : BAL II, Z = 600 Ω
Frequency	[8], [13] : 813 Hz

Measurement:

Make a measurement at the reference frequency and note the level value for correcting later test values.

Measurement:

Filter	PS-19 output frequency	Filter attenuation specified error limits (e)	Test setup error (m)
4 kHz lowpass	813 Hz 4.8 kHz	reference measurement > 30 dB	± 0.15 dB
4.6 kHz highpass	10 038 Hz 3 600 Hz	reference measurement > 30 dB	± 0.13 dB

8.10 DIGITAL SIGNAL AND CLOCK PULSE WIDTH AND AMPLITUDE

Test equipment required:

1 oscilloscope Tektronix 2465 Tektronix

1 line termination, 75 Ω ± 1%

Test setup:

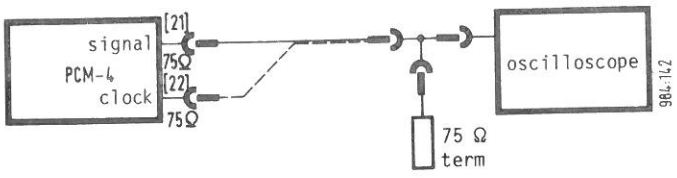


Figure 8.10-1 Test setup for measuring pulse amplitude

Instrument settings:

PCM-4:

Measurement mode	[1], [6] : MODE LIST A 11
General parameter	[1], [6] : 3 12 ENTER 22 ENTER 31 ENTER
General parameter	[1], [6] : 6 12 ENTER

Oscilloscope:

Timebase	: 100 ns/cm (50 ns/cm)
Y sensitivity	: 1 V/cm (0.5 V/cm)

Measurement:

The amplitude is referred to the zero line.
The waveforms depicted below must be present if the above settings are made. The pulse width is measured at half pulse height.

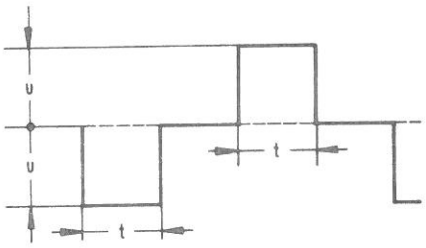


Figure 8.10-2 Output signal oscilloscope display

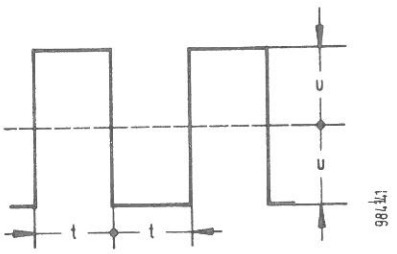


Figure 8.10-3 Output clock oscilloscope display

Pulse amplitude (U);	specified error limits (e):	2.37 V ± 10%
	test setup error (m):	± 3% (± 0.07 V)
Pulse width (t);	specified error limits (m):	244 ns ± 30 ns
	test setup error (m):	± 3% (± 7.3 ns)

9 FUNCTION AND CIRCUIT DESCRIPTION

9.1 FUNCTION DESCRIPTION OF THE INSTRUMENT

9.1.1 FUNCTION DESCRIPTION OF THE ANALOG SECTION

9.1.1.1 Analog generator

Principle of signal generation

Digital samples of various signals are stored sequentially in an EPROM. The samples are read out at the appropriate frequency.

There are two types of signal:

- Signals with a fixed frequency - these are read out by incrementing the EPROM address by one each time. If the address is greater than the array length -1 (array length = number of samples; -1 because the first address in the array is 0), read-out is started again at address 0000.
- Signals with variable frequency (sinusoidal functions):
  A whole cycle of a sinusoidal signal is stored in memory, the length of the array is a prime number. The values of the function are given by the following formula

  $$Yn = \sin [(2 \times \pi/F) \times n]$$

  The frequency that is generated, f, is given by the formula below.

  $$f = I \times f(clock)/F, \text{ where}$$

  I = increment
  f (clock) = rate at which samples are read out
  F = length of array (number of samples).

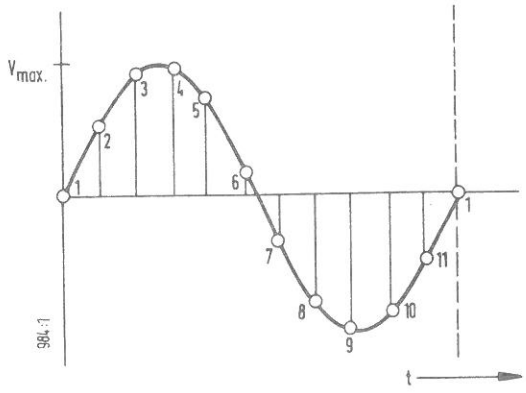


Figure 9.1.1-1a Cycle of a sinusoidal signal constructed from 11 samples

If the increment is equal to 1, the sinusoidal signal will have the lowest frequency.

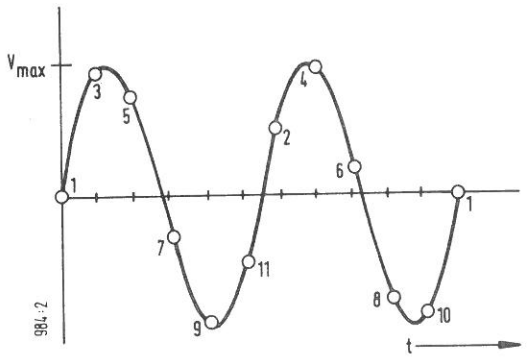


Figure 9.1.1-1b Same sample as in fig. 9.1.1-1a, but with increment equal to 2. Double the frequency is produced.

Example: Using a sampling frequency of 20 kHz, we want to produce a 1000 Hz sinusoidal tone from a set of 1999 sinusoidal samples (in-band signal):
The sequences Y0, Y100, to Y1900, Y1 (equals Y2000), Y101 to Y1901, Y2 (equal. to Y2001) ... are called up. Only when all 1999 samples have been used does the cycle repeat itself.

If increments other than 1 are used, other frequencies which are integer multiples of f_{min} (I = 1) are produced.

A prime number of samples is used to ensure that each sample is only used once in a complete cycle. This is an important criterium for noise reduction.

The analog generator has two outputs:
- Main output (CF connector on the front panel, balanced, floating, 20 Hz to 72 kHz)
- Auxiliary output unbalanced (coax.) and balanced (CF connector), both of these outputs are on the back panel.

Main output:

A specially developed address circuit has been developed to address the EPROM. The circuit can be programmed using the computer bus. In conjunction with the clock generation circuit, (200 kHz, 20 kHz and 8 kHz) it delivers a digital signal to the EPROM and the data latch.

The data (12 bits) is passed with the same timing as the clock via a data latch to a DAC which also acts as a multiplier. The data latch uses edge-triggering and suppresses glitches by simultaneously applying all 12 data bits to the DAC. It also suppresses incorrect addressing to the EPROM which occurs when the address circuit overflows.

The DAC multiplies the signal by a factor equal to the applied reference. The reference is adjustable and is controlled by the computer by means of another DAC. This allows one to alter the analog signal by about 0.5 mB per bit. This circuit is used to provide fine level adjustment and si equalisation for sinusoidal signals (see below).

A lowpass is used to limit the bandwidth of the signal, all components greater than 72 kHz are removed (band limiting out-of-band signal).

Depending on the frequency range, lowpasses with cutoff frequencies of 4.5 kHz and 1.76 kHz are used (see fig. 9.1.1-2 memory organisation for the main output).

Removing the high frequency components causes a drop in level which is described by the si function:

$$si\ (f) = \frac{\sin\ [2 \times \pi \times f\ (signal)/f\ (sampling\ rate)]}{2 \times \pi \times f\ (signal)/f\ (sampling\ rate)}$$

The samples for signals with fixed frequencies have a correction factor "built-in" and so do not need any further correction for the drop in level.

If the frequency of a signal can be varied (sinusoidal signals), the reduction in level is taken into account when the attenuator is set, the level at the reference converter is increased by the appropriate amount.

Coarse level setting is carried out in three stages:
1st stage: selectable 0 dB, 6 dB, 12 dB, 18 dB and 24 dB
2nd stage: selectable 0 dB, 30 dB
3rd stage: selectable 0 dB, 42 dB (output stage)

Output stage

The signal which is referred to earth is converted into a balanced, floating signal by means of two transformers (amplifier path and attenuator path). This signal is output at a CF connector, the output impedance is selectable and has the values 600 Ω, 850 Ω, 900 Ω and complex.

The generator signal can be looped-through internally, direct to the receiver, the output connector can be replaced by a bridge (calibration loop, send-side balance and return loss measurements).

To prevent dc voltages damaging the impedances that form the output impedance, the dc voltage level is monitored after these impedances. If the voltage is 1 V higher than the maximum open-circuit voltage, all resistors forming the internal impedance are disconnected for 70 ms (lowest signal frequency = 20 Hz -> 50 ms, no relay chatter at the signal frequency if the wanted signal is large and the superimposed dc voltage small).

A floating power supply for the output stage is produced in the power supply section.

The CF connector of the auxiliary output can be connected to the isolating amplifier of the 72 kHz lowpass to carry out absolute calibration on the generator signal (no coarse attenuator in the signal path); a calibrated level meter is connected. By adjusting the DIL switch, the calibrated level meter's display is made to read 0 dB.

Sample type	Address [hex]	Range division A13,A12,A11,A10, A9	Array length [dec]	Signal	Clock freq. [kHz]	Freq. range [Hz]	in steps of [Hz]	Low pass [kHz]	Output level [dB] without attenuator at Z_{out} = 600Ω
HFSRL	3 F F F 3 C Ø Ø	1 1 1 1 Ø	1 0 2 4	High frequency singing return loss	8.000	7.8 to 4000	7.8 Line sep.	4.5	8.523
SRL	3 B F F 3 8 Ø Ø	1 1 1 Ø Ø	1 0 2 4	Singing return loss	8.000	7.8 to 4000	7.8 Line sep.	4.5	10.123
ERL	3 7 F F 3 4 Ø Ø	1 1 Ø 1 Ø	1 0 2 4	Echo return loss	8.000	7.8 to 4000	7.8 Line sep.	4.5	10.391
Conventional Telephone Signal	3 3 F F 3 Ø Ø Ø	1 1 Ø Ø Ø	1 0 2 4	Convent. Telephone Signal	8.000	7.8 to 4000	7.8 Line sep.	4.5	10.302
	2 F F F		1 2 8						
GLZ 163	2 F 7 E 2 E Ø Ø	1 Ø 1 1 1	3 8 4	GLZ 163	8.000	3395.8	-	4.5	8.754
	2 D F F 2 D 8 Ø		1 2 8						
GLZ 134	2 D 7 E 2 C Ø Ø	1 Ø 1 1 Ø	3 8 4	GLZ 134	8.000	2791.7	-	4.5	8.754
	2 B F F 3 B 8 Ø		1 2 8						
GLZ 125	2 B 7 F 2 A Ø Ø	1 Ø 1 Ø 1	3 8 4	GLZ 125	8.000	2604.2	-	4.5	8.754
	2 9 F F 2 9 B Ø		1 2 8						
GLZ 86	2 9 7 F 2 8 Ø Ø	1 Ø 1 Ø Ø	3 8 4	GLZ 86	8.000	1791.7	-	4.5	8.754
	2 7 F F 2 7 B Ø		1 2 8						
GLZ 48	2 7 7 F 2 6 Ø Ø	1 Ø Ø 1 1	3 8 4	GLZ 48	8.000	1000.0	-	4.5	8.754
	2 5 F F 2 5 8 Ø		1 2 8						

GLZ 29	2 5 7 F 2 4 Ø Ø	1 Ø Ø 1 Ø	3 8 4	GLZ 29	8.000	604.2	-	4.5	8.754
	2 B F F 2 B Ø Ø		1 2 8						
GLZ 24	2 3 7 F 2 2 Ø Ø	1 Ø Ø 0 1	3 8 4	GLZ 24	8.000	500.0	-	4.5	8.754
	2 1 F F 2 1 8 Ø		1 2 8						
GLZ 14	2 1 7 F 2 Ø Ø Ø	1 Ø Ø Ø Ø	3 8 4	GLZ 14	8.000	291.7	-	4.5	8.754
Sine 2 kHz	1 F F F 1 E Ø Ø	Ø 1 1 1 1	5 1 2	Sine 2 kHz sub Harm.	8.000	2.000	-	1.76	13.012 dB
	1 D F F 1 C C 7		3 1 3						
Fast sine	1 C C 6 1 C Ø Ø	Ø 1 1 1 Ø	1 9 9	Fast sine	200.65	10 to 4.000	10	4.5	14.09 - SI
Fast noise	1 B F F 1 8 Ø Ø		1 0 2 4	Fast noise	8.000	350 to 550	7.8 Line sep.	1.76	6.555
	1 7 F F 1 6 3 D	Ø 1 1 Ø Ø	4 5 1						
4-tone	1 6 3 C 1 Ø Ø Ø	Ø 1 Ø Ø Ø	1 5 9 6	4-tone	8.000	8.57 to 1388		1.76	7.905
Noise	Ø F F F Ø 8 Ø Ø	Ø Ø 1 Ø Ø	2 0 4 8	Noise	8.000	350 to 550	3.9 Line sep.	1.76	6.486
	Ø 7 F F Ø 7 C F		4 9						20.11 - SI limited to approx. 15 dB in the output stage
Sine	Ø 7 C E Ø Ø Ø Ø	Ø Ø 0 Ø Ø	1 9 9 9	Out-of-band	200.65	100 to 72.000	100	none	
				In- band	20.065	10 to 4.000	10	4.5	14.09 - SI

Bild 9.1.1-2 Memory organisation at the main output

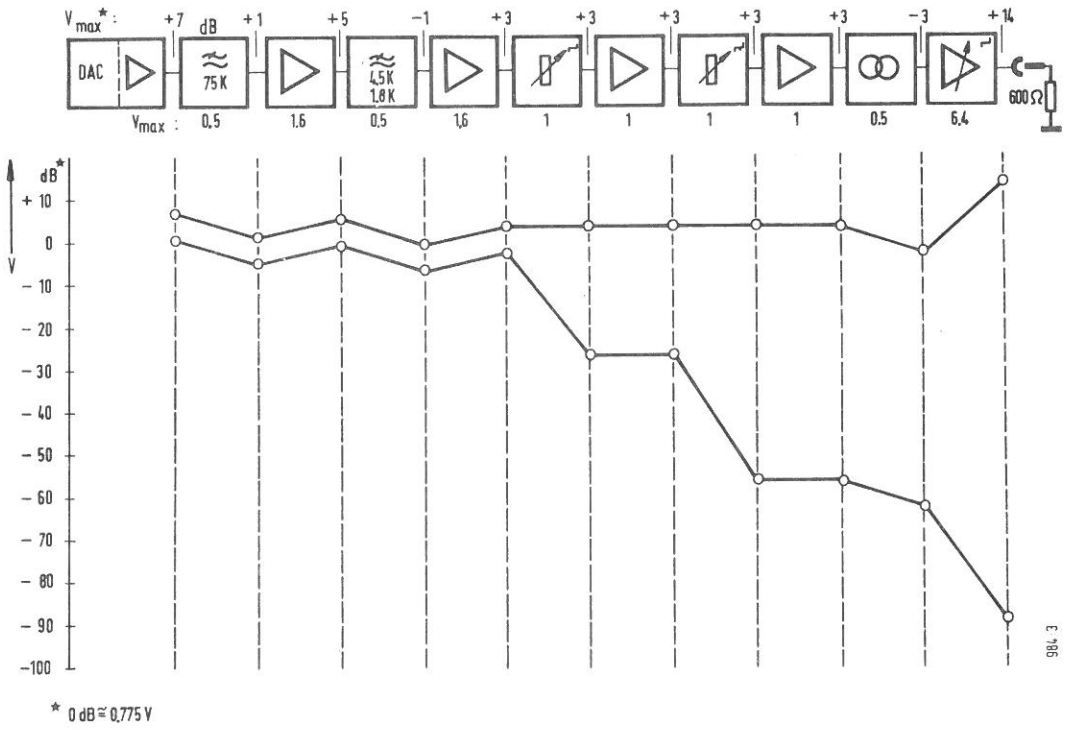


Figure 9.1.1-3 Level plan for the main output

To calibrate the analog receiver, a calibrated level is looped through the receiver via the line "cal. I".

Using the calibrated receiver, the actual attenuations produced by the coarse attenuator stages in the analog generator are measured and stored. When an attenuator setting is being calculated, it is these actual values that are used.

Auxiliary output:

The signals at this output have a fixed frequency (increment = 1). The number of samples used is 2048. A simple asynchronous counter is used to address the area in which the samples are stored. The counter increments the 11 address bits at a rate of 8 kHz, when it reaches 2047, the count starts again at 0000.
A data latch is not required for the auxiliary output, as the lowpass with its relative low cut-off frequency gives sufficient glitch suppression at the generator output. Incorrect addressing by the asynchronous counter is not possible when an overflow condition occurs.

The data is stored in octets in the EPROM. The data directly controls a DAC which also acts as a multiplier, multiplying the value of the signal by a factor which is equal to the applied reference. The reference can be adjusted in 1.5 dB steps by the logarithmic DAC.

The lowpass, which has a cutoff frequency of 845 Hz, suppresses the components whose frequencies are higher than that of the clock. The si losses that would occur are already compensated for in the samples.

An amplifier is used to carry out level matching for the unbalanced output connector, another amplifier is used for the balanced connector which is balanced by the output transformer.

Sample type	Address	Array length	Sampling frequency	Frequency	Line separation	Output level when terminated with 600 Ω
Sine 2 kHz	Ø F F F M to Ø 8 Ø Ø H	2 0 4 8	8 kHz	2 kHz	—	0 dB [-40 dB]
Noise	Ø 7 F F H to Ø Ø Ø Ø H	2 0 4 8	8 kHz	350 to 550 Hz	7.8 Hz	0 dB [-40 dB]

Figure 9.1.1-4 Memory organisation for the auxiliary output

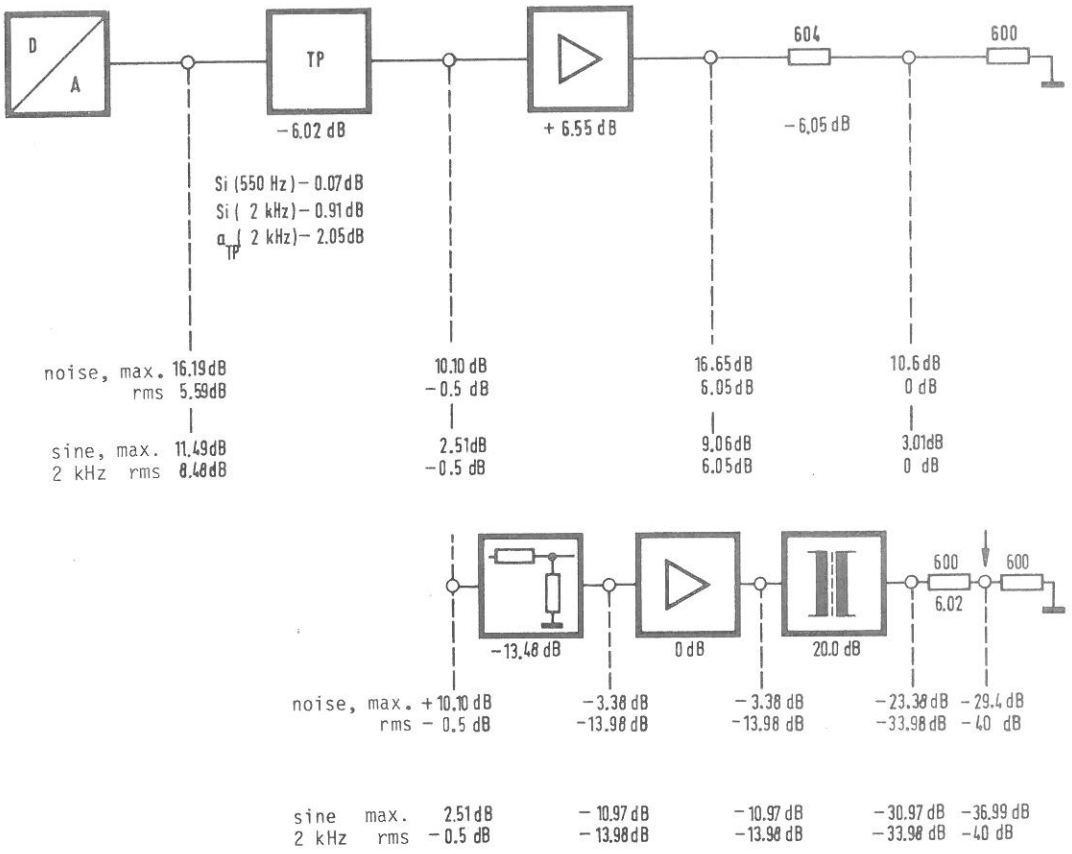


Figure 9.1.1-5 Level plan for the auxiliary output

9.1.1.2 Receive section - analog

Switching board [984-AF]

The RX input for 4-wire reception and the TX/RX transmit/receive line for 2-wire operation are connected to the switching board. Relays on this board are used to switch the signals to various functional blocks, the operating mode determines which blocks are used.

The input signals can be connected in the following ways:

- RX input signals to preliminary stage
- RX input signals via test bridge to preliminary stage

For 2-wire transmit and 2-wire receive, the switching board switches the TX/RX connector to transmit or receive. The complex 2-wire termination can also be switched in as a load.

It is also possible to make 2 calibration loops. Calibration loop, cal 1, connects the calibration signal "cal 1" to the preliminary stage. Calibration loop cal 2 connects the generator internally to the preliminary stage.

An overvoltage monitoring circuit checks the receive signal at the input, if necessary the signal path is interrupted by opening the input relay.

Preliminary stage [984-AE]

The input signal is passed from switching board [984-AF] to the preliminary stage. The preliminary provides dc decoupling for the input signal and performs preliminary level matching to the following stages.

Five different input impedances can be selected by relay on the primary side of the input transformer.

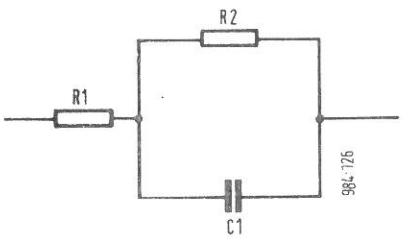
The impedances are: 600 Ω, 850 Ω, 900 Ω, complex impedance, $\geq$ 30 kΩ.

In the standard version, the complex impedance is realised by means of an RC parallel circuit containing the following components:

R1 = 220 Ω

R2 = 820 Ω

C1 = 115 nF.



At f = 1 kHz the magnitude of this impedance is 900 Ω.

An active input attenuator, which can be set to various attenuations between 0 dB and -18 dB, and two amplifier branches with an overall gain of 0 dB, 12 dB, 24 dB are used for level matching. A digital control section controls the attenuator (CPU 2/3).

Input [984-E]

The input 1 pcb contains various attenuators and an amplifier to carry out level matching to the following analog filter section. During automatic calibration, the reference attenuator is used as a standard to determine the correction factors for the attenuator. Digital control is used to set the attenuator coefficients. The control function is carried out via the interfaces of the test computer (CPU 2/3).

A comparator is used to monitor the level. When there is an excess level of 14.5 dB at the input of the output amplifier, the comparator sends an "overdrive" signal to the digital control.

Analog filter [984-I]

There are three types of filter on the analog filter board. These provide 3 signal paths for the three frequency bands, depending on the operating mode that has been selected.

The 4 kHz lowpass is an active filter (Bruton filter). It acts as an anti-aliasing filter for the following sampling circuits, it also produces the IMBAND signal.

The second signal path contains the passive 130 kHz filter.

The signal "input 2" is connected to a 4.6 kHz Cauer highpass. The signal is amplified by 63 dB and connected to a 130 kHz lowpass. The resulting frequency band is referred to as the A-band, 4.6 kHz to 72 kHz.

The IMBAND and A-BAND signals pass from the analog filter board to a decoupling transformer and are connected to the AF/VF connector, impedance 600 Ω.

ADU [984-K]/[984-AR]

The ADC board forms the interface between the circuit performing analog signal processing and digital signal processing.

A sample and hold circuit samples the analog input signal IMBAND, the results are passed to an ADC. The sampling rate is 10 kHz for A-A measurements, if digital signal processing is involved, e.g. A-D, the sampling rate is reduced to 8 kHz.

Another way of processing the signal is to take samples at random time intervals in the frequency range 20 Hz to 72 kHz (band limit at approx. 130 kHz). This prevents errors due to an insufficient sampling rate.

The digital word representing the sample (16 bits) passes through an output port to a block where signal processing is carried out (clock filter [984-L]).

Before reaching the sample and hold circuit, the ABAND signal is passed through an rms rectifier. Rectification takes place before sampling because the sample and hold module is not able to handle input frequencies higher than 80 kHz. The output of the rms rectifier is monitored by a level comparator.

9.1.2 FUNCTIONAL DESCRIPTION OF THE DIGITAL SECTION

9.1.2.1 PCM-30 generator/receiver

PCM-30 generator [984-T]

The PCM-30 generator simulates the send-side equipment of a PCM-30 system.
In the PCM-30 system, the PCM-30 send-unit is that group of circuits that interleaves thirty 64 kbit/s channels to give one 2048 kbit/s channel. This unit also inserts the alarm words, the alignment words and signalling into the frame.

The generator contains time channel and frame control circuits. Channel information, i.e. the information to be carried by a specific channel is passed to the PCM-30 generator by the PDG-64 unit [984-H] or is provided by an external source.
Analog signals can also be input via connector Bu 33, they are coded in an appropriate manner.
The channel information comprises digital samples representing the following signal types:

Sine signals
Noise
GLZ (test signal for group delay measurements using a modulation frequency of 41.66 Hz or 83.33 Hz)
Four-tone (four signals with the same level and frequencies of 857 Hz, 862 Hz, 1 373 Hz and 1388 Hz)

The PCM coder at the output can handle NRZ, AMI and HDB3 codes (switch-selectable). The 2048 kHz send system clock is provided for the PCM-30 clock circuit [984-V].

A parallel data stream from the PCM-30 receiver is fed to the PCM-30 generator, so that the received data can be looped through to the generator.
The following abbreviations are used for the frame words in the block diagram:
Free channel:
TX channel: transmit channel or selected channel
TS 16 FRØ: time slot 16 in frame 0 = multiframe synchronisation word
TS 16 FR 1...15: time slot 16 in frames 1 to 15 contains the signalling for channels
1 + 16
or 2 + 17
15 + 30
FAS: Frame alignment signal
NOT FAS: NOT frame alignment signal

PCM-30 receiver [984-U]

A digital signal receiver is required to carry out measurements on the send sections of PCM-30 equipment.

The PCM-30 receiver produces thirty 64 kbit/s data streams for the 2048 kbit/s data stream.

At the input, AMI or HDB3 codes are converted to NRZ. Synchronisation then takes place. The reference clock signal of 2048 kHz is supplied by the PCM-30 clock circuit [984-V]. This circuit recovers the clock signal from the received signal. The signal is tapped before it reaches the PCM-30 receiver. The 8 kHz FR clock can be applied externally to induce synchronisation.

After synchronisation, the serial signal is converted into a parallel signal. The NOT FAS, FAS and signalling words are decided in their parallel form and shown by means of an octet display on the front panel (selection and operating menu).
The channel signal, which has been separated by filtering, is fed into a parallel/serial converter, giving a 64 kbit/s data stream. This signal is the receiver signal for the various channels. This signal is either connected to the I/O interface or to the "PDA" (single channel receiver). The PCM-4 uses software to realise this function.

PCM-30 output [984-S]/PCM-30 input [984-R]

Both these boards match the voltage levels of the internal PCM circuits (PCM-30 generator, PCM-30 receiver) to the PCM power levels. The PCM signal level is 2.37 V into 75 Ω for balanced signals, and ± 3 V into 120 Ω for balanced signals.

The send signal and the clock signal are both converted to standard PCM-30 levels by the PCM-30 output board. The input impedance and the output impedance are selectable, i.e. can be set to 120 Ω (balanced) or 75 Ω (unbalanced) by means of the operating menu.

PCM-30 clock circuit [984-V]

This circuit generates the 2048 kHz system clock.
This can be done in four ways:
1. Internal quartz oscillator
2. Clock recovery from the PCM receive signal
3. External clock input
4. External clock passed through PLL.

2048 kHz is the transmission speed for the PCM-30 system.

9.1.2.2 PDG-64 generator [984-H]

The PDG-64 carries out simulations on single PCM-30 channels and provides a 64 kbit/s data stream.

The send signal codes are samples from:
- sinusoidal signals
- Noise signals
- GLZ signals for group delay measurements (modulated frequency 41.66 Hz, 83.33 Hz)
- Four-tone signal (All four signals have the same level, frequencies of 857 Hz, 862 Hz, 1373 Hz, 1388 Hz)

The most important part of the PDG-64 is the signal sample memory for sine, noise, GLZ and four-tone signal samples.

The codewords are read out by means of an addressing circuit. An adder stage is used to add various factors to the code words to give the level setting.
The companding characteristics are taken into account in the A/μ block. Before the signal reaches the output of the PDG-64 generator, each even bit is inverted (the bits are assigned the numbers 1 to 8, so bits 2, 4, 6, 8 are inverted). The reason for this is that continuous sequences of low bits or high bits must be prevented. Such sequences occur in PCM systems when no signal is present.

9.1.2.3 Digital receiver

The PDA-64 block is used to analyse a single channel bit stream (64 kbit/s) from the PDG-64, from an external interface or from the PCM-30 receiver.

In the PCM-4, only software is used to realise the PDG-64 block. The 64 kbit/s signal from the signal sources mentioned above is fed to the clock filter [984-L] where the serial data stream is converted into words 16 bits wide. These words are then passed through a digital filter [984-F] and fed to the evaluation processor [984-M].

Clock filter [984-L]

The clock filter is connected to the parallel bus line between the ADC [984-K], [984-AR] and the digital filter [984-F]. The 16-bit word from the ADC is not affected by the clock filter, but is ORed and connected to an internal 16-bit data bus.

The 64 kbit/s data stream which is to be evaluated in serial form, passes from the PCM-30 receiver or the I/O interface to the clock filter circuit.

Serial/parallel conversion is carried out on the 64 kbit/s data stream, and a 16-bit data word is produced. This is fed to the second input of the OR circuit.

The clock signal (conversion signal) for the analog/digital converter on the ADC board is generated by a clock oscillator. Switchover to random sampling is possible. The sampling points are determined by reading suitable values from an EPROM.

There is also a decoder on the clock filter board. The decoder is used to convert the 64 kbit/s bit stream into an analog signal. The decoded analog signal is connected to connector [37] on the back panel of the instrument.

The digital filter [984-F] requires a reference clock to produce the various internal control clocks. This reference clock is generated on the clock filter board. One of two clock oscillators can be selected by means of switch S1.

1) Oscillator for the conversion signal
2) Oscillator which is synchronised to the 8 kHz signal from the PDG unit.

Digital filter [984-F]

The 16-bit data word is passed through the digital filter to produce band limiting or band selection.

The heart of the digital filter is the 16 x 16-bit multiplier with coefficient memory providing input and output buffering.

The clock circuit controls the filter. A clock memory is used to realise the clock circuit. There is a range of coefficients available for the multiplier. These are fed to the multiplier via the I/O interface and make it possible to realise a number of different filters. The coefficients are stored in a coefficient memory.

Evaluation computer [984-M]

The evaluation computer is the last element in the chain of components responsible for digital signal processing. The computer evaluates the input signals that originate from the ADC (analog section) or the digital receiver, or that have passed through the digital filter. The results are passed on to the test computer (CPU 2/3). The 16-bit 8086 CPU is the main component of the evaluation processor. The test computer unit is connected to the evaluation processor by means of the I/O data bus and the I/O address bus. It has an autonomous RAM and EPROM for the evaluation program and the intermediate results (rms, average etc.).

The control clock is supplied by the clock memory circuit of the digital filter.

9.1.3 SIGNALLING DISTORTION

Signalling information for PCM-30 systems can be tapped at the input or output of the system. Delays between the input signal and the output signal change the duty cycle.

Using [A-D], [D-A] and [D-D] measurements, this circuit can be used to measure the difference in the duty cycle of a rectangular pulse as it passes through the system.
There are two back-panel connectors for the input signal and the output signal and these are used to perform analog measurements. The digital input signal and the digital output signal are fed to the PCM-30 receive unit and the PCM-30 send unit by internal means. The signalling words in the 16th time slot of the frame in question are examined or altered. The test computer, which is connected by means of an I/O interface, controls this circuit. The computer unit is responsible for generating the pulses that are sent and for evaluating the received signals.

A comparator section is located at the receive-side input, and checks the make and break resistance of the device under test (make < 300 Ω, break > 20 kΩ).

9.1.4 CONTROL AND OPERATION

The control circuits for the PCM-4 can be divided into two groups, "internal control" and "external control".
The internal control system is hierarchic and comprises a master processor and two slaves. This system deals with the screen display and the test sequence.

The external control system comprises the keyboard and the control facility via the <IEC> bus. The master computer (CPU 2A/1) operates either the operation board (keyboard) or the IEC bus interface (depends on the instrument operating mode).

The slave computers and the keyboard can send interrupt signals requesting service to the master computer by means of the interrupt logic on coupling board 2. The master processor has direct access to the real-time clock on coupling board 2.

The master computer sends instructions to the slave computers to produce the display and control the test sequence, these instructions are transferred via coupling board 1. This board is used to connect either the test computer (CPU-2/3) or the video computer (CPU-2A/2) to the master computer. Because of the way the circuit has been designed, it is not possible to effect direct coupling or direct data exchange between the test computer and the video computer.
A memory expansion for the video computer has also been accommodated on coupling board 1. The test computer controls the complete test sequence. The test computer's I/O data bus and I/O address bus are therefore connected to all test circuits which have to be controlled. To select each test assembly and to handle the acknowledgements from the test subassemblies, the test processor uses coupling board 3 which has a decoding circuit and interrupt logic.

The video processor is responsible for the display, i.e. showing results and menus on the screen. The video control board 962/01 is supplied with video data by the video processor.
The video control board is used to generate composite video signals. The deflection circuits and the HT circuits are to be found on the monitor board (980/01).

9.2 SUBASSEMBLY CIRCUIT DESCRIPTION

9.2.1 MOTHER BOARD (50)

The mother board is a multilayer board. Fig. 9.2.1-2 is a cross section showing:

- Connection points for the supply voltages
- Wire-links for supplying battery power to the CPU board.
  The signal "no arithmetic processor" for CPU-2A/1 can be generated with the wire-link H-G.

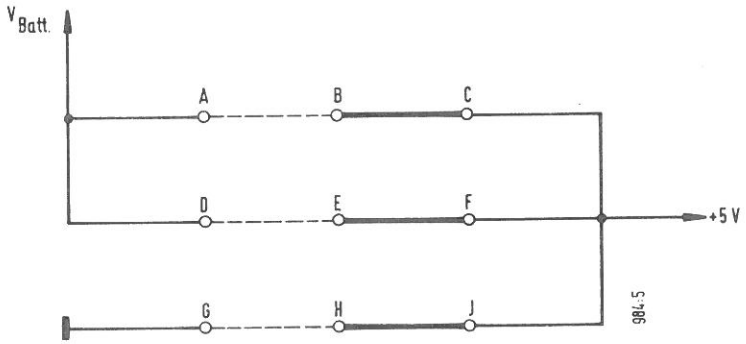


Figure 9.2.1-1 Normal wire-link assignment for back-up battery mode

Point B: connected to 29c on CPU-2A/2 (video computer)
Point E: connected to 29c on CPU-2/3 (test computer)
Point H: connected to 19c on CPU-2A/1 (master computer)

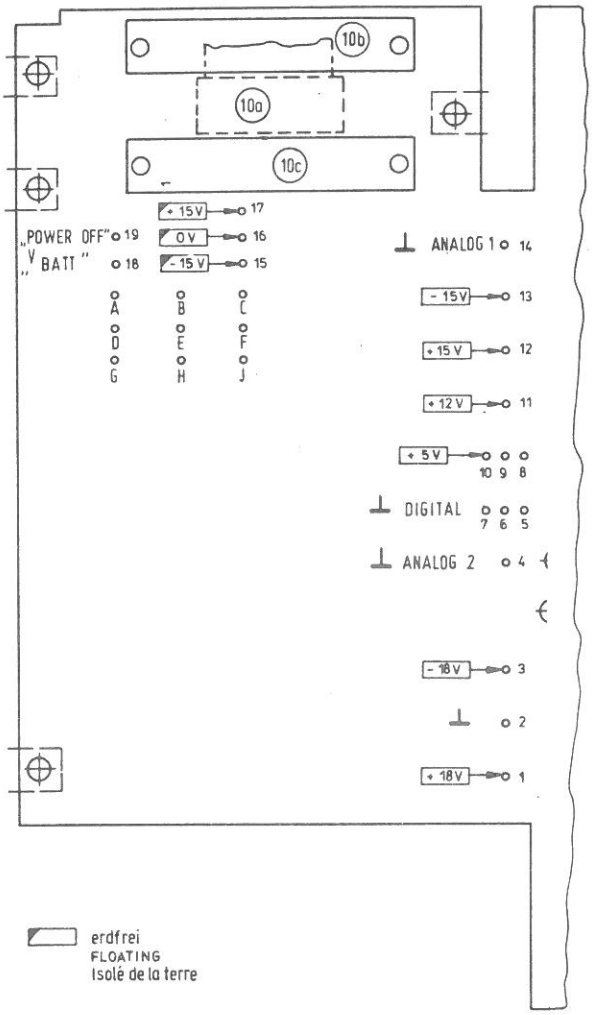


Figure 9.2.1-2 Section of mother board [984-A]

9.2.2 AUXILIARY MOTHER BOARD [984-B] (7)

Description using circuit diagram 984-7507

The auxiliary mother board is used to adapt the mother board (984-7000) to the test bridge (option [984-AH] and switching panel 984-7030. A 26 pole flat cable is used to connect the auxiliary mother board to the switching panel.

Two voltage regulators (UA7812 IC 1 and UA7912 IC 2) produce voltages of +12 V and -12 V for the test bridge and the switching panels.

9.2.3 OPERATION [984-C] (28)

Description using circuit diagram 984-7528

The following circuits are accommodated on the board:
- Key matrix
- LED multiplex matrix
- LED drivers for displaying the received code words

Key matrix

The "columns" of the key matrix are driven by output gate IC 10/IC 11. The "rows" can be interrogated via input gate IC 6/IC 7/1 by the processor.

In the idle state, all those "columns" that can accept a keystroke are set to low by the software (activated). The "rows" are set high by IC 14. The output of IC 39 is therefore low. If a key in an activated column is pressed, the "row" in question goes low and the output of IC 9 goes high. This process causes an interrupt to be triggered at the processor by the keyboard debounce circuit (coupling board 2). The processor then begins to search for the key that has been pressed. The processor sets all "columns" except one to high and interrogates the "rows" via the output gate. If all the "rows" were high, the key was not pressed in the activated "column". All the columns are searched in this way until the key that has been pressed is found.

If a "column" has already been set to high in the idle state (not activated), no interrupt is generated when a key in this column is pressed. The keystroke has no effect.

Diodes G1 09 to G1 16 and resistors IC 37 are there, should several keys in the same column be pressed. If these diodes were not there, the outputs of the column drivers would be short-circuited.

LED multiplex circuit

The LED matrix is 5 columns by 4 rows. IC 13 and IC 14 are the column information memories, these are filled by the µP. Using the clock from coupling board 2 (approx. 61 Hz), the stored information is fed cyclically to the memory drivers. At the same time, IC 12 switches through the relevant row drivers.

9.2.4 INPUT 1 [984-E] (4)

Description using circuit diagram 984-7504

The following stages are accommodated on the input 1 board [984-E]:

- Buffer stage [984-7047] (from series C ... transferred to input 1)
- Intermediate attenuator 1 ZT1
- Reference divider RT
- Intermediate attenuator 2 ZT2
- Intermediate amplifier 1 ZV1
- Intermediate amplifier 2 ZV2
- Output amplifier AV
- Overdrive evaluation
- Address decoding
- Pulse generation using monostables
- Voltage stabilisation

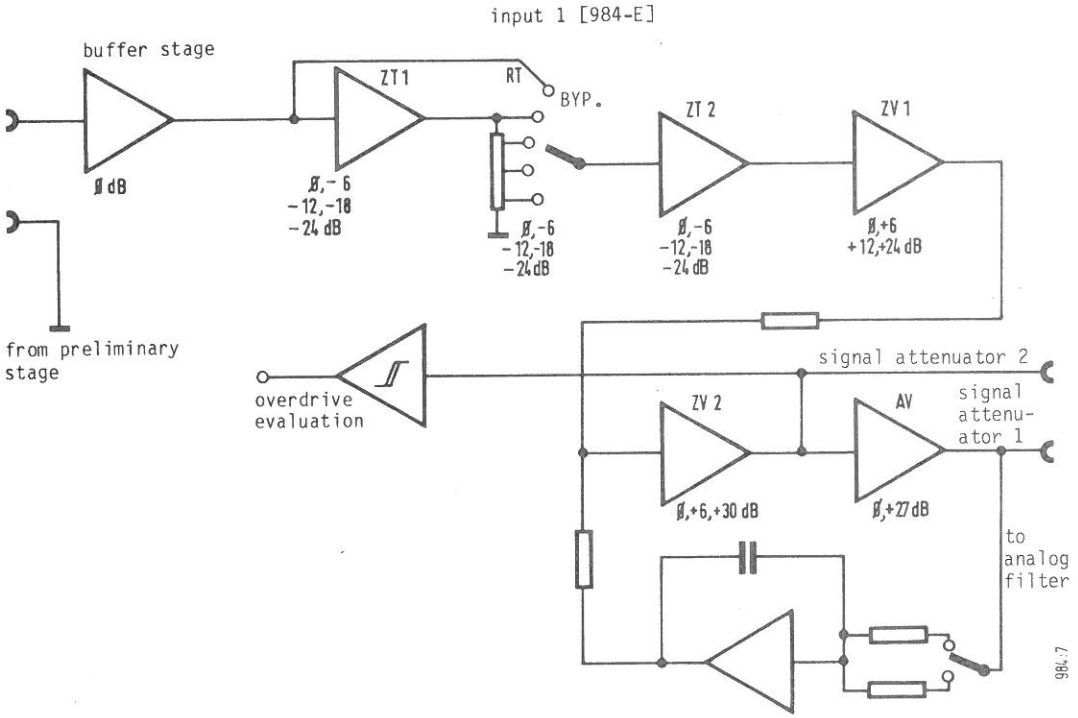


Figure 9.2.4-1 Block diagram of input 1 board

The following figure shows the relationship between the following as far as pulse generation goes, in a simplified form:

Input signal separation (circuit diagram)

Regulation time constants (preliminary stage and input 1)

Overdrive display (input 1)

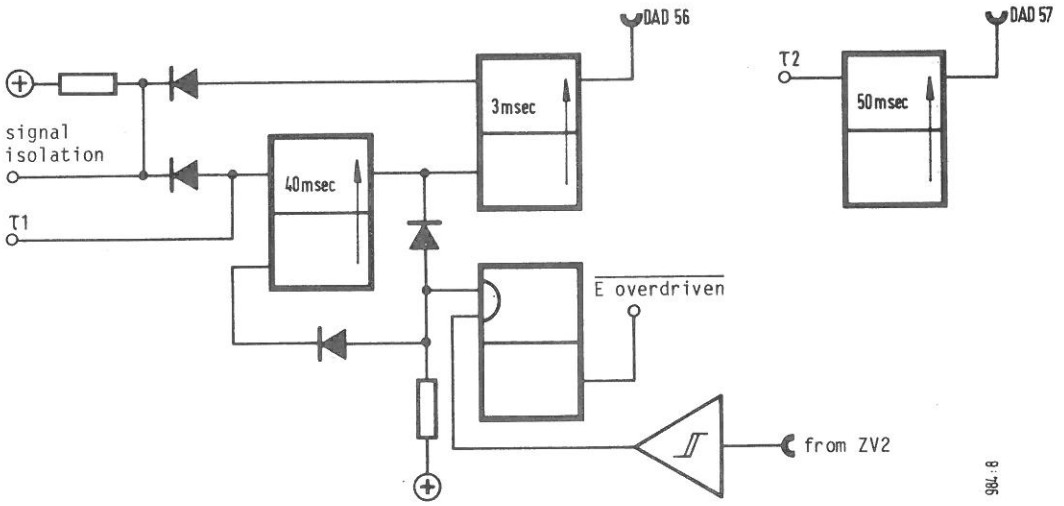


Figure 9.2.4-2 Pulse generation for offset regulation

The I/O address decoding for the whole analog-input section is also accommodated on the input-1 board (IC 26, IC 27). As the control function here is only concerned with output, the active low signal WEMP is used as an enable signal.

The decoded addresses DAD50 to DAD59 are either used directly as trigger pulses, or control the data transfer in the octal flip-flops (IC 6, IC 8, IC 10, IC 28).

The following gives the control address assignment:

DAD50	ZT1, RT
DAD51	Output impedance setting, E correction
DAD52	ET, EV, ZV1, ZV2
DAD53	test bridge
DAD54	test bridge
DAD55	switching panel
DAD56	signal isolation, τ1
DAD57	τ2
DAD58	reset/overdriven
DAD59	switching panel

The output of intermediate amplifier 2 (signal divider 2) has one branch going to the analog filter board (input, high-pass, out-of-band measurements) and another to the overdrive evaluation circuits (IC 32, IC 24, IC 25):

If the level is too high by +14.5 dB (comparator threshold), monostable IC 25 generates the active low pulse "E-overdriven".

A regulation circuit is used to provide offset correction for the whole circuit (includes the buffer stage from series C). Feedback is provided by IC 22 and IC 17. The time constant for the integrator stage is selectable (signal τ 2). Gain switch-over is program-controlled (cf preliminary stage). A pulse of length τ 2 = 50 ms is provided by monostable IC 4/1.

While $\tau 2$ is active, the output amplifier offset is eliminated using small time constants. The pulse length $\tau 2$ (50 ms) overlaps pulse length 1 (43 ms) and is also longer than the time taken to carry out signal separation and offset elimination in the preliminary stage.

This means that any jumps in the offset have largely died away before a measurement is started.

The input signal passes from the output of the preliminary stage to the buffer stage [984-7074], which decouples the regulation circuit in the preliminary stage from the intermediate amplifier ZT1 (offset adjustment with P3).

Input 1 board matches the input level to the following analog filter board by selecting various attenuator/amplifier ratios in six consecutive stages.
With the exception of the RT transformer reference divider, all level corrections are carried out by means of resistive dividers. The settings are determined by analog CMOS switches.

The following adjustments are available:
- Intermediate attenuator 1 (IC 1): 0 dB, -6 dB, -12 dB, -18 dB, -24 dB
- Reference attenuator (IC 3, IC 5): 0 dB, -6 dB, -12 dB, -18 dB, -24 dB
- Intermediate attenuator 2 (IC 7, IC 9): 0 dB, -6 dB, -12 dB, -18 dB, -24 dB
- Intermediate amplifier 1 (IC 11, IC 12): 0 dB, +6 dB, +12 dB, +24 dB
- Intermediate amplifier 2 (IC 13, IC 15): 0 dB, +6 dB, +30 dB
- Output amplifier 1 (IC 20, IC 21): 0 dB, +27 dB

The reference attenuator RT is of particular importance because of narrow tolerances. It is used to perform calibration. Corrections for the other attenuator/amplifier settings are referred to this attenuator and are stored in RAM.

---

* Series C and following transferred to input 1

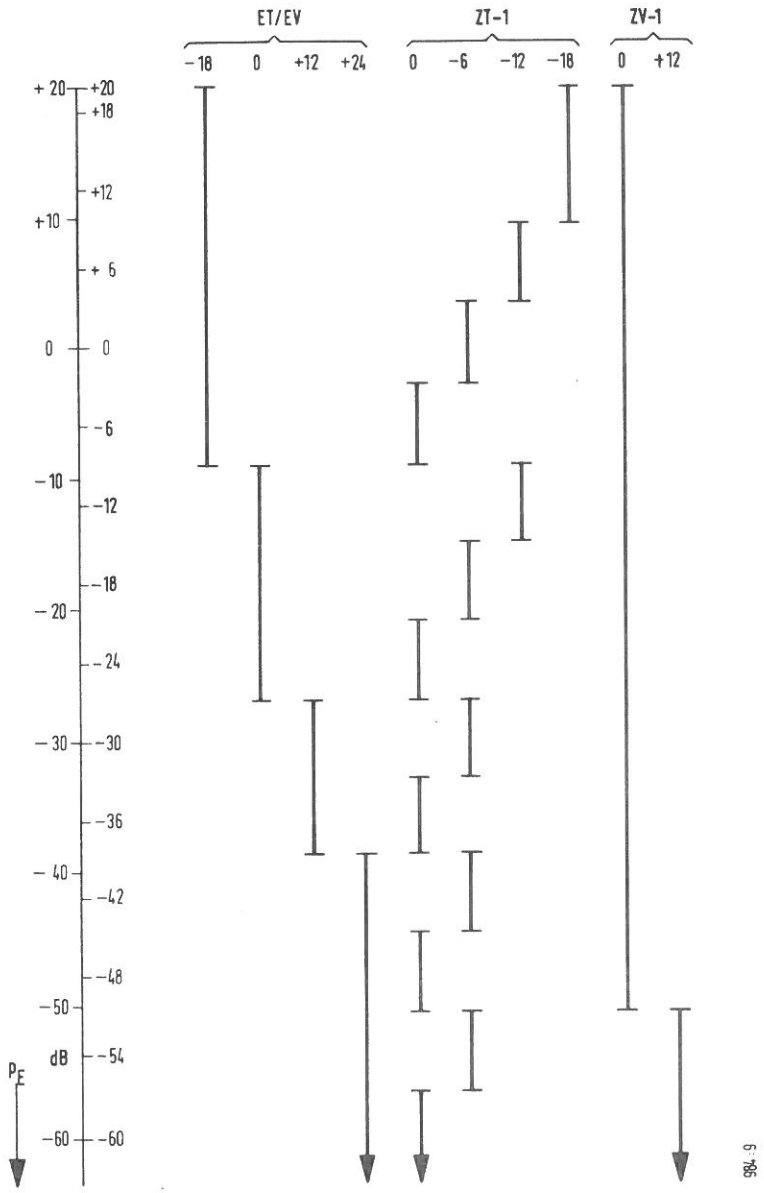


Figure 9.2.4-3 Attenuator control with attenuator setting "NORMAL"

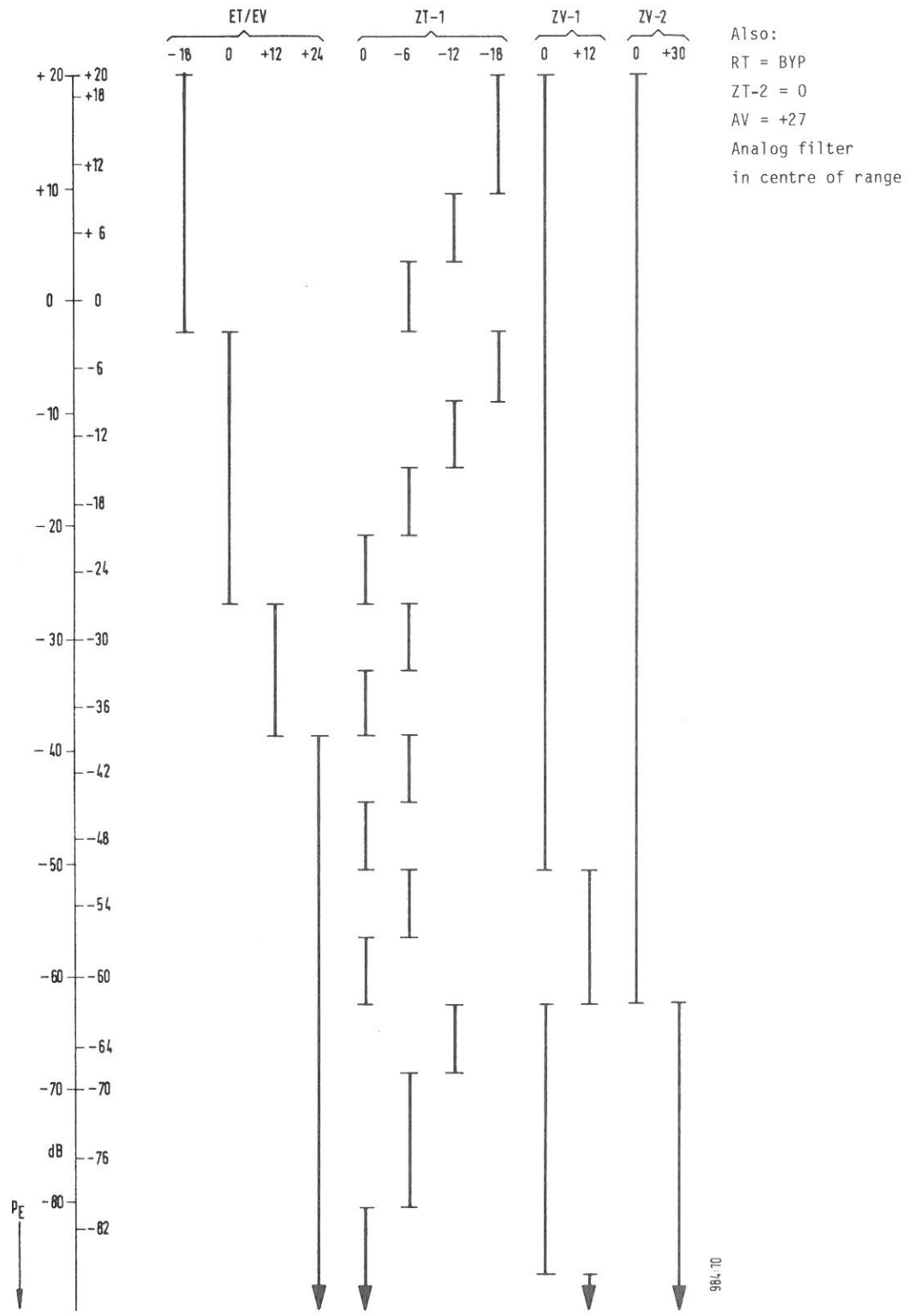


Figure 9.2.4-4 Attenuator control with attenuator setting "SENSITIVE"

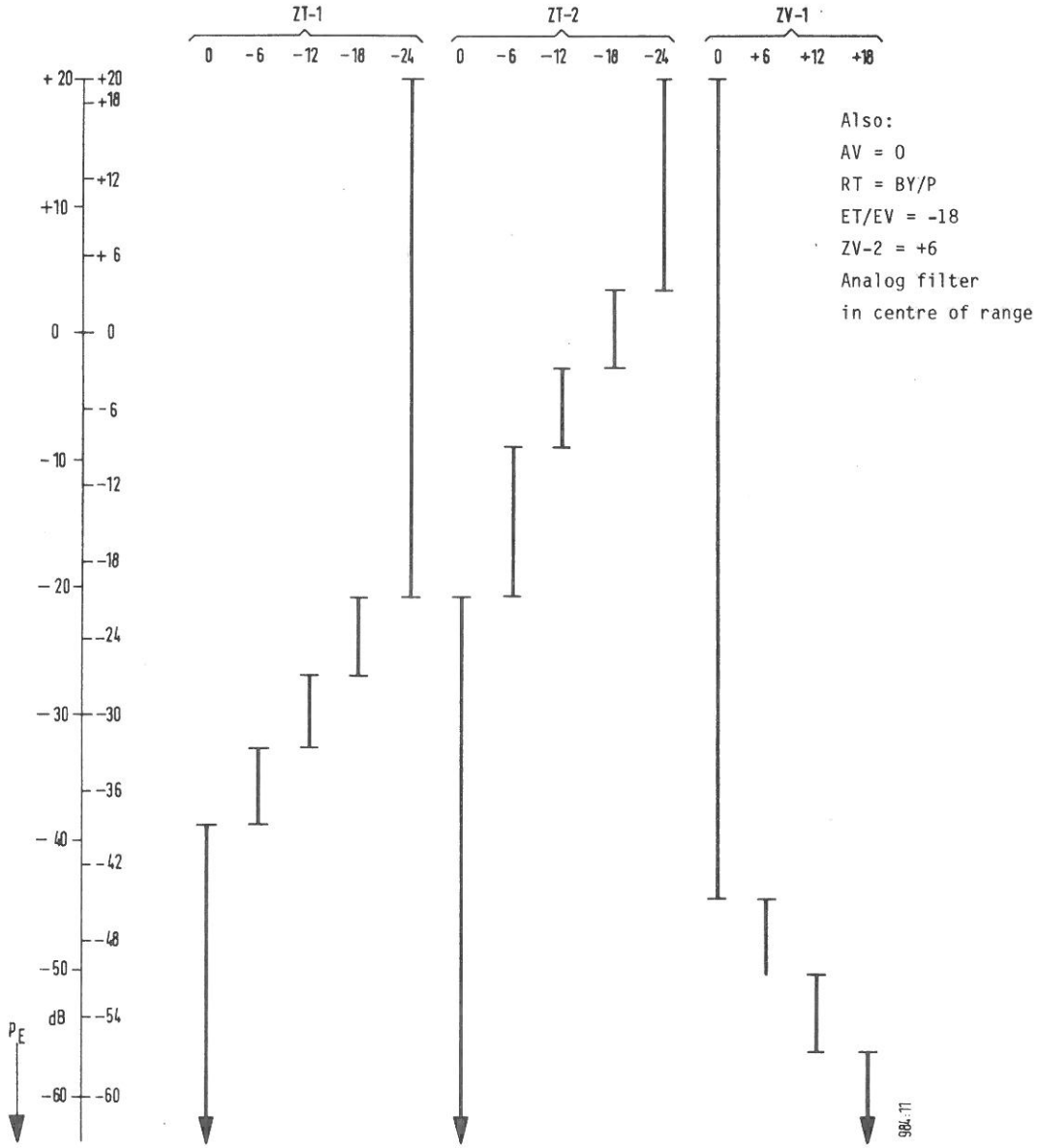


Figure 9.2.4-5 Attenuator control with "OUT-OF-BAND" attenuator setting

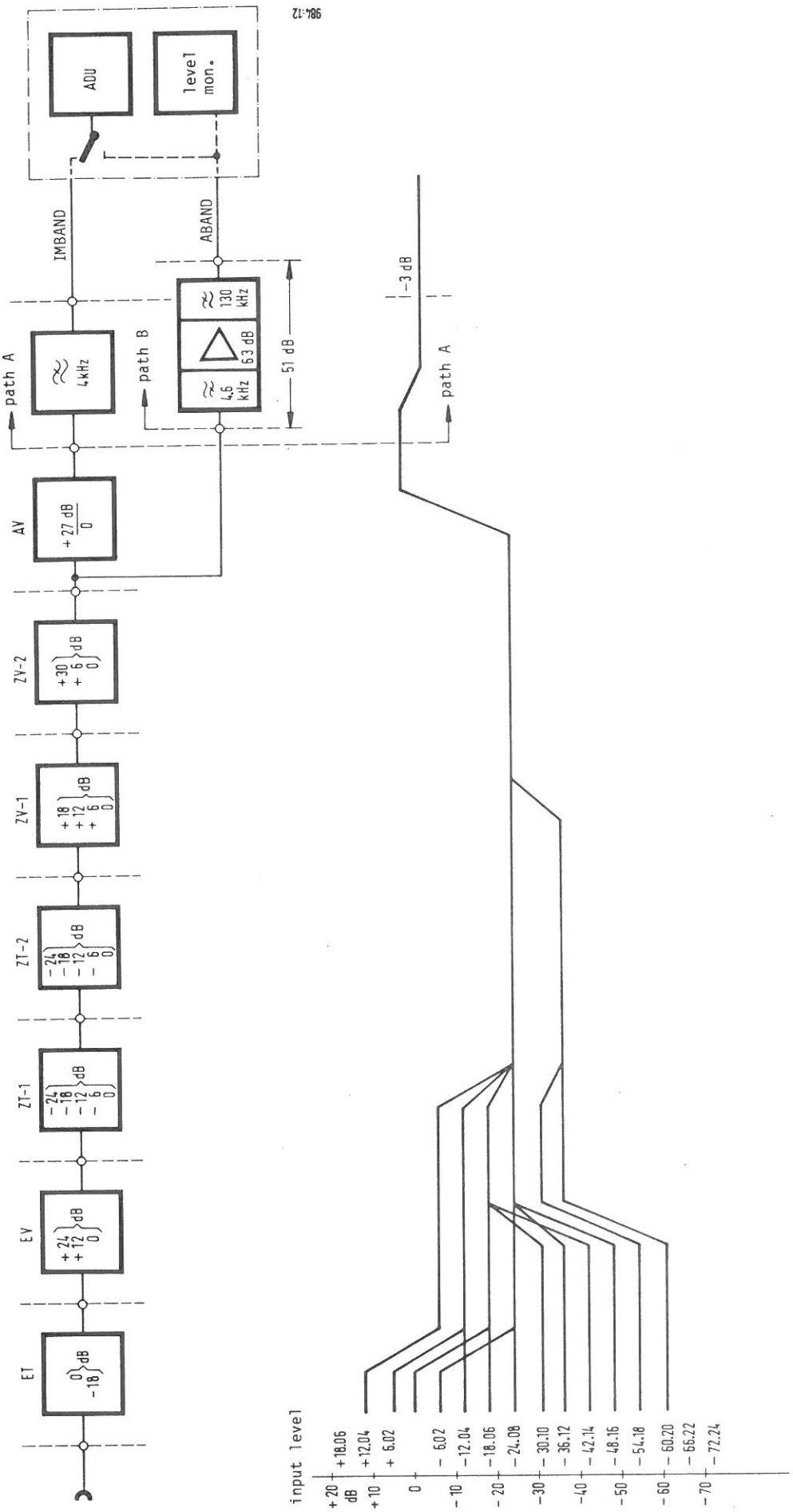


Figure 9.2.4-6a Example showing attenuator control: MODE A 11

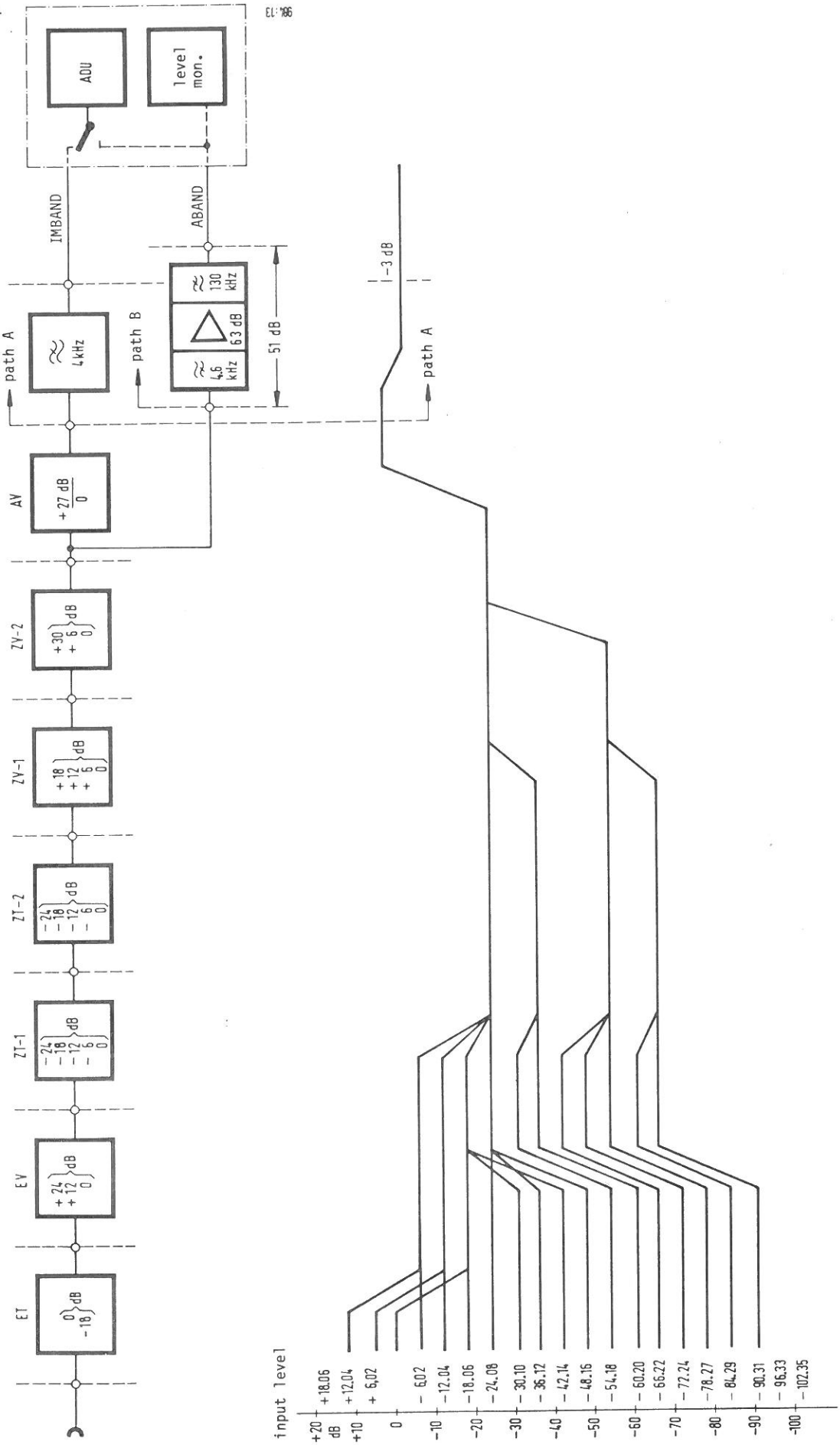


Figure 9.2.4-6b Example showing attenuator control: MODE A 61

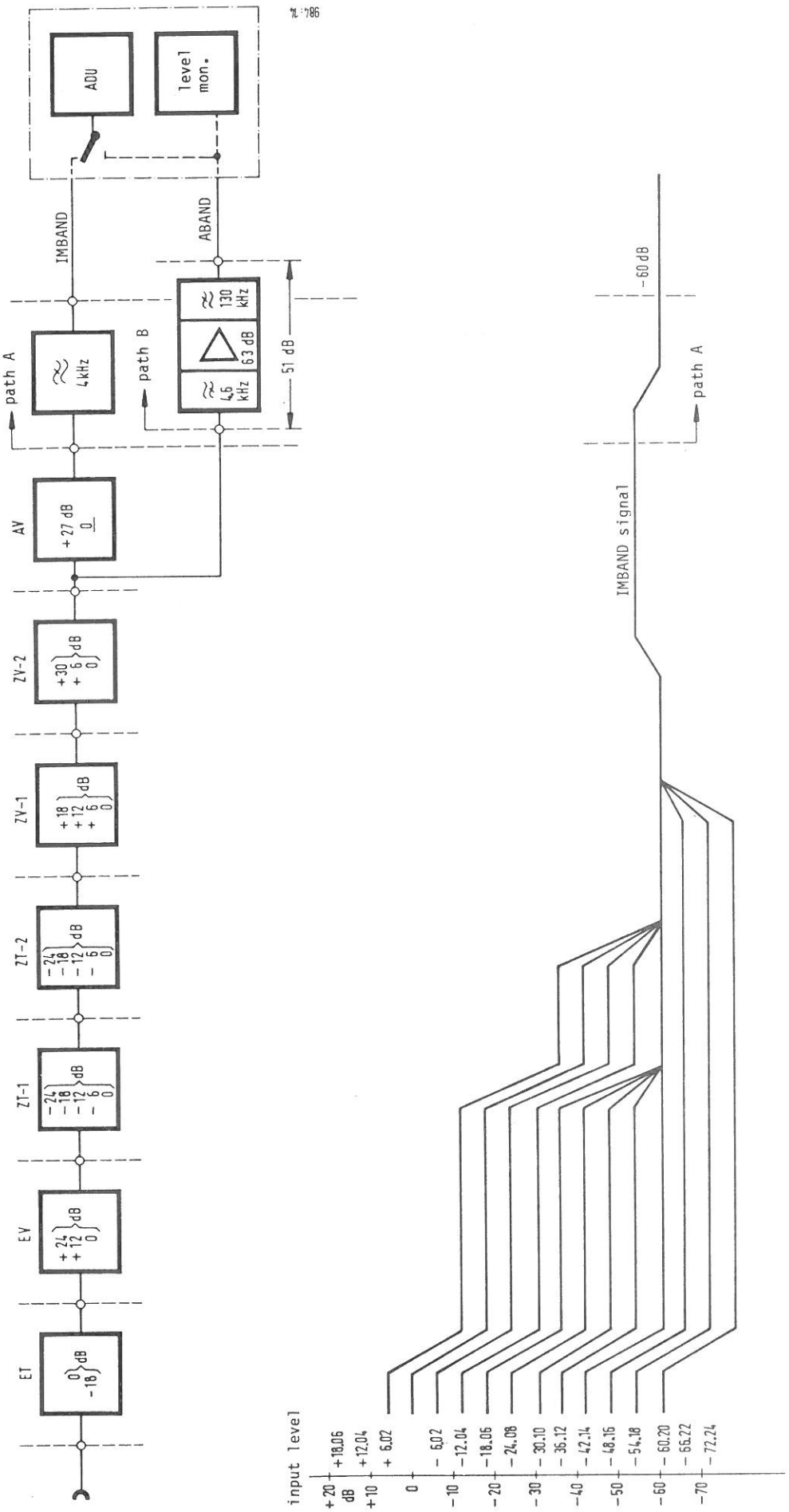


Figure 9.2.4-6c Example showing attenuator control: MODE A 81

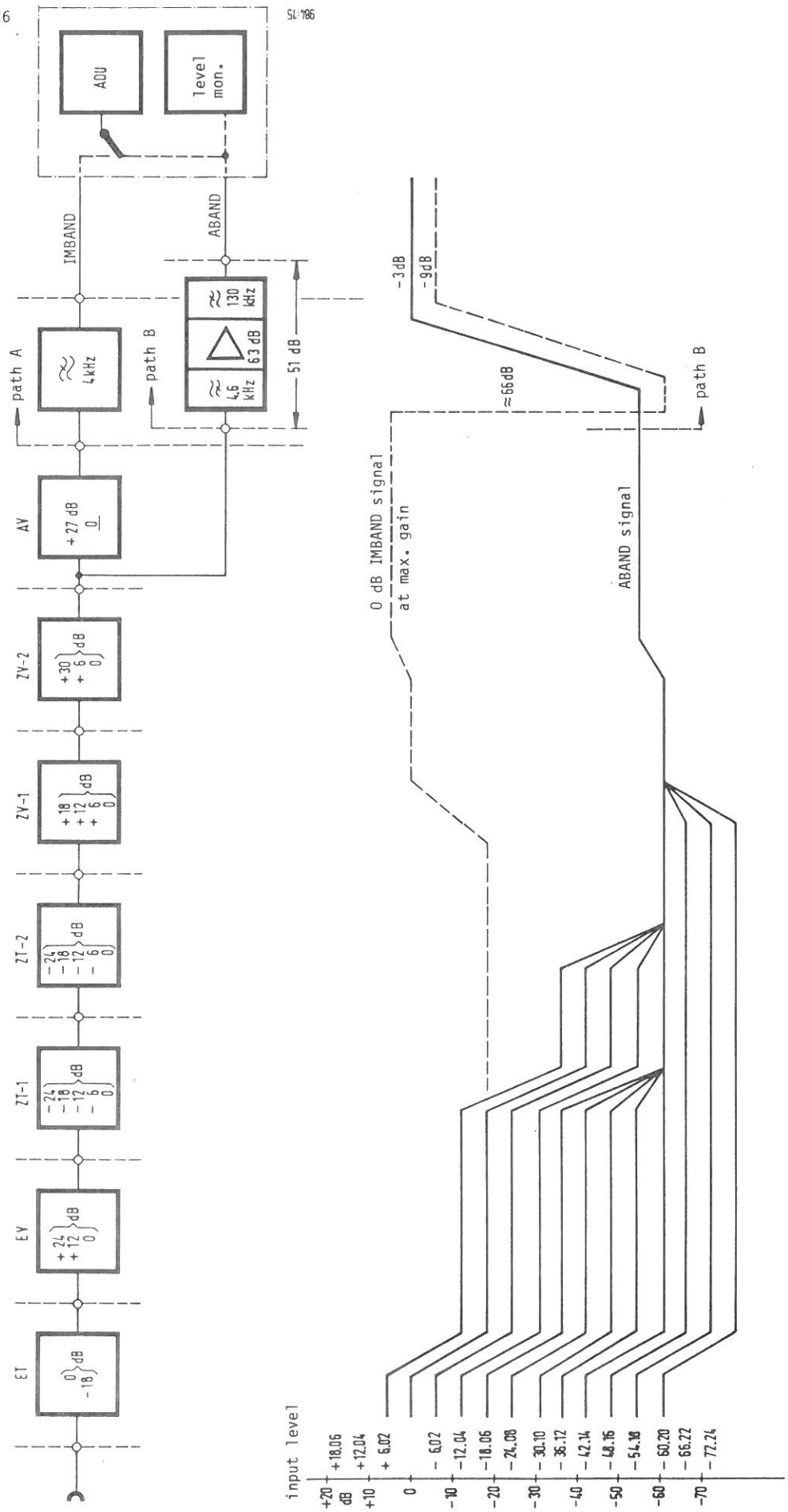


Figure 9.2.4-6d Example showing attenuator control: MODE A 82

9.2.5 CIRCUIT DESCRIPTION OF THE DIGITAL FILTER [984-F], (19)

Description using circuit diagram 984-7519

A 16-bit digital signal is fed to the input of the digital filter. When, say, a digital measurement is being made, this signal is transferred at the rate of 8 kHz to the input buffer (IC 49, IC 51) of the digital filter. The 16-bit digital signal is a linearised, extended 16-bit PCM word that has been encoded using the A-law or the μ-law.

When an analog measurement is being made, a 16-bit word is sent to the digital filter every 100 μs (sampling rate of 10 kHz) by the A/D converter.

When a digital measurement is being made, the 4.096 clock (point 29b) is fed to the 512:1 divider comprising IC 7 and IC 3. The 8 kHz signal that is produced at Pkt. 28b is fed to the CLOCK FILTER, this closes the PLL (see block diagram).

Inside the digital filter the input value is further processed using a high frequency clock.

A complete description of digital filter principles would be too long to be included in this service manual, if the user wants to know more about the theory of filters of this kind we suggest he consult the relevant literature.
Basically when the signal passes through a digital filter it is operated on by a series of adders, scalers and delay circuits, which, in mathematical terms can be thought of as digital transfer functions. The coefficients which are required to realise the various transfer functions are stored in a coefficient memory. The sequence of calculations is controlled by a 16 x 16 multiplier accumulator an a RAM.

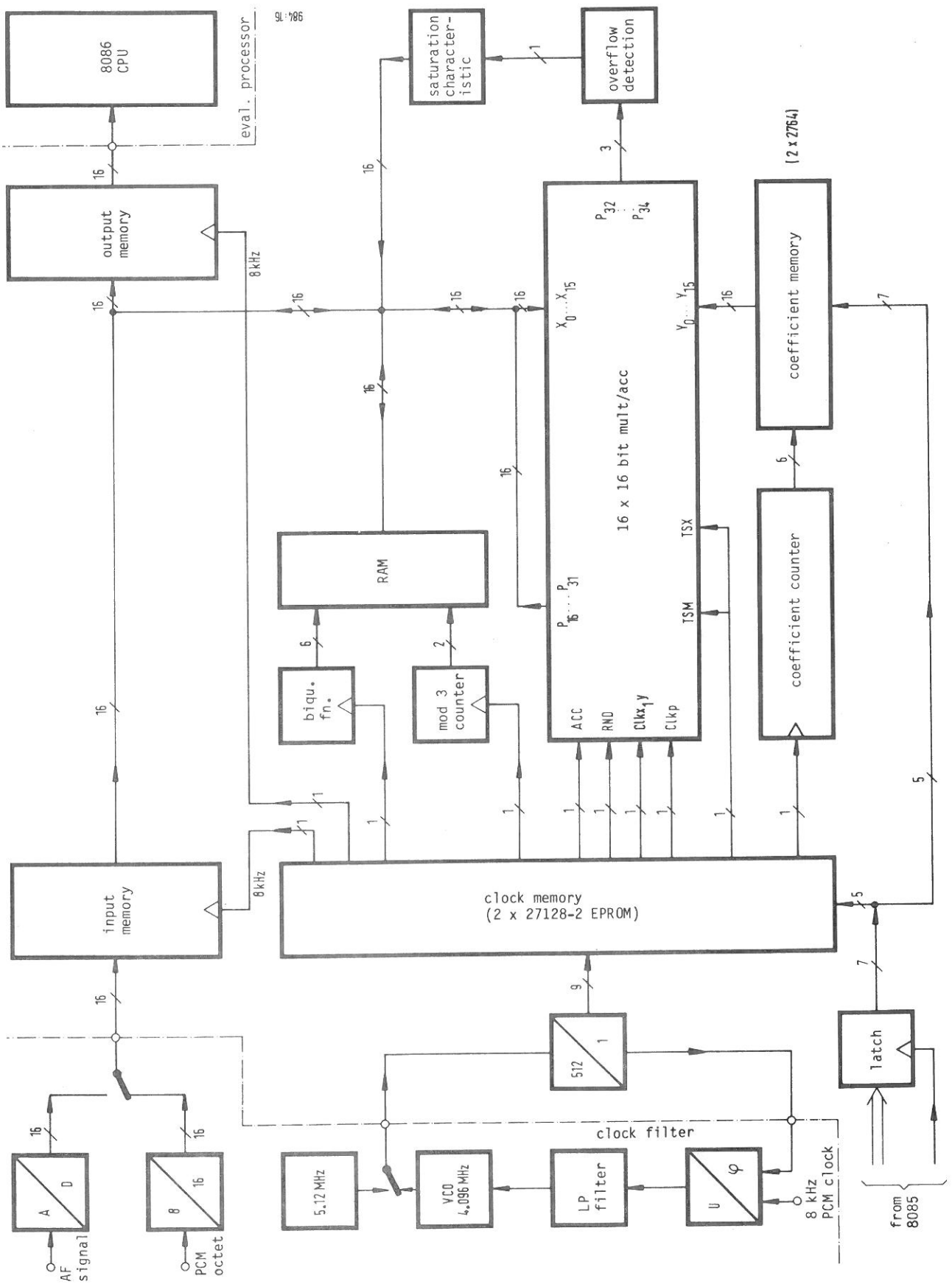
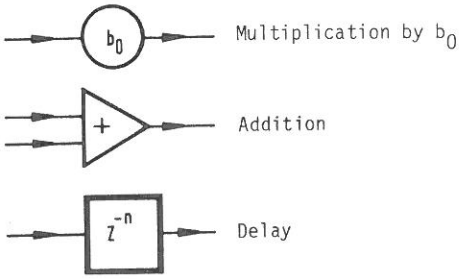


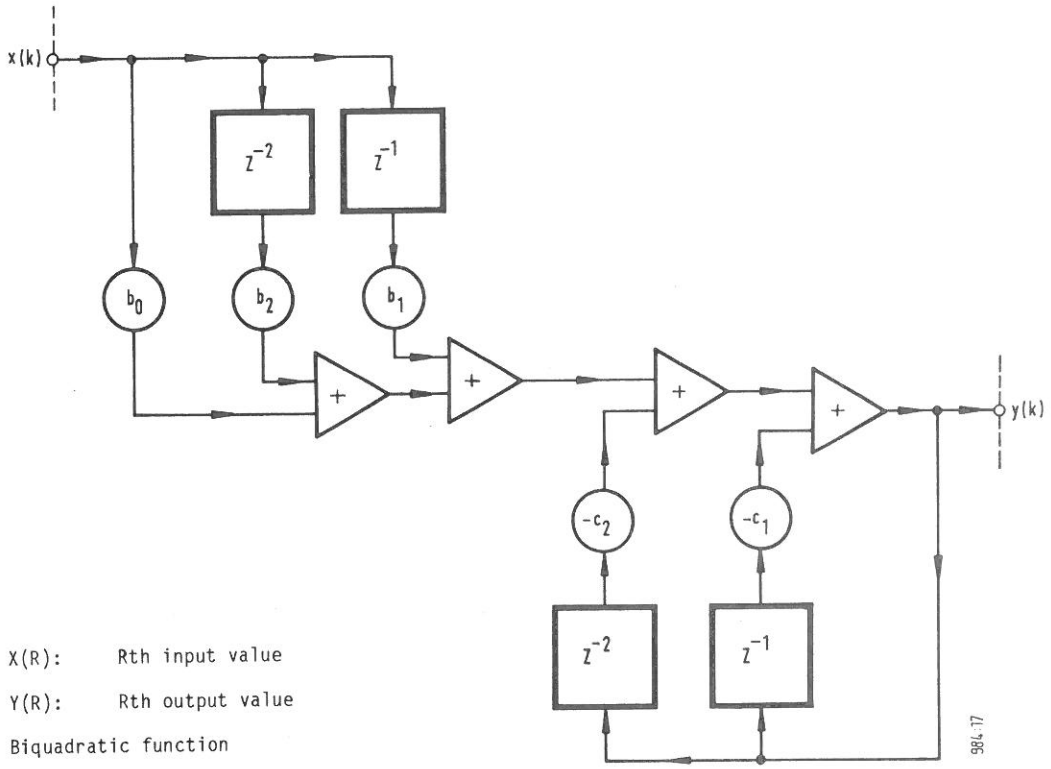
Figure 9.2.5-1 Block diagram of the digital filter

Between two samples there are 512 = 2 x 256 clock cycles available. During this interval of 512 clock cycles, two digital filters which are required for S/N measurements are realised. A filter for determining the signal component is realised during the first 256 cycles, a filter for determining the noise is realised in the course of the remaining 256 clock cycles.

"Double" filters are also realised when wideband, noise or selective filters are selected. The first filter is an all-pass that transfers the input signal to the evaluation processor, while the second filter realises the required transfer function.

When double filters of this kind are used, the input and output buffers of the digital filter are clocked at a rate of 16 kHz for digital measurements and at a rate of 20 kHz for analog measurements. The heart of the digital filter is a 16 x 16 multiplier/accumulator module (IC 29). This module processes the input and output values which are stored in RAM (IC 38, IC 40) using the following algorithm. The following definitions should be noted:





X(R): Rth input value

Y(R): Rth output value

Biquadratic function

$$Y(k) = b_0 \times X(k) + b_2 \times X(k-2) + b_1 \times X(k-1) - C_2 \times Y(k-2) - C_1 \times Y(k-1)$$

Figure 9.2.5-2 Hardware realisation of a digital filter, 1st canonic form, 2nd order

Up to 8 biquadratic functions can be processed with 256 clock cycles. Five multiplications and 4 additions are required for each biquadratic function. Coefficients ≥ 0.5 are split up into a series of coefficients each of which is < 0.5. This increases the number of multiplications. On average, 30 clock cycles are required to process a biquadratic function. A large part of this time is required for controlling the clock memory (IC 16, IC 17), the coefficient EPROM (IC 35, IC 41), the RAM memory (IC 38, IC 40) and the multiplier/accumulator module IC 29.

Eight clock cycles are needed to read in a sample and eight clock cycles are required to read out the filtered value.

This means that a total of 256 clock cycles are required to realise a filter. If the pseudorandom undersampling method is used for level measurements in the range 20 Hz to 72 kHz, the 16-bit input signal bypasses the actual digital filter via IC 52 and is fed into a 1:1 path which leads directly to the evaluation processor. This path can also be selected via VAR.MODE 3 (71).

The multiframe signals "data valid MSB" (Pkt. c19) and "data valid LSB" (Pkt. b27) are derived from the "start ABM" signal in this mode. The latter signal is generated in the CLOCK FILTER board the signal indicates the start of out-of-band measurements. An overdrive at outputs P_{31}, P_{32}, P_{33}, P_{34} of the multiplier/accumulator module can be detected and the saturation characteristics switched in via IC 45, IC 47.

The adder chain IC 28, IC 30, IC 32, IC 33 has a facility for reducing the 32-bit result of a 16 x 16 bit multiplication to 16 bits. At the present time this facility and the facility for randomly rounding off the result (using the random bit control line at Pkt. c16) are not used. The result is rounded off in the multiplier/accumulator module itself. This is done by means of the "RND" control line at IC 29, pin 54.

The various control signals for the RAM, the coefficient EPROM, the multiplier accumulator, the input buffer and the output buffer are derived from the clock memory EPROMs IC 16, IC 17. The latter IC are addressed using time multiplexing to give the required time of 195 ns which corresponds to the system clock of 5.12 MHz.

9.2.6 COUPLING BOARD [984-G] (26)

Description using circuit diagram 984-7526

The following circuits are accommodated on coupling board 1 [984-G]

- Data bus and address bus coupling from master processor CPU-2A/1 to test processor CPU-2/3 and video processor CPU-2A/2
- DMA control
- Memory expansion for CPU-2A/2
- Signal source

Data and address bus coupling

This processor interface connects the three CPU boards CPU-2A/1, CPU-2A/2, CPU-2/3. The signal names for CPU-2A/2 (video processor) contain an "S", those for the CPU-2/3 (test processor) an "M" to distinguish the various CPUs.

In order to access the memories of the test processor and the video-processor, the I/O data bus of the master processor has a bidirectional connection to the internal data lines of the slave processor via IC 9, 10, 12, 16, 20/1, 22, 23/1. The address lines are formed by storing the internal data lines of the slave processor as the most significant address byte by means of a latch (IC 24 for the test processor, IC 19 for the video processor). The I/O address lines of the master processor via IC 1 and IC 12/IC 16 (video processor) IC 23/2, IC 21/2 (test processor) form the least significant address byte. This means that the master processor can access all the memory addresses of the slave processor (Direct Memory Access, DMA):

DMA

Before DMA, the master stores the most significant address byte in output port IC 19 (IC 24). This is possible if SOD is low. This switches on the I/O decoder IC 13, IC 14, IC 15. At the same time the flip-flop IC 13/1, IC 18/1 changes state. The slave receives the *"HOLD" signal and clears its bus system (three state logic), it then acknowledges this state with *HDLA. Only when this line is high does the master start DMA.

To perform DMA, the master switches SOD high. Each time an I/O access is made, the drivers mentioned above become active, so allowing data exchange with the slave memory. The other ports are not affected because they only go into the active state when SOD is low.

To end DMA, the master sets the *HOLD signal to low using its I/O decoder. The slave has now regained control over its own bus system and operates independently from the master.

In order to force the slave to carry out a particular operation, the master can trigger a pulse on the SRST 7.5 (MRST 7.5) using its I/O decoder (slave interrupt). The same applies to the video processor and the test processor.

Memory expansion

A memory expansion comprising 48 k ROM and 8 k RAM for CPU-2A/2 is accommodated on the board. The address lines and the data lines of the video processor (CPU-2A/2) are connected to the coupling board.

Then memory modules are selected by means of decoder IC 28. The ROM address range is 0000 to BFFF, that of the RAMs is E000 to FFFF. As the memory area of the CPU board has the same address range, a bank switch over must take place before the memory expansion is accessed. This switchover is made by IC 37 and the following RS flip-flop IC 36/1, 36/3. The CPU of the video processor performs this switchover by means of an I/O write operation.

---

* = M or S

9.2.7 PDG-64 [984-H] (22)

Description using circuit diagram 984-7522

9.2.7.1 Function of the PDG-64

This plug-in board generates and feeds the signal which is selected in VAR.MODE 2 to the digital PCM-4 generator. The periodicity of the signal that is currently being sent is indicated by the signal designated "signal trigger" (Bu 1).

9.2.7.2 Signal memory

All signals (with the exception of 2(44), series A-D, 2(45) from series E and 2(63)) that can be selected in the VAR.MODE 2 are stored in various areas of the signal memories IC 13 and IC 14. Each of these memory areas contains several samples which have a maximum width of 14 bits. These are addressed at a rate of 8 kHz by the address circuit. The memory area is selected by means of IC 8, IC 9, IC 11 and IC 12.

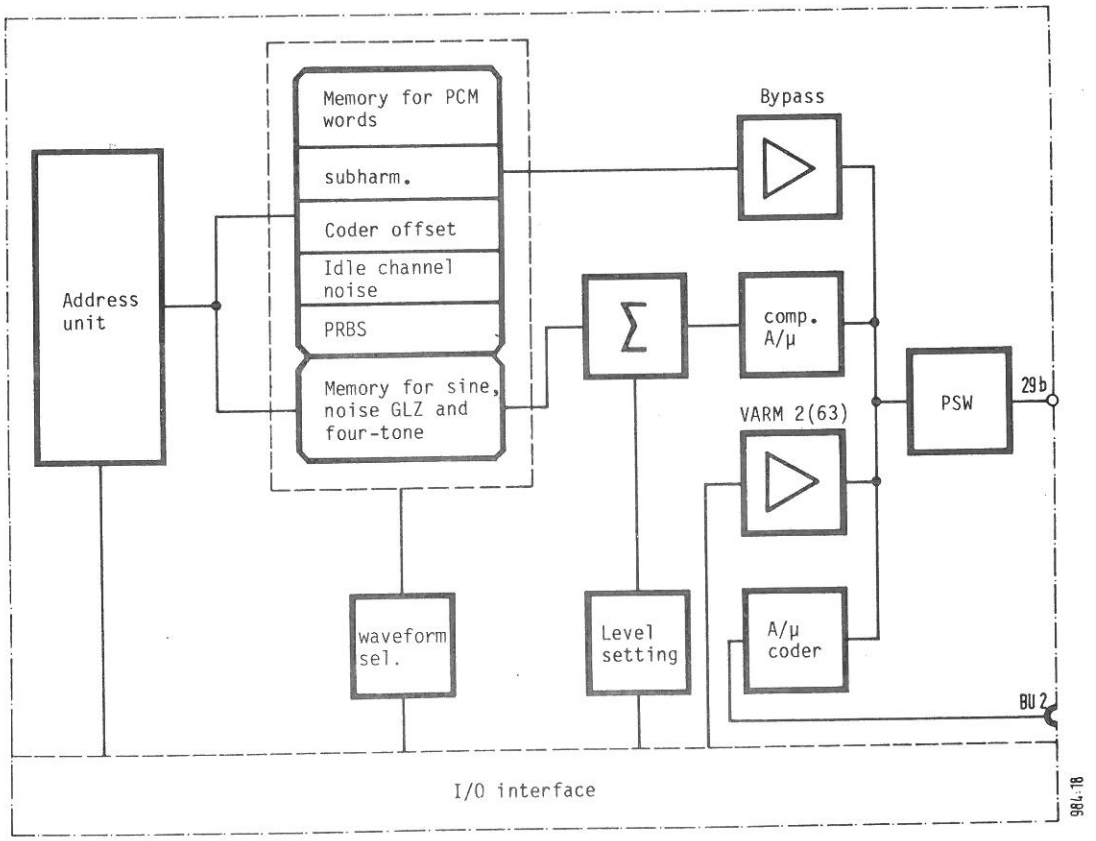


Figure 9.2.7-1 Block circuit diagram of the PDG-64

9.2.7.3 Signal paths to PSW (IC 31)

For signals whose transmission level can be selected using the keyboard

A 13-bit word corresponding to the log of the signal sample (no sign) passes through the adding stage IC 17 to IC 20 to the compander EPROM IC 23. The adders are used to add various correction factors to the sample word so that its level is the same as the level set using the keyboard.

After the sample has been converted by IC 23 according to the A-law or the μ-law, a 7-bit word (bit 2 to bit 8) is available for the PSW IC 31. The sign bit (bit 1, IC 31 pin 1) is fed directly via a by-pass from IC 13 pin 17.

A 64 kbit/s signal is output at pin 26b of the PDG-64.

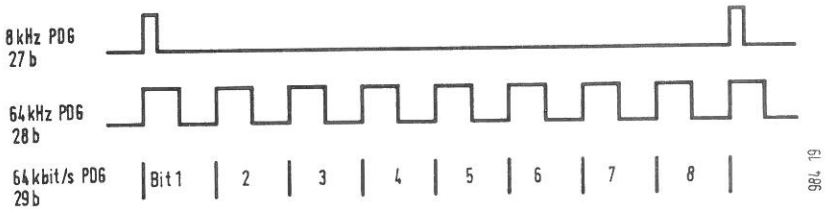


Figure 9.2.7-2 Timing diagram 1

PRBS signals and signals at the test level are fed directly to the PSW via a by-pass, the adders and the compander EPROM. Depending on the type of send signal that has been selected, IC 15 and IC 16 take the octet either from signal memory 1 (IC 13) or signal memory 2 (IC 14).

The octet which can be selected in the VAR.MODE 2 (63) passes via IC 24 to the parallel/series conversion circuits.

In codec mode VAR.MODE 2 (44) (series A to D, 2 (45) series E), IC 30 codes the instantaneous value of an analog signal at Bu 2 into an octet which is transferred to the PSW (IC 31) by IC 32. IC 30 uses a 8 kHz clock.

9.2.7.4 Principle of sinusoidal signal generation

Depending on the frequency that has been set, the address counter (IC 1) selects the required samples from the memory block for sinusoidal signals [VARM. 2 (11) or 2 (12)]. The samples may be read out consecutively or certain samples may be missed out to realise higher frequencies.

The samples that are stored correspond to one cycle of a sinusoidal signal at a particular frequency.

The number of samples that has to be stored is determined by the lowest frequency that is to be realised (10 Hz) and the sampling frequency.

$$\text{No. of samples} = \frac{\frac{1\,s}{10}}{\frac{1\,s}{8 \times 10^3}} = \frac{0{,}1\,s}{125\,\mu s} = 800 = n$$

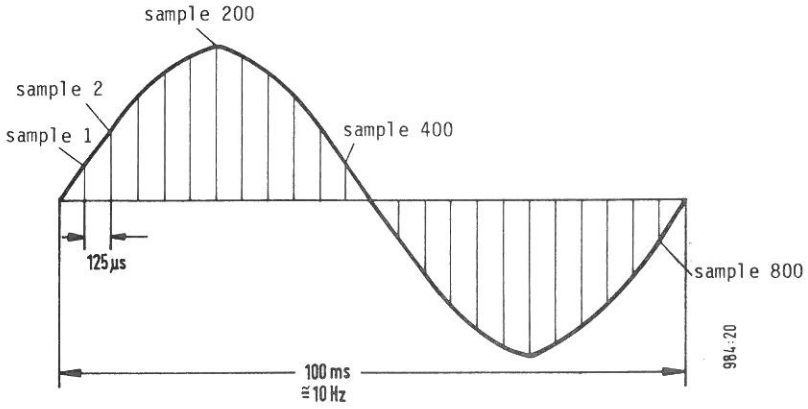


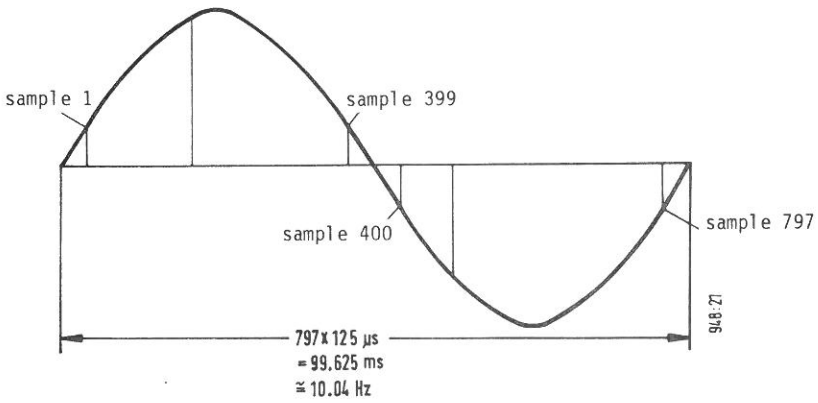
Figure 9.2.7-3 The sampling procedure

By selecting every mth sample, harmonics of the 10 Hz fundamental are produced.

$$f = \frac{8000\ Hz}{800} \times m$$

m = 1 to 400

In VAR.MODE 2 (11) and 2 (12) n = 797 (prime number) and n = 97 (prime number) samples are used. As the number of samples is prime this means that n samples must be taken before a value is repeated.



The lowest frequency in VAR.MODE 2 (11) is 10.04 Hz. The lowest frequency is given by the following formula:

$$f = \frac{8\ kHz}{797} \quad \text{step width}$$

When the maximum step width is selected (398) the frequency is 3 995 Hz

Figure 9.2.7-4 Principle of sampling (VAR.MODE 2 <11>)

9.2.7.5 Reading out the samples

"Timing 2" shows three samples being read out (addresses 0, 1 and 2).

Clock 1 connects the signal memory and the compander PROM to the appropriate bus systems. The clock rate is 8 kHz, the trailing edge of the clock sets the address counter to the next address.

"OVERFLOW" indicates that all available samples have been read out and that a new address cycle is being started.

The signal trigger (Bu 1) indicates bit 1 of the first octet.

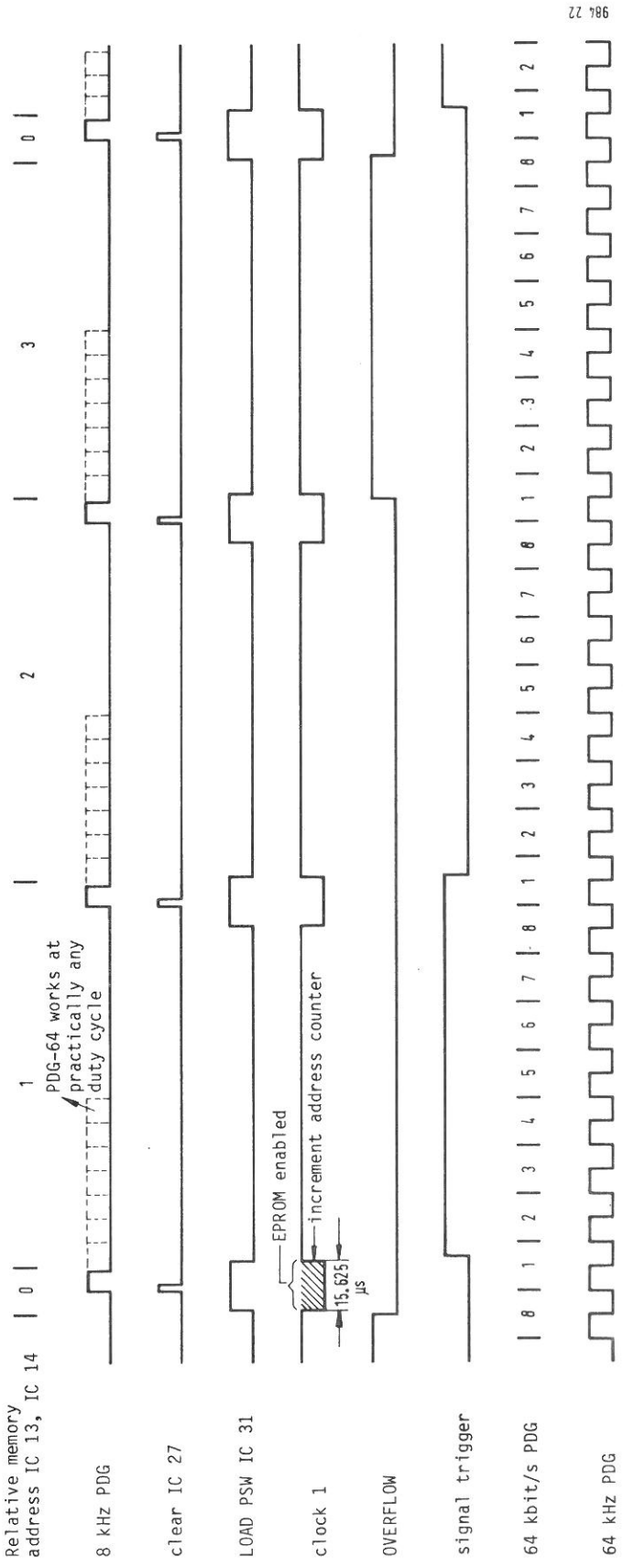
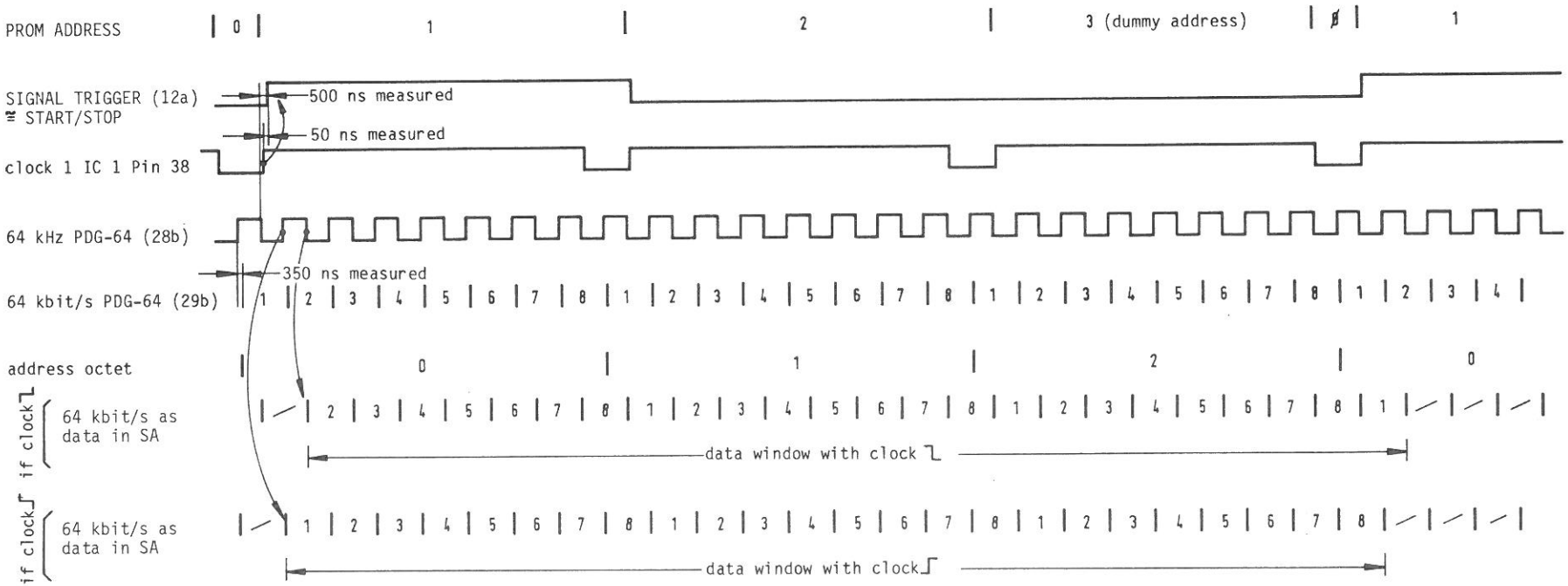
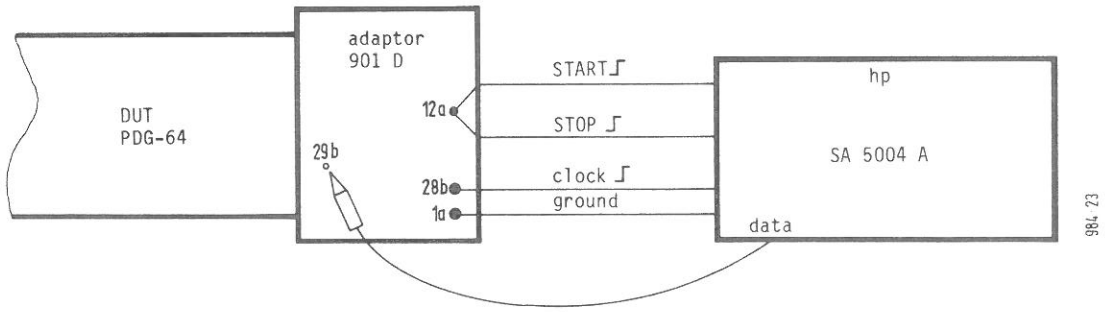


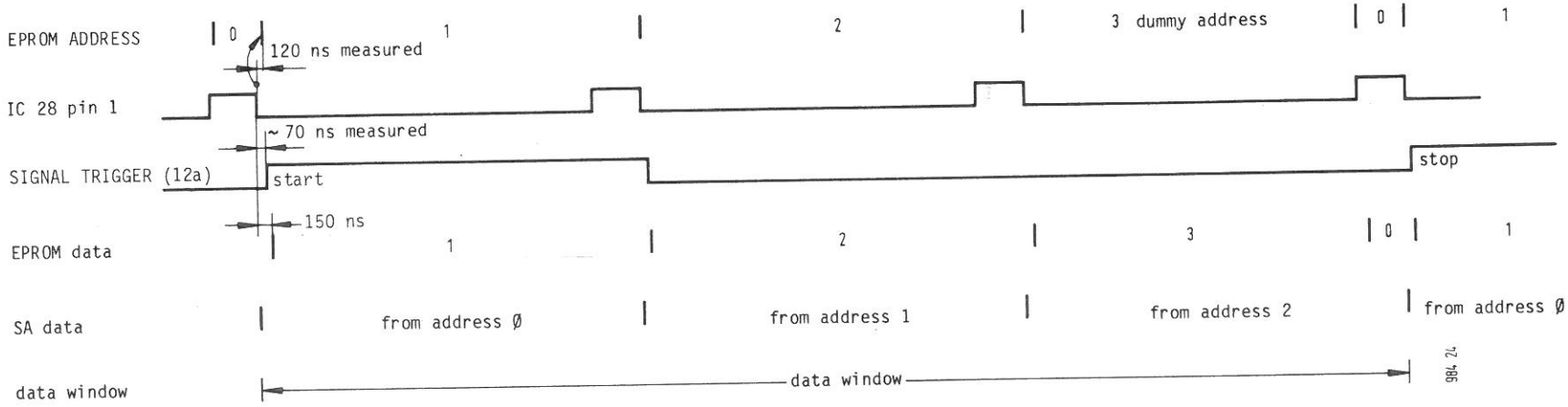
Figure 9.2.7-5 Timing diagram 2





The signatures are for the clock setting ⌟

Figure 9.2.7-6 64 kbit/s signature at output (29b)



clock ⌐ to IC 28 pin 1
start/stop ⌐ → 12a

Figure 9.2.7-7 EPROM signatures

9.2.8 ANALOG FILTER [984-I] (18)

Description using circuit diagram 984-7518

The high pass and low passes used for selecting the bandwidth are accommodated on analog filter board [984-I].

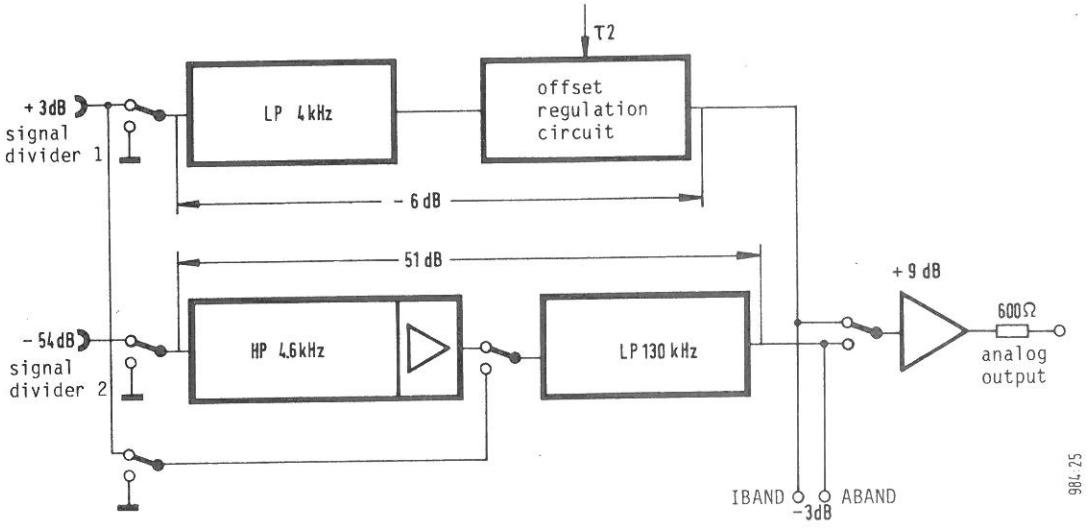


Figure 9.2.8-1 Block circuit diagram of analog filter [984-I]

The signal "SIGNAL ATTN 1" passes from the output of the INPUT-1 stage to the anti-aliasing filter (lowpass) with a cutoff frequency of 4 kHz. It is an active filter comprising IC 1, IC 2, IC 3.

An offset regulation circuit is connected to the output. The time constants of this circuit can be adjusted by means of T 2 (cf INPUT-1 board). If the T 2-signal is true, FET T1 bypasses the input resistor of the integrating stage (IC 4). This means that sudden offset changes which occur when the gain is altered are quickly eliminated.

A second signal path connects the signal from the SIGNAL ATTENUATOR directly to the lowpass (cutoff freuquency 130 kHz). The following digital signal processing circuits which are selected in this operating mode sample the signal randomly. This means that signals, whose frequency is greater than the average sampling frequency can be processed. The upper frequency limit is about 80 kHz.

A second signal tap SIGNAL DIVIDER 2 (after intermediate amplifier 2 on INPUT-1 board) leads to the highpass (cutoff frequency 4.6 kHz). This is realised as a CAUER filter with an output amplifier stage (IC 5, IC 6).

The following lowpass is used to select the bandwidth for out-of-band measurements. In this operating mode, a wideband rms rectifier is used.

Signals having frequencies up to the cutoff frequency of the 130 kHz lowpass can be processed. The filter output signals IMBAND and ABAND are connected to the A/D conversion circuits. After passing through a further stage of amplification (IC 7, +9 dB) they are output at the back panel of the PCM-4.

9.2.9 A/D CONVERSION BOARD [984-K]/[984-R] (17)

Description using circuit diagram 984-7517/984-7514

After the signal has passed through the appropriate analog filter (the 4 kHz lowpass is the anti-aliasing filter for the subsequent sampling of the IMBAND signal), analog-digital conversion is carried out by the ADC board.

There are two versions the only difference between the versions being the A/D converter and the A/D converter drive.

ADC 1 (HS 9516-6) [984-K]
ADC 2 (PCM 75 KG) [984-R]

The following diagram shows the most important functions of the ADC board:

- RMS rectifier for ABAND signals with frequencies up to 130 kHz
- Sample hold
- 16-bit A/D converter with subsequent memory latches (D flip-flops)
- 10-bit D/A converter for eliminating offsets
- Timing units (monostables)
- Level monitor
- Relay drive
- Address decoding

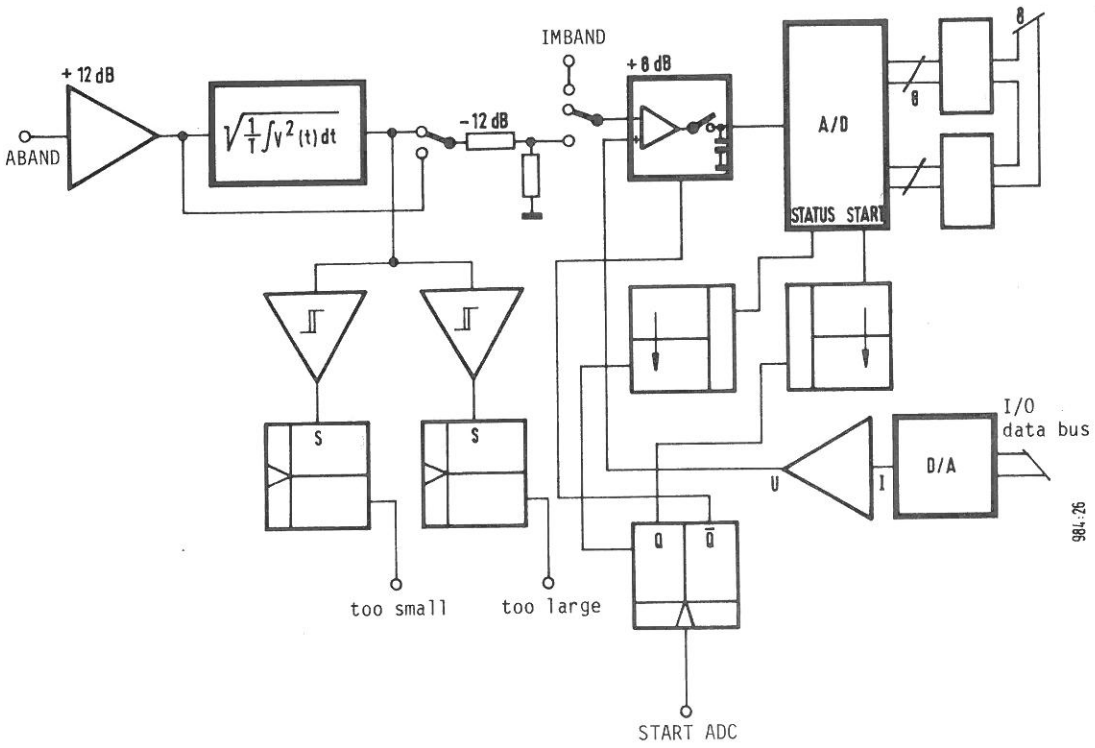


Figure 9.2.9-1 Block circuit diagram for ADC board

ABAND, one of the two output signals from the analog filter, is connected to an amplifier stage (IC 1). The stage amplifies the signal so that its level is +12 dB higher than that produced by the rms rectifier AD 536 AKD (IC 2).

For crest factors < 6, the output voltage deviates by no more than 1% from the actual rms value. To reduce this error as much as possible and at the same time ensure matching with the following sample & hold stage, the signal level at the output of the rms rectifier must be determined.

The level monitor, a composite circuit comprising comparators (IC 3) and the following "overdrive" flip-flops (IC 4) compares the output voltage with fixed thresholds above and below the centre of the range -3.02 dB (input ABAND/IMBAND). Hysteresis of -13/-14 dB or 6.68/6.63 dB ensures unambiguous switching states for the "overdriven" output signals ("too large", "too small").

The lower comparator threshold of -13/-14 dB (input ABAND) is not used by the software at the present time.

The upper comparator threshold is used to monitor the overdrive level referred to the ADC (digital output).

The following diagram shows the various levels on the ADC board.

Hysteresis switching points for the level monitor:

	Nominal value		Tolerances	
ABAND input	6 .68 dB	6.63 dB	7.01 dB	6.27 dB
Input comp. (TP2)	18.7 dB	18.65 dB	19.03 dB	18.29 dB
ADC input	14.7 dB	14. 65 dB	15.02 dB	14.29 dB

Depending on the test mode selected, (out-of-band measurements with sinusoidal signals (4.6 kHz to 72 kHz)) or wideband measurements (noise to 128 kHz), the rms rectifier can be bypassed by switching over rel 1.
The signal path contains a resistive divider (level reduction, well-defined terminating impedance of 6.98 kΩ), this is connected to rel 2 which is used to select the out-of-band signal or the IMBAND signal (-3 dB).

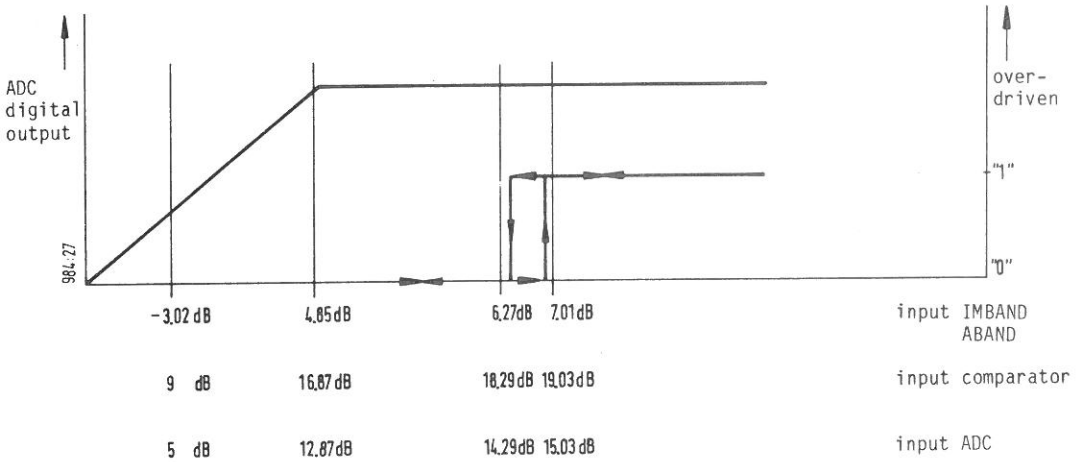


Figure 9.2.9-2 Level diagram for the level monitor

The IMBAND signal is directly connected to the S&H module.
The auxiliary circuitry for the S&H module (MP 260, IC 5), fixed its gain at +8 dB (+14 dB). The timing block described below controls the sample and hold procedure, the time constant is dimensioned for max. error of 0.0015% (1 LSB).

The samples (range centre +5 dB) are fed to a 16-bit A/D converter. The successive approximation method is used for both versions:

ADU 1 (HS 9516-6)
ADU 2 (PCM 75 KG)

The clock rate for ADC 1 is adjusted externally with P2; the required reference voltage is derived from that of the D/A converter (IC 13). At the output of the A/D converter, the 16-bit words are buffered in IC 10 and IC 11. Using the "output enable" signals for the LSB and the MSB, they are read out in sequence onto the data bus.

A 10-bit D/A converter, AD 7522 (IC 13) and a subsequent current/voltage converter are used to eliminate the S&H amplifiers's offset. The feedback is connected to the non-inverting input of the S&H circuit.
Two alignment values, symmetric about the range centre, are supplied to the S&H circuit and the D/A converter during the calibration phase.

The offset shift is calculated using the reconverted digital results, and a correction value is stored permanently in the data latch of the D/A converter.

The timing block (IC 6, IC 8, IC 9) is responsible for controlling a conversion cycle. The signal "START ADU" (8 kHz or 10 kHz sampling frequency, depending on measurement mode starts the conversion cycle. The signal comes from the digital filter.

Activating the "START ADU" signal causes the S&H flip-flop to go into the "hold" state. Monostable $\tau 1$ (IC 8/1) is triggered and initiates "start conversion" after 1 has elapsed. When the conversion has been completed "status out" activates monostable 2 (IC 8/2), which, in turn, resets the S&H flip-flop. The next sample is then read out.

Address decoding for "output enable" signals and "clear" level monitor is performed by the 2 and 4-decoders IC 14 and IC 15.

The relay energising circuit (port address 63H), comprising data flip-flop IC 17 and the relay driver IC 18 are responsible for signal selection.

In-band/out-of-band (ABAND),
RMS rectifier on/off, (BBAND)
Filter selection on the analog filter board.

9.2.10 CIRCUIT DESCRIPTION OF THE CLOCK FILTER [984-L] (20)

Description using circuit diagram 984-7520

The following functional groups are realised on the CLOCK FILTER BOARD (see following block diagram):

1) Converting a serial 64-kbit/s data signal (Pkt. 4c) into an analog signal at Bu 1 by means of code module D 2913 from INTEL (IC 8).

2) Clock generation for the digital filter
   a) When digital measurements are being made, a 4.096 MHz clock signal is generated from the 8 kHz, the 8 kHz reference signal at Pkt. 3c by means of a PLL comprising phase detector IC 2, lowpass filter IC 5, the 4.096 MHz VCO based on transistor Q1 and comparator IC 6, the clock is available at Pkt. 3b. The signal is then divided down by a factor of 512, so giving an 8 kHz signal which is fed to the 2nd input of the phase detector at Pkt. 4b and closes the loop.

9.2.11 CIRCUIT DESCRIPTION OF EVALUATION PROCESSOR [984-M], (21)

Description using circuit diagram 984-7521

The evaluation processor evaluates signals and results. The following are evaluated. Output signals from the digital filter, PCM octet signal for the selected channel (or for 64 kbit/s input), signalling and various frame-error signals.

The block diagram shows the three main functions of the circuit.

- processor core
- computer-computer coupling
- signal input

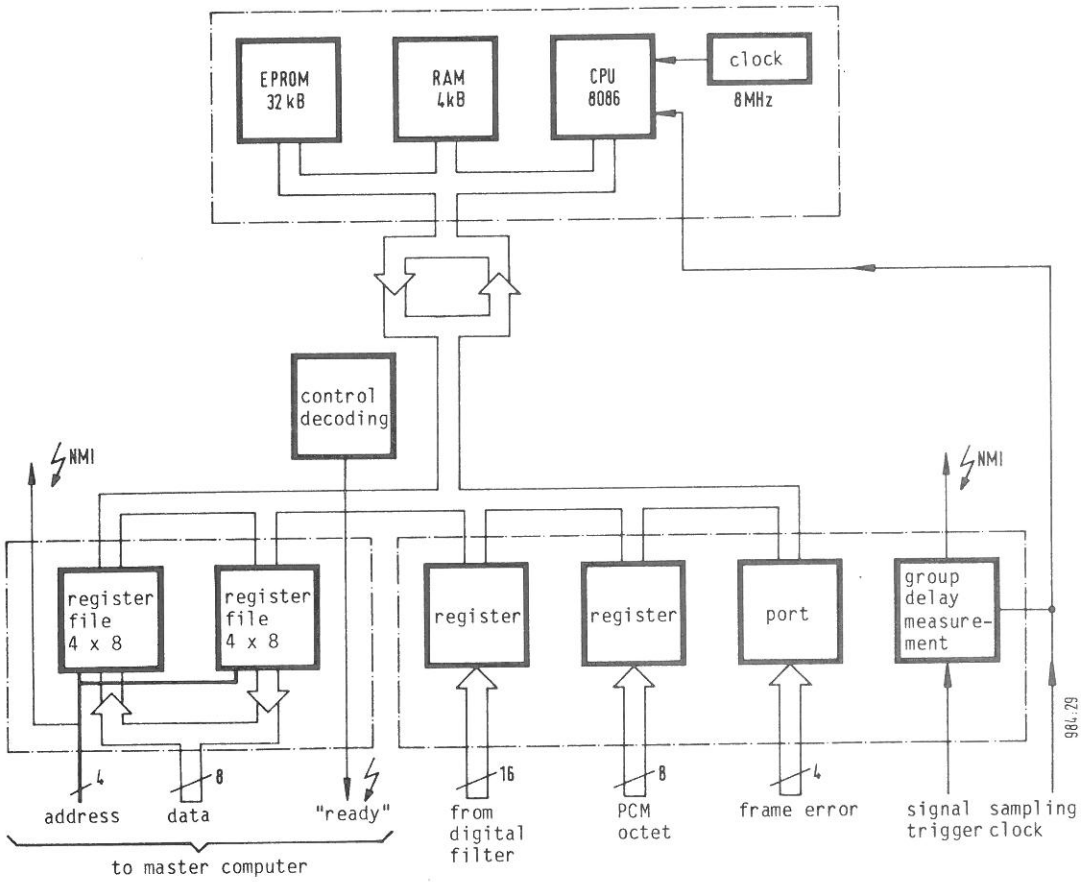


Figure 9.2.11-1 Block diagram of the evaluation processor

Main computer component:

The main computer component is the 8086 16-bit microprocessor which operates at a clock rate of 8 MHz. It has a 32 kbyte EPROM and a 4 kbyte RAM.

Only a 64 kbyte segment is used and this means that addresses A16 to A19 are not required. The RAM address range is ØØØØ to $ØFFF_H$ (one-many address mapping to $7FFF_H$). The EPROM address range is 8ØØØ to $FFFF_H$.

To prevent the computer core data bus being slowed down by capacitative loads, the peripheral data bus is connected by means of bus transreceiver IC 13, IC 14.

IC 18 is the I/O address decoder which provides separate read and write addresses. Various control signals can be switched with latch IC 25:

- Disable NMI
- Ready
- Enable signals for group delay measurements.

Computer-computer coupling

CPU-3 ("test computer") is the master computer for the evaluation processor. A slowed down I/O bus is used to connect both processors. The input of the computer coupling is a 4 x 8 bit register file (IC 15, IC 17), the output also has 4 x 8 bit register file (IC 19, IC 20).

The I/O read-address RAR (pin 10a) and the I/O write address WAR (pin 10b) are precoded in the PCM-4 with 8 x H. The evaluation is therefore addressed by means of the I/O addresses 80_H to 83_H (many-to-one addressing in range 80_H-$8F_H$, a complete decoding has not taken place).

A system of interrupts is used for communication. Writing to the operating mode register W 8Ø (I/O write address 80_H) sends an interrupt (NMI) to the 8086 CPU via IC 21/1, 21/3 and IC 3/2. This causes the evaluation processor to carry out the appropriate task. When the task is complete, the ready line "FMAR" is set to high, triggering an interrupt at the master processor. FMAR stays high until the evaluation processor is started again.

Signal entry

The output signal from the digital signal and the PCM octet signal are accompanied by the sampling clock. These signals and the clock are stored in the appropriate input latches. To save pins both signals are transferred alternately. The synchronisation of the program with the sampling clock is carried out by interrogating the "TEST" input (8086, pin 23) which is tied to the clock. The monostable IC 29 ensures proper synchronisation with the next sample, after the TEST input is interrogated once more after a certain time interval (10 µs) has elapsed.
The signalling and the three error signals have no accompanying clock and are directly interrogated by the computer via port IC 22/1.

IC 28/1, IC 28/2, IC 3/1 and IC 21/1 are used for group delay measurements. Synchronisation to the reference point takes place and the time between the reference point and the sampling edge is measured.

9.2.12 SIGNALLING DISTORTION [984-N] (12)

Description using circuit diagram 984-7512

This board ([984-N]) is used for measuring signalling distortion.

Subassemblies accommodated on the board:

- Signalling generator
- Signalling receiver

The generator is controlled by the test processor. The received signals are evaluated by the evaluation processor [984-M].

The circuit can be used for analog/analog, analog/digital, digital/digital and digital/analog measurements.
For [A-A] send and [A-A] measure, the outputs and inputs are connected to Bu 2 and Bu 1 respectively. The digital send signal (signalling bit output) is fed to the PCM generator [984-T], the digital receive signal (signalling bit input) is fed to the PCM-30 receiver [984-U].

Signalling generator

The generator is driven by CPU-2/3 by means of flip-flop IC 2/1. IC 3/1 and IC 3/2 are used to decouple the digital send signal.
The optocouplers IC 4 and IC 5 are used to isolate the analog send signal. The output stage of the generator can provide a bipolar or unipolar send signal. To this end, transistor T1 is connected to a bridge rectifier circuit. S1 is used to select bipolar or unipolar signals. The advantage of this bridge circuit is that the current flowing, T1, always has the correct polarity.

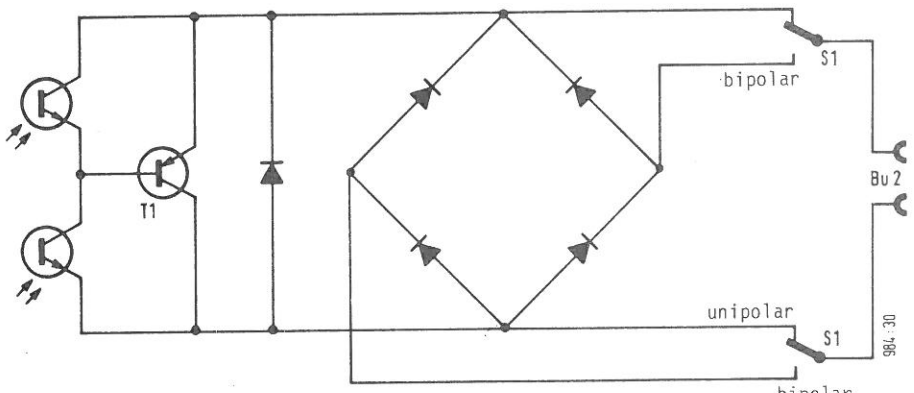


Figure 9.2.12-1 Simplified circuit diagram of the generator output

Signalling receiver

The analog input of the receiver is connected to connector Bu 1. To simulate the input current of a normal PCM-30 signalling converter, resistor R8 (750 Ω) is connected to -15 V. (A real PCM-30 system would have a relay here). T2 and T3 are used for amplitude limiting.

The comparators LM211, IC 6 and IC 7 form a window comparator. This circuit is used to check the closed circuit resistance "Zein" (should be less than 300 Ω) and the opencircuit resistance "Zaus" should be greater than 20 kΩ) of the connected signal source. By pulling down the GND (pin 1) of IC 6 and IC 7 to -15 V by means of R20, R21, G1 13 and G1 14 CMOS voltage levels are obtained at the output of the comparators.

If the on and off impedances of the signal source are not within tolerance, this state can be determined by the test processor by interrogating IC 12/1, the signal is provided by logic operations on IC 8 and IC 11/2.

The actual analog receive signal is passed to the evaluation processor as the signal "W PDG-64" via IC 10/1, IC 11/1, IC 12/2. Both signals (the analog receive signal and the error signal) can be blocked by IC 2/2. Simultaneously, this causes the digital input channel (signalling bit input) to be connected to IC 10/2 on the evaluation processor (digital/digital measurements and analog/digital measurements).

Switch S2 is for status messages. Software polling has not yet been implemented.

9.2.13 DIODE BOARD [984-Q] (14)

Description using circuit description 984-7514
The LEDs show the following states for the PCM frames at the PCM-30 input:

NO SIGNAL	Input signal is too low
AIS	Alarm indication signal (all ones signal)
NO FRAME	Frame synchronisation cannot be achieved
NO MFRM	Multiframe synchronisation cannot be achieved
$\geq$ 3 kΩ	Input impedance at the PCM-30 input > 3 kΩ

9.2.14 PCM-30 INPUT [984-R] (14)

Description using the 984-7514

The unbalanced 75 Ω input Bu 1 handles NRZ, AMI and HDB3. The input circuit converts signal amplitudes between 30 mV and 3 V at the balanced input and signal amplitudes between 23.7 mV and 2.37 V at the unbalanced input into TTL levels. In the case of the pseudoternary line codes AMI and HDB3, the positive and negative pulses are output separately as the signals PCM+ and PCM-. The positive input pulses are fed via the decoupling amplifier IC 1 to a peak value rectifier (IC 2/1, Gl 5, C8, IC 3/1). The voltage is reduced by a factor of a half by a divider (R 22, R 23), and at TP 4 it gives a suitable switching threshold for the comparator IC 4/1. The comparator processes the positive input pulses and outputs PCM+.

The inverting amplifier IC 3/2 and the voltage divider R24, R25 provides the switching threshold for comparator IC 4/2, at TP 5. This comparator processes the negative input pulses and provides the PCM- signal. Comparator IC 2/2 monitors the positive amplitude of the input signal and outputs a "NO SIGNAL" message when the input voltage is lower than 20 mV. The switching threshold for NO SIGNAL can be adjusted with P4. Three potentiometers are used to adjust the offset of this circuit.

P1	offset alignment for IC 1
P2	offset alignment for the peak-value rectifier IC 2/1, IC 3/1
P3	offset alignment for IC 3/2

The circuit R2, Gl 3, Gl limits the output signal of IC 1 to $\pm$ 2.5 V.

9.2.15 PCM-30 OUTPUT [984-S] (16)

Description using circuit diagram 984-7516

There are two separate output stages at the PCM-30 output. One for the data signal and one for the clock. An unbalanced 75 Ω output and a balanced 120 Ω output is provided for each stage. The output stages convert the TTL levels used inside the instrument into the PCM line levels of ± 2.37 V into 75 Ω or ± 3 V into 120 Ω.

Basically, the output stages comprise four switches that connect twice the characteristic impedance 2 x Z = 150 Ω to a positive or negative voltage. The magnitude of these voltages is twice the output voltage (2 x 2.37 V = 4.74 V) when terminated with Z = 75 Ω.

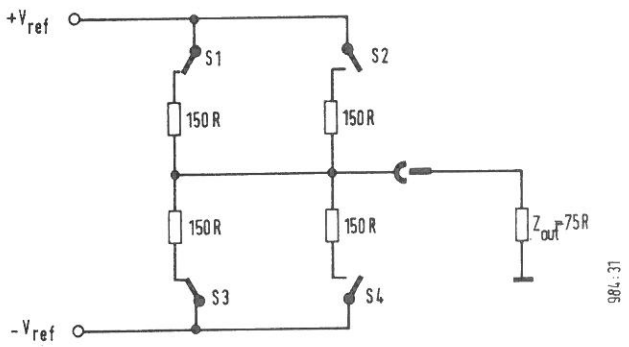
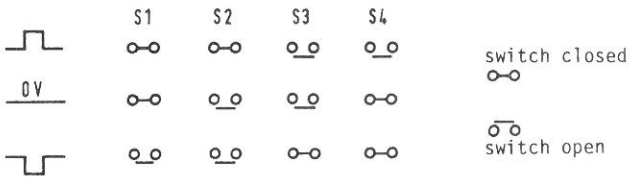


Figure 9.2.15-1 Simplified circuit diagram of the output stage

As two switches are always closed, the circuit has an output impedance of 2 Z/2 = 75 Ω no matter what the output level is. The following table gives the switch state as a function of the output level ($+V_{out}$, 0 V, $-V_{out}$).



The four switches (S1 to S4) in the simplified circuit diagram are replaced by the transistors T1 to T4 (clock output stage) or T6 to T9 (data signal output stage).

The output voltage at TP 1 or TP 2 depends on the operating voltage $+V_{ref}$ (TP 3) and $-V_{ref}$ (TP 4). The reference voltages can be adjusted with potentiometers P1 ($-V_{ref}$) and P2 ($+V_{ref}$).

9.2.16 PCM-30 GENERATOR [984-T] (24)

Description using circuit diagram 984-7524

The PCM-30 generator produces a 2.048 Mbit/s serial data stream. This signal has the frame structure set for GENERAL PARAMETER. The block circuit diagram of the PCM-30 generator shows the most important functional blocks of the circuit. They are described briefly in the following sections.

The computer interface connects the PCM-4's I/O data bus with the hardware of the PCM-30 generator via buffer IC 63 and is used to transfer the setting data and the PCM frames and multiframes. Demultiplexer IC 2 decodes the port addresses CØ to CF. The memory for the frame alignment word has C3 for its address.

The gate array frame circuit IC 5 (Bv. 984-9302.517) generates the timing clock for constructing the frame and multiframes. The circuit is basically a time slot counter with decoding for the frame and time slot signals. Using the address inputs AØ and A1, the time slot selection and the frame structure setting functions are stored in two 6 bit registers.

Functions of the most important frame circuit output signals:

TS 0	Clock signal for time slot 0
TS SYNC	Clock signal for the frame alignment word
TS MW	Clock signal for the not frame alignment word
TS 16 CCITT	Clock signal for time slot 16
TS T	Clock signal for the occupied time slot
FREE TS	Code for free time slots
T8	Octet clock signal
TS DYN 1, 2, 4, 8, 16, 32	Time-slot counter outputs
FRAME 1, 2, 4, 8	Frame counter outputs

The PCM words required to construct the frame, e.g. frame alignment words, not frame alignment words etc. are stored in registers with TRI-STATE outputs. The outputs of the registers are all connected to the octet bus (OCB1 to OCB8). The frame circuit provides the bus enable signal for these registers.

The serial 64-kbit/s interfaces to the PDG-64 and to the 64 kbit/s input are realised in the same way and are both codirectional, i.e. an 8 kHz octet clock and a 64 kbit/s bit clock are output to receive the 64 kbit/s data signal. The 64 kHz signals are generated by the counter IC 48/1 and IC 48/2 by dividing down the 256 kHz octet clock T8 by a factor of four. The D flip-flops IC 46/1 and IC 46/2 are used to synchronise the 64 kHz clock with the 8 kHz channel signal.

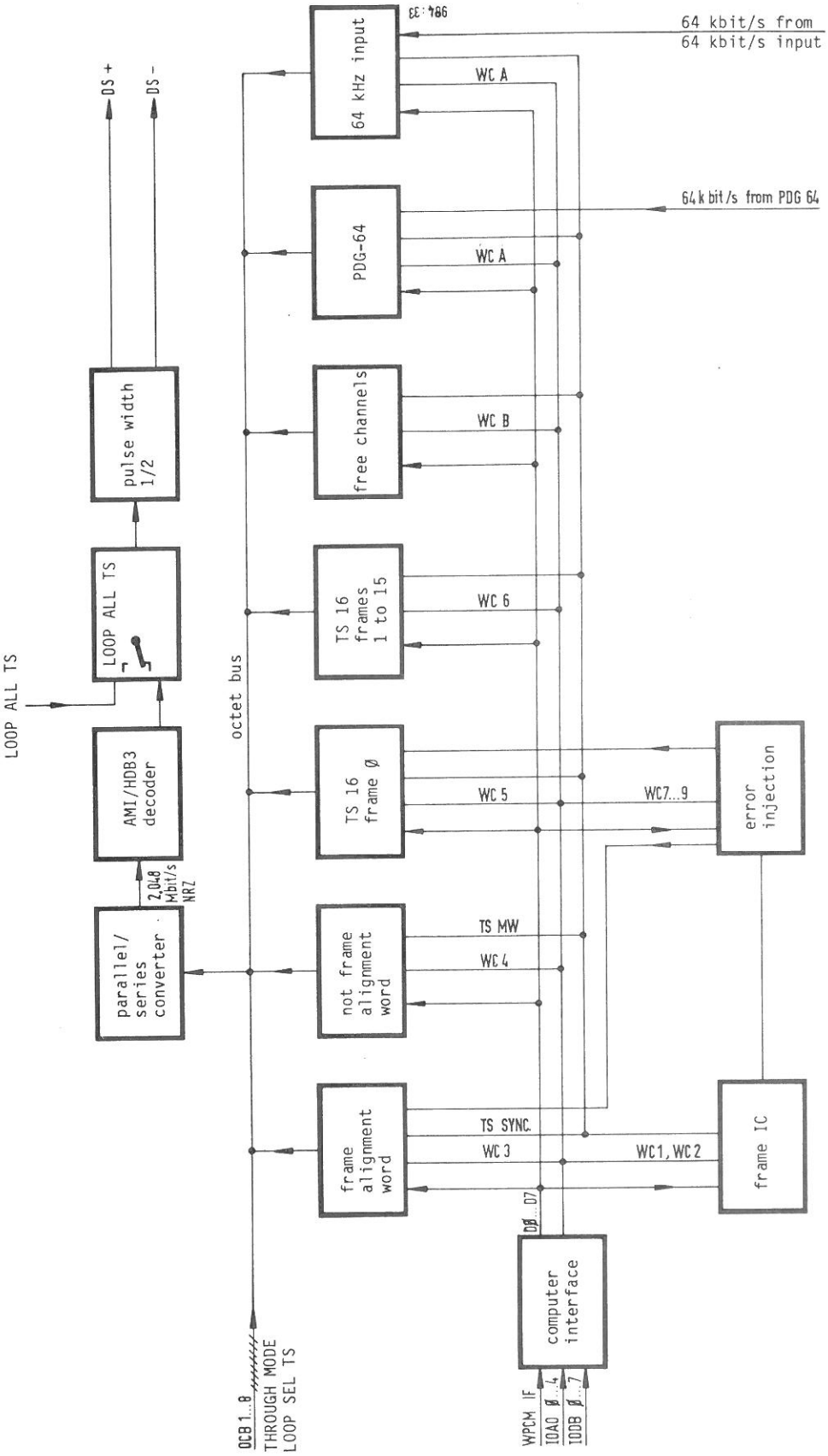


Figure 9.2.16-1 Block diagram of the PCM-30 generator

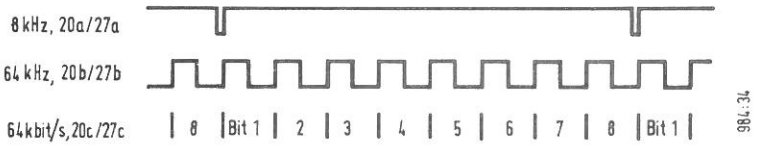


Figure 9.2.16-2 Timing diagram for the 64 kbit/s interfaces

IC 39 connects the signalling bits for the telephone channel in time slot 16, frames 1 to 15 to the octet bus OCB1 to OCB8. When the frame structure "G.732 TS 16 INTERNAL" is selected, the signalling bits come from the 4-bit register IC 34, when "G.732 TS 16 EXTERNAL" is selected from connector 1 pins 1 to 4. When LOOP SELECTED TIME SLOT is selected the signalling bits come from the PCM-30 generator via board connection points 17a, 18a, 18b, 18c. When signalling distortion measurements are being carried out, ICs 35 and 36 replace one of the four signalling bits (a to d) with the signal WKZ-T (19c) which is produced on the signalling distortion board. The selection is made by decoder IC 27/1.

The programmable 16-bit backward counter IC 18, IC 22 is the main component of the circuit for injecting errors into the frame alignment word. The 8-bit registers IC 19 and IC 23 are used to program the counters. In accordance with the GENERAL PARAMETERS 621 to 624, the multiplexer IC 21/1 selects the appropriate error ratio. The exclusive OR gate IC 13/1 inverts bit 1 (OCB2) of the frame alignment word each time an error pulse is generated.

The exclusive OR gate IC 13/4 inverts bit 2 (OCB2) in the multiframe to inject an error. The multiplexer IC 21/2 selects the error ratio defined by the GENERAL PARAMETERS 625 and 626.

The parallel/series converter IC 55 converts the 8-bit wide octet bus OCB1 to OCB8 to a serial 2.048 Mbit/s NRZ signal. To this end, the channel octets are loaded synchronously in sequence using the octet signal $\overline{T8}$. An all ones signal (AIS) can be generated by the OR gate IC 56/2.

The coder IC 57 has, as is appropriate for AMI or HDB3 codes an output for positive data signals (+HDB3 OUT, pin 15) and an output for negative data signals (HDB3 OUT, pin 14). Output CKR (pin 10) provides an NRZ signal with the same digital delay as $\pm$ HDB3 OUT. When the LOOP ALL TS operating modes has been selected, the received PCM signal is looped-through directly to the PCM-30 generator (21c, 22c, 23c). Multiplexer IC 60 is used to select the normal generator mode or the LOOP ALL TS mode.

Flip-flops IC 61/1 and IC 61/2 limit the pulsewidth of the output signals $\overline{DS+}$ (29a) and $\overline{DS-}$ (29b) to half the bit width for AMI and HDB3. The DIL switch S 1/1 can be used to select the full bit width. The other switches (S1) provide the static drive for the PCM-30 output when tests are being carried out.

9.2.17 PCM-30 RECEIVER 1 [984-U] (23)

Description using circuit diagram 984-7523 and the block circuit diagram of PCM-30 receiver 1.

The main function of the PCM-30 receiver is to synchronise the incoming PCM frames and to generate the frame and multiframe clock signals, which are necessary for further processing.

The two monostables IC 2/1 and IC 2/2 increase the pulse width of the incoming $\overline{PCM+}$ and $\overline{PCM-}$ bit streams which are half a bit wide (244 ns) to a width of 1 bit (488 ns). In this way, data bits can be sampled with the clock from the clock recovery circuit. Decoder IC 7 converts the incoming AMI or HDB3 coded signals into NRZ coded signals. The module is transparent to incoming NRZ signals. The input signal is also monitored for all ones (AIS, pin 7) and code errors in the form of BPV (EPROM, pin 9).

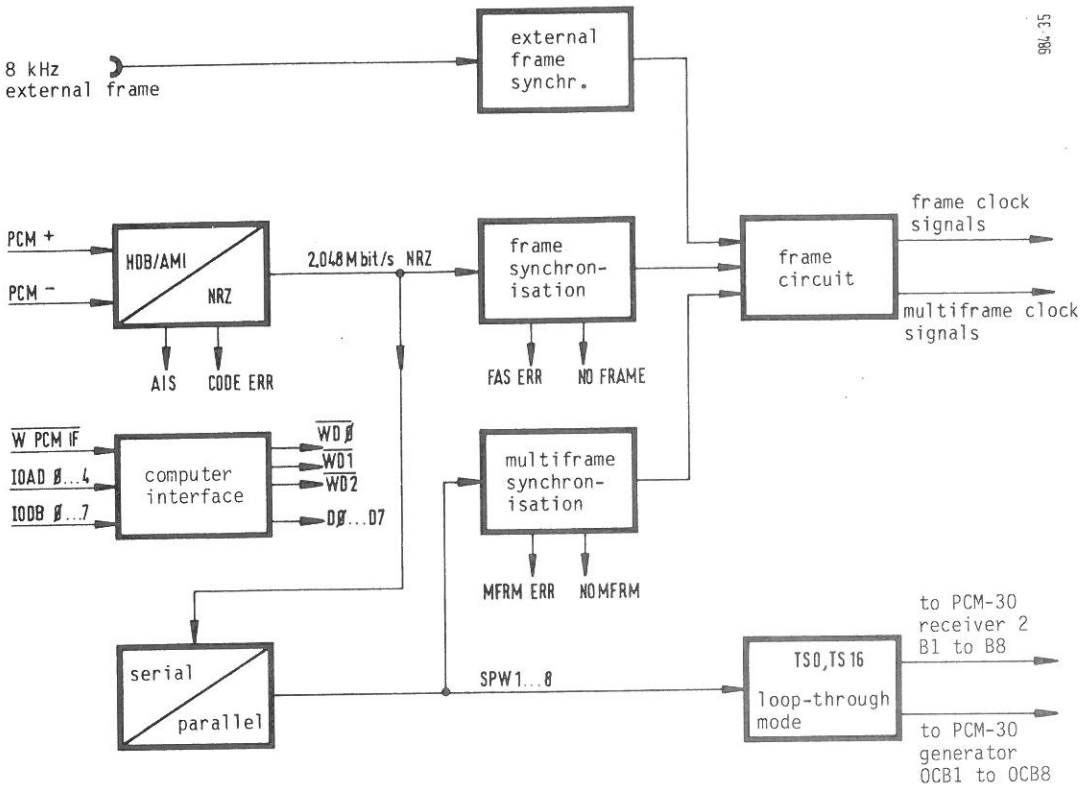


Figure 9.2.17-1 PCM-30 receiver 1

Frame synchronisation is ensured by the synchronous word receiver IC 13. The module provides the signal for setting time slot 1. The SYNC. ALARM output (pin 6) indicates loss of frame synchronisation, the ERROR output (pin 5) outputs an error ulse when an errored frame alignment word is detected.

To make processing easier, shift register IC 17 converts the serial data stream into an 8 bit parallel bit stream. This data stream is decoded by IC 35/1 to give the multiframe synchronisation word (ØØØØ). IC 35/1, IC 35/2 and IC 43/1 recognise an "all zeros" signal. The further components of the multiframe recognition circuit are the errored multiframe alignment word counter IC 39 and the all zeros counter IC 40 for time slot 16. When the actual multiframe synchronisation procedure is taking place, the frame counter IC 19 in the frame circuit is set to zero by IC 18/2 when the first correct multiframe alignment word is received.

An 8 kHz signal, whose positive going edge is in phase with the leading edge of bit one the incoming frame, must be applied to Bu 2 if external frame synchronisation is used.

The analog delay of the PCM-30 input and the pattern/clock converter is equalised by means of line receiver IC 5 and the RC network R6, C38. The digital delay introduced by decoder IC 7, IC 6/3 and series/parallel converter is equalised by counter IC 9. The 8 kHz synchronisation pulse is switched through to frame circuit IC 9 via IC 18/1, where it sets the time slot counter to time slot zero.

The gate array frame circuit IC 19 (Bv. 984-9302.517) is the same as the frame circuit in the PCM-30 generator. For a description of the former circuit see the description of the frame circuit for the PCM-30 generator.

When the THROUGH MODE and LOOP SELECTED TS operating modes have been selected, both frame circuits must be synchronised. The signal $\overline{\text{TS LOAD}}$ (14c) is used to synchronise the two time channel counters, the signal SET (15c) is used to synchronise the two frame counters. The synchronism of the two frame circuits is monitored by IC 25, 20/2, 22/3 and 24/2, if need be the circuits are resynchronised.

The parallel, converted signal from IC 17 is sampled using the 256 kHz time slot clock (t8) in IC 36, so that the appropriate time channel octet appears at the output for 3.9 µs. This bus (B1 to B8) is connected to the PCM-30 receiver so that further processing can be carried out. The octet bus (OCB1 to OCB8) which connects the PCM-30 receiver to the PCM-30 generator is interrupted by IC 33 in the normal send and receive mode, when the THROUGH MODE INSERT is selected, the occupied telephone channel is masked out in IC 33 by the signal $\overline{\text{TST}}$ (28a). The 4 signalling bits in this channel are masked out with the signals < TS 16 = L (13b) or > TS 16 ≅ L (13c).

When the LOOP SELECTED TS operating mode has been selected, the octet for any telephone channel can be stored in IC 37 and then inserted in the occupied telephone channel of the PCM-30 generator.

9.2.18 PCM-30 CLOCK CIRCUIT [984-V] (25)

Description using circuit diagram 984-7525

The PCM-30 clock circuit generates the 2048 kHz clock signals for the PCM-30 generator and PCM-30 receiver.

GENERAL PARAMETER 331 to 334 for the generator clock are selcted by multiplexer IC 8. When GENERAL PARAMETER 331 INTERN 2 048 kHz HAS BEEN SELECTED THE CLOCK SIGNAL IS GENERATED BY TRANSISTORS T3 and T4, which form a quartz oscillator. The quartz oscillator oscillates at the nominal frequency of crystal Q1. The signal extracted by comparator IC 18 is divided down to 2048 kHz by IC 13 and fed to line driver IC 9/2 via multiplexer IC 8.

When GENERAL PARAMETER 332 EXTERN 2 048 kHz is selected, a 2038 kHz clock signal must be applied to connector Bu 1 [64]. The clock signal passes via comparator IC 3 to multiplexer IC 8. Switching hysteresis for comparator IC 3 is produced by the feedback circuit R7, R10, R12, R13, C6, Gl 13 and Gl 14. Switch S1 is used to select the input impedance of connector Bu 1 [64], two values are possible 75 Ω or high impedance ($\geq$ 3 kΩ). When GENERAL PARAMETER 333 EXTERN 8 kHz is selected, an 8 kHz synchronisation signal must be applied to Bu 1 [64]. The frame, time slot and bit clock signals for the generator are derived with the help of a PLL. The 8 kHz signal passes via comparator IC 3 and multiplexer IC 14/2 to the reference input (TP 18) of the flip-flop phase comparator which comprises IC 16/1, IC 16/2 and IC 17/1. Transistors T1 and T2 form a pump circuit which has a very small leakage current. The active lowpass filter is realised using opamp IC 19. The oscillator T3, T4 is switched to VCO mode. The loop is formed by the frame circuit in the PCM-30 generator, which acts as a 256:1 divider and outputs the 8 kHz TS 16 signal dyn., signal path 11b (TS 16 dyn.), TP 16, TP 17, the tracking input of the phase comparator.

The TS 16 dyn. signal is inverted by IC 12/2 to give the frame trigger signal. The shift registers IC 10, IC 11 equalise the digital delay time of the PCM-30 generator, so that the frame trigger signal at 11c is in phase with the leading edge of the first bit in each frame at the 2048 kHz digital signal output. As the PLL from TP 17 to TP 18 sets the phase difference to zero, the external 8 kHz synchronisation signal at Bu [64] is also in phase with the frame trigger signal at Bu [61].

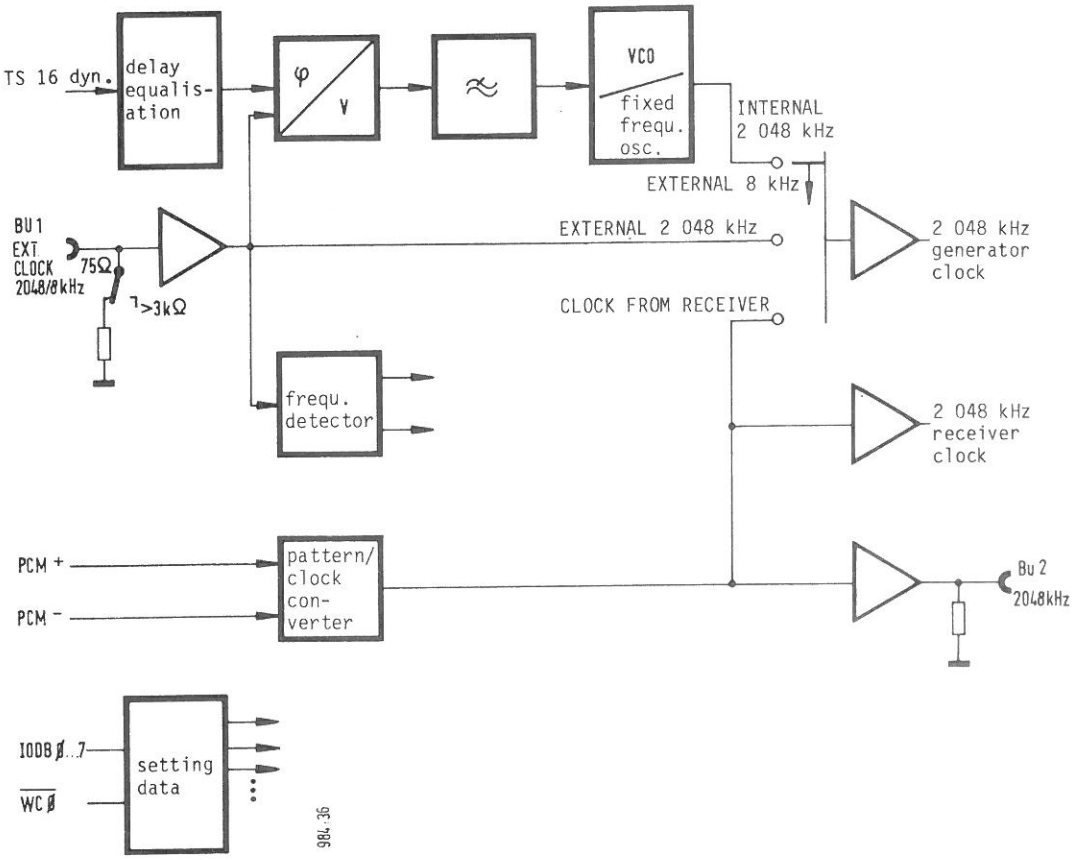


Figure 9.2.18-1 Block circuit diagram of the PCM-30 clock circuit

The delay network IC 12/4, R24, C11 and IC 12/3 equalises the delay of IC 3, IC 9/3 and the 75 Ω driver for the frame trigger signal in the PCM-30 generator. Multiplexer IC 14/2 can be used to select an 8 kHz reference signal from the 64 kbit/s input (27a). Multiplexer IC 14/1 can select the $\overline{\text{TST}}$ signal, the $\overline{\text{TS 16 CCITT}}$ signal or the frame trigger signal as the tracking signal.

When GENERAL PARAMETER 334 CLOCK FROM RECEIVER has been selected, multiplexer IC 8 switches through the pattern/clock converter clock signal through. The post-triggerable monostable IC 4 monitors the input signal from Bu 1 [64]. It is triggered by each positive going edge of the input signal. If there is no signal at Bu 1, the monostable returns to its idle state and the NO EXTERN CLOCK output (10b) goes high. The frequency detector comprising IC 5, IC 6 and IC 7, monitors the input frequency and indicates whether the frequency of the input signal is 8 kHz or 2048 kHz, 8 kHz ≙ H (12c) or 2048 kHz ≙ H (12b).

Pattern/clock converter circuit [893-E]

Circuit description using 893-7502

The pattern/clock converter circuit recovers the 2048 kHz clock signal from the incoming PCM data stream from the receiver.

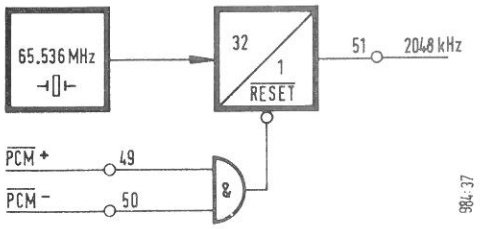


Figure 9.2.18-2 Simplified circuit diagram

The quartz oscillator T101 and T102 uses a crystal Q101 oscillating at the third overtone. The resonant circuit L101, C103, C104 and C105 prevents parasitic resonances. The 65.536 MHz signal is decoupled using the ECL comparator IC 101/1 and is fed to the 16:1 ECL divider IC 102. Transistor T103 provides level matching for the 2:1 TTL divider IC 104. When a negative going edge appears at data input 49 or 50, a reset pulse for the 16:1 divider IC 102 is produced by comparator IC 101/2. IC 103/3 and IC 103/4 produce a reset pulse for the 2:1 divider IC 104. When the reset is taking place, output 51 outputs a positive-going edge of the 2048 kHz clock signal.

The bitrate of the incoming 2048 kbit/s data signal and the clock frequency of the 65.536 MHz quartz oscillator are not in synchronism. This causes systematic jitter with a peak-to-peak amplitude of 1/32 = 3.125% in the recovered 2048 kHz clock signal.

9.2.19 OUTPUT STAGE CONNECTOR [984-W] (11)

Description using circuit diagram 984-7511

The output stage connector is used to connect output stage 1 and output stage 2 to analog generator board 1. Relay 7 is also accommodated on this board, the relay allows one to interrupt signal 2 which comes from the analog generator board. The output stage connector board has been located so as to minimise cross-talk.

The signal calibration 1 passes via the connector board to connector Bu 2.

9.2.20 ANALOG GENERATOR 1 [984-X] (10)

Description using circuit diagram 984-7510

The analog generator comprises the following subassemblies:

Analog generator 1:	signal generation
Analog generator 2:	filter, divider
Output stage 1:	transformer, amplifier
Output stage 2:	output impedances, protective circuits

Purpose, operation

The signals for both generator outputs (main output and auxiliary output) are generated on the analog generator 1 board. The signals undergo digital processing and are connected to a D/A converter so that they are available as an analog signal at the board output.

Clock generation Q1, IC 1, IC 2:

The address counter needs three clock frequencies, i.e. 8.000 kHz, 200.65 kHz and 20.065 kHz.

The frequency of the system clock signal is 8.000 kHz so this signal is already available in the instrument. The 200.65 kHz signal is provided by a 8.0261 MHz quartz oscillator and a 40:1 divider (IC 1). The 20.065 kHz signal is obtained by dividing down the 200.65 kHz signal with the 10:1 divider IC 2.

Address counter for the digital generator IC 5

The address counter (Bv 984-9301.505) is a user-specific circuit which was developed to read data from an EPROM to generate various signals.
The number of samples is variable and must be redefined each time the IC is initialised or another type of signal is selected. The step width can also be programmed and determines the frequency of the output signal for a given sampling rate and a given number of samples.
The address range of 16 k can be divided up into block of n x 0.5 k (n = 1 to 32), this is useful when one switches over to other signals (see fig. 9.1.1-2 memory organisation at the main output).

A multiplexer is accommodated on the IC and, when it is controlled by the processor, carries out clock selection. The selected clock frequency is output at the pin "clock out" and serves as a clock signal for the data latch and for test purposes.

The reset function can also be controlled by the processor.

Changes in the step width must be synchronised with the selected clock. This is carried out with an output command from the processor. An external criterium (high at the enter input) may be taken into account.
Successful synchronisation is indicated by a high pulse which lasts at least one clock period at the EntAck (Enter Acknowledge) output.

EPROM IC 8, IC 9:

Samples having a resolution of 12 bits (equal to $\pm$ 2037 steps) are required for the D/A converter. The address counter addresses two type 27128 EPROMs (each 16 k x 8 bits) in parallel; only 12 of the 16 available bits are used.

The memory organisation is shown in fig. 9.1.1-2.

If you want to expand the memory type 27256 EPROMs can be used. The address counter selects the relevant half of the memory area (each 16 k) by means of control line "control 1".

Data latch IC 10, IC 11:

The data latch comprises two 8-bit modules (74HC273). Address counter IC 5 controls the clock and reset for this module. The flip-flops are triggered by the positive going clock edge.

Enter signal for the sweep mode IC 6:

When the sweep mode has been selected, the frequency should be changed whenever the sine function has a positive zero-crossing. The data in the EPROM are coded using binary offset format (MSB = 1 for all positive values, for all negative values MSB = 0).

If the MSB changes from 0 to 1 (i.e. a positive zero crossing), monostable IC 6 is triggered. The monostable then applies a pulse lasting approximately 10 µs to the enter input of the address counter.

Multiplying D/A converter IC 12:

A type 566 D/A converter is used as a multiplying converter. It provides an output current that is proportional to the required output voltage. The following amplifier IC 16 acts as a current/voltage converter and uses two adjusted resistors in the D/A converter to determine the gain. These resistors have a very small relative error. A signal with a voltage of $\pm$ 2.5 V is available at the output of amplifer IC 16. A/D converter 566 has no internal reference. It obtains its reference voltage from the reference converter IC 15 via IC 13.

Reference converter IC 15:

A type 567 a/d converter is used as the reference converter. It has an internal reference voltage of 10.00 V. This voltage is multiplied by the data word which is set by the processor. The data (12 bits) is written serially in two blocks (bits 0 to 7 and bits 8 to 11) to the pre-latches. Parallel transfer in 12-bit blocks from the pre-latches to the main latches is initiated by the signal EntAck (Enter Acknowledge), after synchronisation of the settings. The current output by the converter is converted into a voltage between 0 and +10 V by IC 13 (see multiplying D/A converter IC 12).

The differential amplifier IC 14 and R10 to R13 invert the reference voltage from IC 15 and pass it to converter IC 21 (reference converter auxiliary output). The differential amplifier also decouples the ground system from the main output and from the auxiliary output.

Asynchronous counter (address counter at auxiliary output) IC 17

An asynchronous counter (CD 4040, 11 outputs used) is used to carry out addressing at the auxiliary output. It counts from 0 to 2047 at a rate of 8.000 kHz (same rate as system clock). This process is repeated until the counter is reset by a computer output port.

EPROM auxiliary output IC 18:

The signals from the auxiliary output are stored in a type 2732 EPROM as 8-bit words. Using an output port, the processor can select one of the 2 k memory sections. Fig. 9.1.1-4 shows the memory organisation of the auxiliary output.

Multiplying D/A converter at the auxiliary output of IC 19:

The multiplying D/A converter DAC 0800 converts the 8 data bits to a current in the range 0 to -1 mA (0 mA for $+V_{max}$, -2 mA for $-V_{max}$ for a 10 V reference) after the 8-bit word has been multiplied by the reference voltage which has been set, see fig. 9.2.20-2a.

The converter output sees a terminating impedance of 5 kΩ (R15, R16), there is a voltage drop across this impedance which is proportional to the output current. The maximum value (peak-to-peak) is always equal to the reference voltage (see fig. 9.2.10-2b). The voltage generated in this way has half the applied reference voltage superimposed on it by the voltage divider R15, R16. This means that the output voltage is symmetrical about 0 V (see fig. 9.2.10-2c).

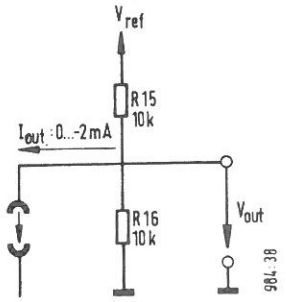


Figure 9.2.20-1 Output circuitry of the multiplying D/A converter at the auxiliary output

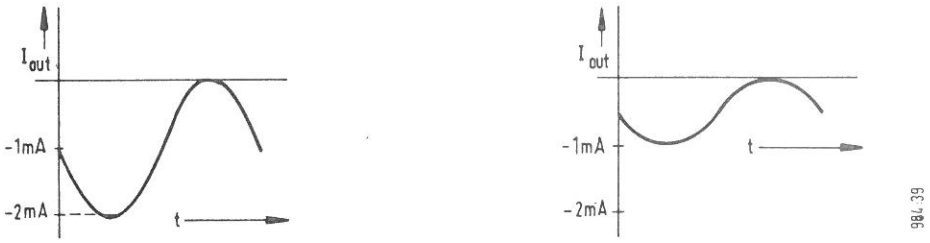


Figure 9.2.20-2a Output current from the converter

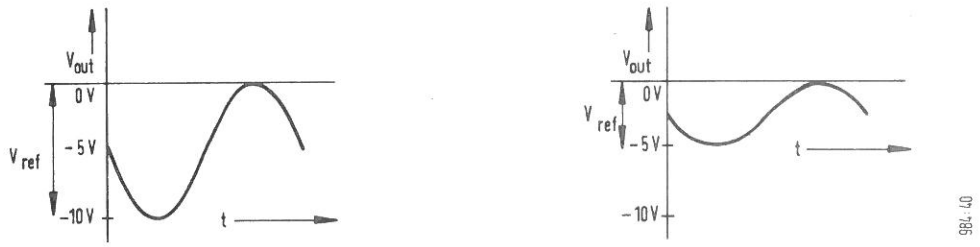


Figure 9.2.20-2b Voltage drop across the output impedance of the converter (R15, R16)

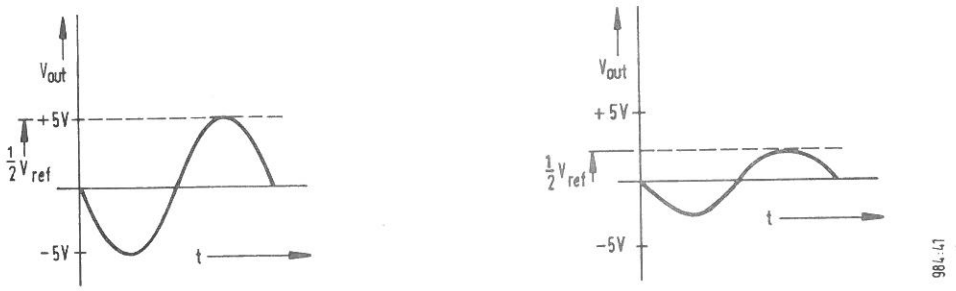


Figure 9.2.20-2c Output voltage after addition of 1/2 V_{ref} through voltage divider R15, R16

Reference converter at auxiliary output IC 21 with inverter IC 20:

The auxiliary output reference converter gets its -10 V reference voltage from differential amplifier IC 14 which is part of the reference converter at the main output.

The logarithmic D/A converter 7118 from AD is used. The applied data (6 bits) is converted to linear 17-bit code in an internal ROM (antilog). An internal 16 bit D/A converter multiplies the applied reference voltage of -10 V with the currently valid value from the internal ROM. The -10 V reference voltage can, in this way, be attenuated in 1.5 dB steps. Inverter IC 20 converts the output current of the AD 7118 into a voltage (inverting). D/A converter resistors are used to determine the gain.

AD 7118 has no internal latches. The data from the computer is written to the 6-bit latch IC 22 and stored there.

Decoder IC 3 to IC 6:

Decoder IC 3/1 splits up the range of the pre-decoded line WSE (16 addresses) into two 8-bit blocks.
One 8-bit block acts as chip enable for the address counter, the other is fully decoded by IC 3/2 and IC 4. The chip select signals drive the output gates for the whole analog generator.

Output ports of the analog generator:

All the analog generator output ports are accommodated on analog generator board 1. Slowed-down control lines control lines then take the control signals for the relays and multiplexers to the other boards (analog generator 2, output stage 1 and output stage 2). Control lines for the relays are buffered by the drive ULN 2803.
As the attenuator settings have to be synchronised, the data is first of all written to prelatch IC 24. When synchronisation is achieved, the data is transferred to main latch IC 25 by the signal EntAck (Enter Acknowledge).

The data for the R_{out} values are stored in the tristate latch IC 27. The tristate input is driven by the protective circuit line (see 9.2.24 output stage 2) "overload". If overdrive occurs, IC 27 is switched to the high impedance state, the resistors R40 to R43 pull the outputs down to 0 V. As a consequence none of the R_{out} relays in the output stage are energised by IC 28 (outputs high) and the overdrive is reduced.

Input port IC 26, S1:

When absolute calibration is carried out, the level is set on DIL switch S1 (6 bits). The switch setting is interrogated via input port IC 26 which is controlled by RSE.

9.2.21 ANALOG GENERATOR 2 [984-Y] (10)

Description using circuit diagram 984-7510

Functions and operation

The signals for generator outputs (main and auxiliary output) are subjected to band-limiting and divided on analog generator board 2.
Driver amplifiers for the output stage are included in the main signal path. Two backpanel connectors, an unbalanced coaxial connector and a balanced CF connector are accommodated on the board and these are for the auxiliary signal path. Both paths to the connectors have an amplifier, in the balanced path there is an extra transformer.

Lowpasses:

The lowpasses which have cutoff frequencies of 72 kHz, 4.5 kHz, 1.76 kHz and 845 Hz (auxiliary signal path) are used to limit the bandwidth of the signals.
As the function of these lowpasses is straightforward no description will be given.

The lowpasses (4.5 and 1.76 kHz) are selected by multiplexer IC 47 as shown in fig. 9.1.1-2 (memory organisation at the main output). If both lowpasses are by-passed (out-of-band signal), the signal level is 6.02 dB higher, as the lowpasses have an insertion loss of 6.02 dB.

Level divider R108 to R116 and IC 50, 51 and 52:

Amplifier IC 50, which has a low output impedance delivers a signal to the level divider.

Level division is carried out on two stages:

Voltage divider with taps at -6 dB, -12 dB, -18 dB, -24 dB, multiplexer IC 51 makes the selection.

Voltage divider with a tap at -30 dB, this is selected by multiplexer IC 52.

Neither of the dividers is decoupled so spurious signals in one divider will affect the performance of the other.

Driver amplifer for output stage IC 53:

Amplifier IC 53/1 provides a high impedance termination for the level divider and also acts as a driver amplifier for the output stage (amplifier path). IC 53/2 matches the level for the transformer divider path in the output stage and also outputs a signal at low impedance.

Output amplifier (auxiliary output) IC 42:

The output amplifier IC 42/1 supplies the unbalanced output via the output impedance of 600 Ω (R81). The level is increased so that noise and sinusoidal signals have an rms value of 0 dB at the output.

The voltage divider R63, R64 divides the voltage from the lowpass, so that the level at the balanced output is 40 dB less than that at the unbalanced output after the signal to the former has passed through the driver amplifier IC 42/2 (g=1), the transformer 01 (turns ratio = 10/1) and been terminated with $Z_{out} = Z_{in} = 600\ \Omega$. Capacitor C65 protects transformer 01 from dc voltages applied to the output.

Calibration signals

After alignment, amplifier IC 40/2 and the voltage divider R50/R51 connected to its input, output a signal having a level of precisely 0 dB.
By moving the wire links a-b and d-e to b-c and e-f resp., this signal is applied to the CF connector of the balanced auxiliary output. The probe of the calibrated level meter can be inserted directly into this connector.*

To calibrate the receiver, the calibration signal is passed through voltage divider R52/R53 to give a signal which can be measured directly by the receiver (no divider in the receiver) and then fed via line calibration I directly to the receiver.

9.2.22 DESCRIPTION OF THE CODIRECTIONAL INPUT [984-Z] (34)

Description using circuit diagram 984-7534

Function in the PCM-4:

Option 984/00.01 provides an input interface for codirectional 64-kbit/s CCITT signals.

Operating mode for option 984/00.01:
RX 64:

The signals "8 kHz PDA" (7b), "64 kHz PDA" (6b) and "64 kbit/s PDA" (8b) are derived from the CCITT signal at Bu 1.
The 64 kbit/s data channel also undergoes series/parallel conversion (octets) and is output via IC 15.

---

* Not used when delivered

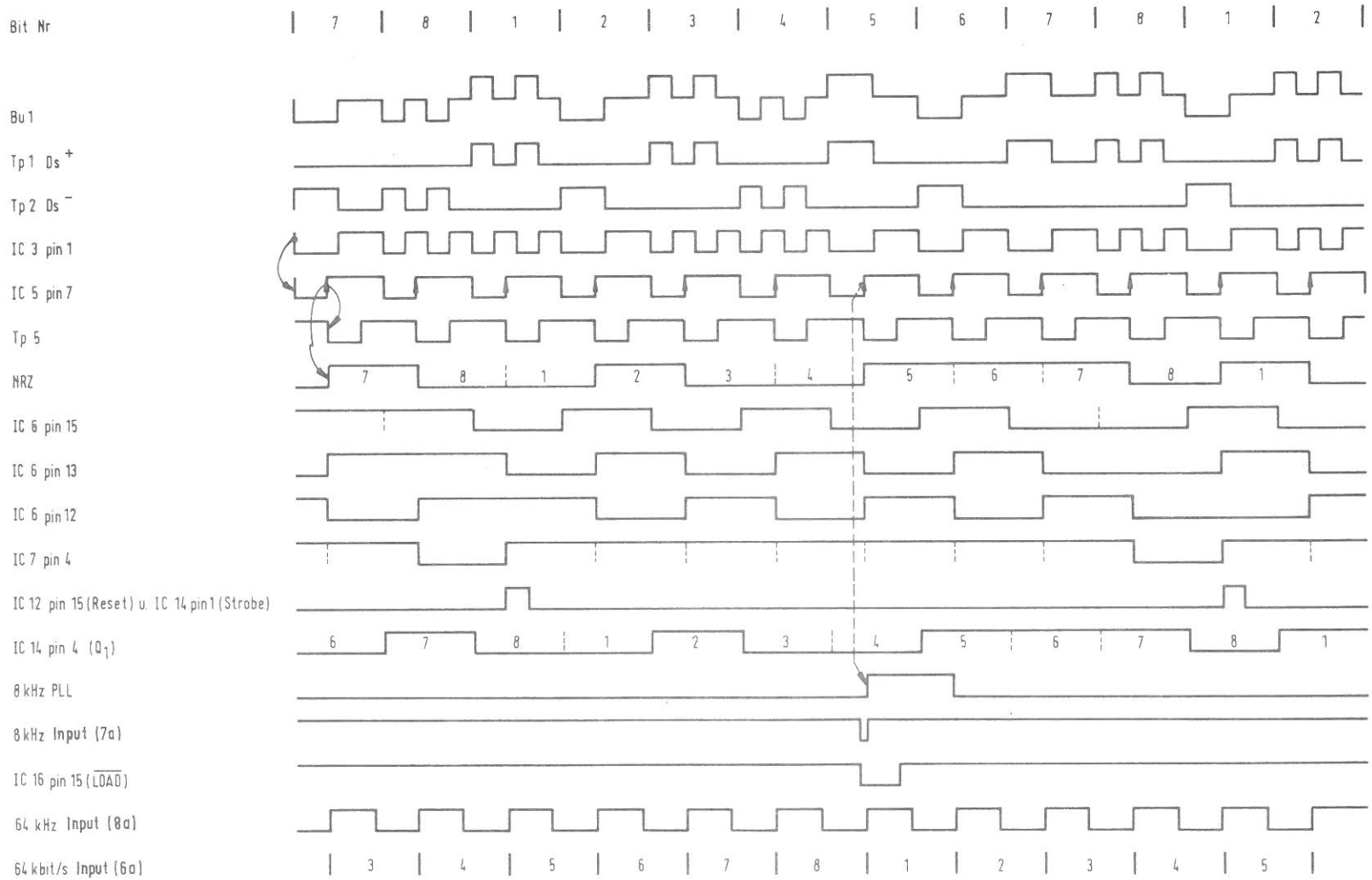


Figure 9.2.22-1 Timing diagram

9.2.23 OUTPUT STAGE 1 [984-AA] (11)

Description using circuit diagram 984-7511

Functions, operation:

On the output stage 1 board, two transformers (amplifier and attenautor) isolate the signal from ground. A relay is used to select the paths.

Amplifier path:

Transformer 02 provides isolation. The inductance and capacitance of the transformer form a resonant circuit with a high Q (the resonant frequency is about 1.1 MHz) as amplifier IC 60 provides high impedance termination. The resonance peak is compensated for by means of the RC network P11/R140/C138 (frequency response alignment).

Amplifier IC 61 is non-inverting but amplifier IC 62 is inverting. Both have the same gain and this means that the voltage between their outputs is double the output voltage of each amplifier with respect to the (floating) ground. Opamps can be used and only half the supply voltage is required.

The output stage has a floating power supply, this comes from the instrument's power supply. Resistors R152 and R153 increase the resistance of the transformer in the amplifier path so that both paths have the same output impedance.

Attenuator path

The transformer divider 03 divides the voltage from analog generator 2 by a factor of 10 and isolates the signal from ground. Because of the turns ratio R = 10:1 no frequency response adjustments are required .

Relay Rel 1 is used to select the amplifier path or the attenuator path, there is a level difference of 42 dB between the two paths.

Protection circuits for the amplifier

If a voltage, which is higher than the supply voltage, is applied to the generator output, the amplifier must be protected until the protection circuit for the Z_{out} resistors in output stage 2 (see output stage 2) comes into effect. The two diodes in the bridge rectifier circuit Gl 24 (depending on the polarity of the applied voltage) protect the amplifier outputs from their supply voltages. The current so caused is taken by the power supply. If the current is so large that the current limiting circuits of the power supply come into effect, its voltage will increase until it exceeds the zener voltages of diodes Gl 22 and Gl 23. The zener diodes then accept the current and diodes Gl 20 and Gl 21 isolate the power supply.

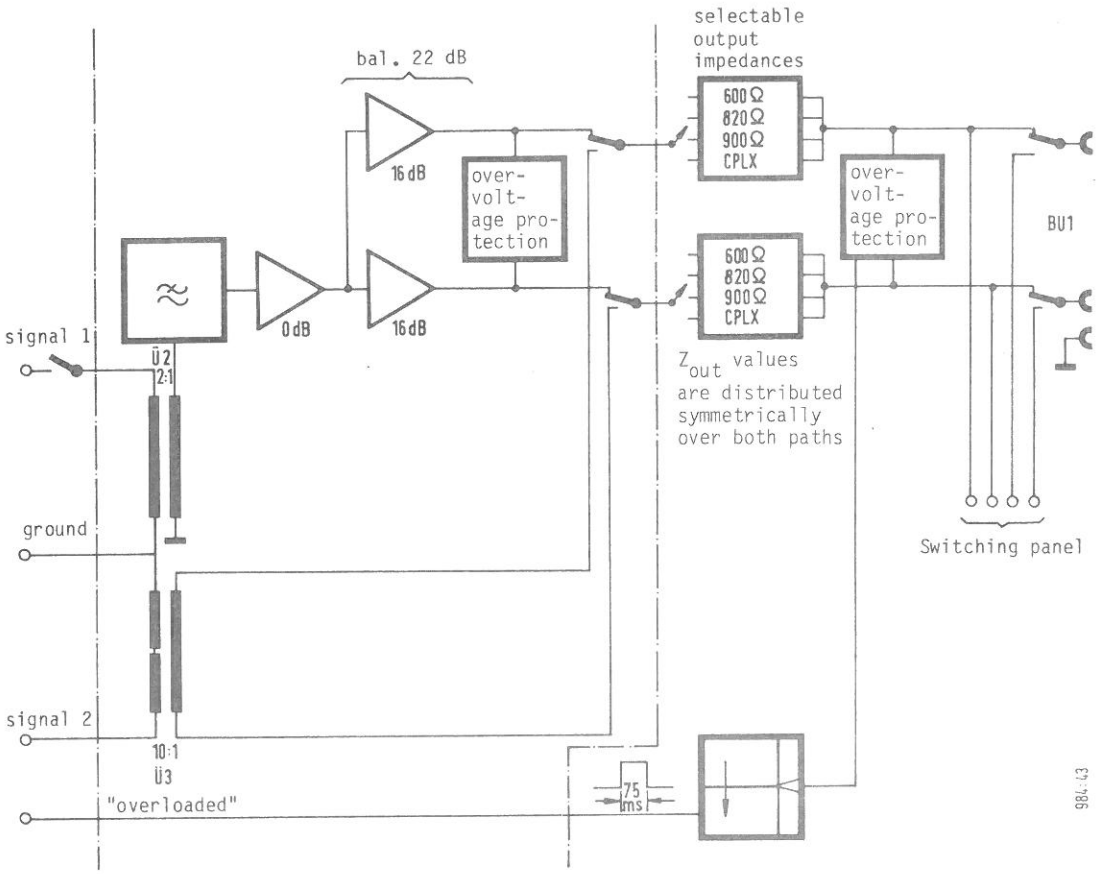


Figure 9.2.23-1 Block diagram of the complete output stage

9.2.24 OUTPUT STAGE 2 [284-AB] (11)

Description using circuit diagram 984-7511

Functions, operation:

The output stage 2 board accommodates the resistors and the protection circuit that stop the resistors that form the output impedance from being overloaded when a dc voltage is applied to the output connector.

Output resistors:

Half of the resistors are inserted in paths a and b to improve balance. Relays rel 2 to rel 5 are used to select the output impedance, i.e. 600 Ω, 850 Ω, 900 Ω and "complex".

Protecting the resistors that form the output impedance

Diodes Gl 30 to Gl 3 rectify the voltage at the output connector via the current limiting resistors R180 and R181. If an external voltage applied to the output connector causes the voltage at the connector to rise by more than 1 V above the max. open-circuit voltage, the zener voltage of Gl 34 is reached and a current flows via the LED of optocoupler IC 64. The phototransistor IC 64 comes on and applies a LOW signal to the input of Schmitt trigger IC 63/4, this in turn switches the overload line to its HIGH state by means of gates IC 63/3 and IC 63/1. The retriggerable monostable IC 65 is also triggered; this monostable has a dwell time which is longer than the longest period in the signal. This means that the overload line is kept high via gate IC 63/1 even if the signal varies periodically about the switching threshold.

When the overload line goes high, the tristate latch in analog generator 1 goes into its high impedance state, this switches off relays rel 2 to rel 5 causing the currently energised relay to be de-energised.

The state of the overload line is also communicated to the processor by means of an interrupt. After the impedance has been connected the generator signal is tapped as an "internal generator signal" for the switching panel board [984-AF] (f8, f4 connector designations).

The signal output (f6, f12, f1) can also be disconnected internally by relay 7, diverted to the switching panel so allowing the output connector to be connected to the test bridge.

9.2.25 COUPLING BOARD 3 [984-AT] (35)

Description using circuit diagram 984-7535

The board accommodates the following circuits:

- Interrupt decoding circuit for CPU-2/3
- Test section interface CPU-2/3
- Monitor brightness control
- Monitor test circuit

Interrupt decoder circuit

The various interrupt signals of the interrupt interface are combined to give two interrupt signals MRST 5.5 and MFST 6.5 (IC 2). The CPU can block each interrupt via the I/O data bus, D latch (IC 10) and AND gate (IC 4, IC 5).

The signals arriving at the interrupt interface are stored by flip-flops IC 11 and IC 13. By means of pulses from the decoder circuit it is again possible to reset the flip-flops. So that the µP can determine the cause of any interrupt, each of the interrupt lines can be interrogated via the input port (IC 8/2, IC 9/1).

The MES END interrupt can be triggered by means of the decoder circuit (IC 3, IC 6, IC 7/1).

Test section interface

The test section interface comprises the decoders IC 14, IC 15 and IC 7/2. Twenty signals are produced in this way by CPU-2/3.

Monitor brightness control

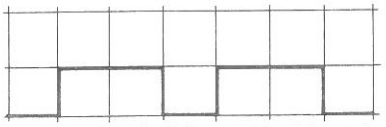
To control monitor brightness, a supply voltage connector, a ground connector and a wire link to take the signal to output connector b are accommodated on coupling board 3.

Monitor test circuit

Using a sampler the flyback signal, which is passed via 2 monostables, is connected to the monitor as an external composite video signal.

div. 500 mV

time base 20 µs



A uniform raster with medium brightness is thus shown by the monitor.

9.2.26 COUPLING BOARD 2 [984-AD] (27)

Description using circuit diagram 984-7527

The following circuit are accommodated on coupling board [984-AD]:

- clock module with drive circuit
- interrupt circuit for CPU-2A/1 (master processor)
- debounce circuit for keypad board [984-C]

Clock circuit

The MC 146818 (IC 18) clock circuit can be initialised by means of the I/O data line, the time and data information can also be read out. The clock frequency to the module is provided by oscillator circuit IC 11 which contains the quartz crystal Q1 (32.768 kHz). The battery supply to prevent loss of data is connected to pin 22. The separate oscillator circuit takes less battery current than the oscillator in the module.

CPU-2A/1 interrupt circuit

The various interrupt signals (SSOD, MESEND, TAS INT, IRQ for the clock) are combined to give two interrupt signals, RST 5.5 and RST 6.5. So that the processor can determine the cause of the interrupt, each of the interrupt lines can be interrogated via input gate IC 5. The processor can also block each of the interrupts via output port IC 7. MSOD or SSOD are acknowledgements from the test processor and the video processor.

Debounce circuit IC 10, IC 12

This is an adaptive debounce circuit. The longer the key bounces the longer the debounce time will be. The TAS INT input indicates whether a key in the activated column of the key matrix has been pressed. Bounce has not been removed from this signal. If no key has been pressed, this signal is LOW. Counter IC 10/2 is therefore not reset and is incremented by the clock (approx. 256 Hz) until it reads 8. Q3 is then HIGH and the count procedure is stopped by the clock input. Simultaneously, the other counter IC 10/1 is reset. This state is maintained until a key is pressed.

When a key is pressed, counter IC 10/1 starts counting and generates an interrupt when it reaches 8. This takes about 33 ms. During this time each bounce pulse resets the counter. The signal from the key must therefore be free of bounce for 33 ms in order to trigger an interrupt.

The interrupt signal is held by IC 6/2 and can be reset by a pulse from the decoder circuit.

9.2.27 PRELIMINARY STAGE [984-AE] (2)

Description using circuit diagram 984-7502

The preliminary stage [984-AE] and the regulator [984-AQ] provide dc isolation for the input signal and some level matching for the following stages.

As the transfer function must have ripple less than or equal to 1 mB over the whole of its central region, and any offset is to be suppressed, a compromise has to be made concerning the settling behaviour of the gain selection circuits.

There are four gain selection stages:
-18 dB, 0 dB, +12 dB, +24 dB.

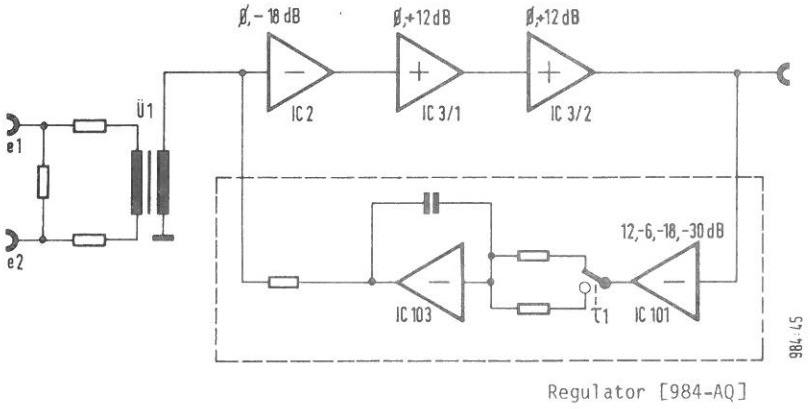


Figure 9.2.27-1 Block circuit diagram of the preliminary stage [984-AE]

The input signal passes from the output of the switching panel (e1, e2) to the primary of the input transformer. The setting of the receiver input impedance is carried out by means of the relay drive circuit (driver switching circuit IC 1); either 600 Ω, 850 Ω, 900 Ω or a complex impedance $\geq$ 30 kΩ can be selected. Small balance corrections can be made with C2.

Transformer Ü1 AND THE INPUT STAGE ET (IC 2) are designed as a current transformer. By switching in or out the feedback resistors gains of -18 dB or 0 dB can be selected (frequency response correction using C3 or C6).

The following stage EV is used to increase the bandwidth, it comprises two opamps (IC 3/1 and IC 3/2) each with selectable gains of 0 dB and +12 dB. Bits 0 and 1 of control address W52 are used to set the attenuator/amplifier combination as shown in the following table:

gain	EV (bit 1)	ET (bit 0)
-18 dB	0	0
0 dB	0	1
+12 dB	1	0
+24 dB	1	1

Figure 9.2.27-2 Attenuator codes

The selection of the resistors in the input attenuator ET that determine the gain is made by relay 7, in all other cases, the CMOS analog switch is used (IC 4, IC 100, IC 102).

The lower cutoff frequency of the input transformer is determined by the time constant L/R, where L is the inductance of the transformer and R is the total series resistance (f_c = 5 Hz). If a measurement mode with a lower cutoff frequency of 20 Hz is selected, the series resistor R16 is by-passed using the signal "E correction" (the impedance correction on the primary side is also by-passed), so that a further reduction in the cutoff frequency is obtained with the remaining ohmic resistance.

A regulator circuit whose feedback path is formed by IC 101 and IC 103, is used to correct the offset of the preliminary stage. The amplifier stage and IC 101 compensates the selected attenuator/amplifier level by +12 dB, -6 dB, -18 dB, or -30 dB (see table).

The following integrator stage (IC 103) is for selecting the time constant of the whole regulation circuit. Attenuator/amplifier selection is program-controlled, timing is provided by a monostable which outputs pulses 43 msec long.

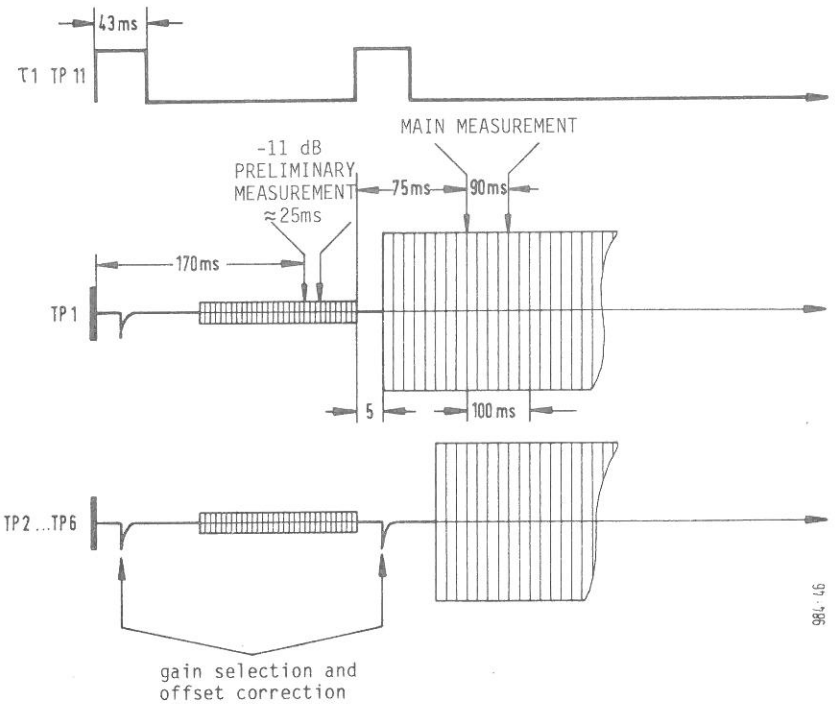


Figure 9.2.27-3 Timing of preliminary and main measurements

Complete sequence:

- Input signal is switched off at the switching panel (τ1 on)
- Selection of the smallest regulator time constant
- Attenuator/amplifier selection
- Pause
- The smallest time constant is switched off (τ1 off)
- The input signal is switched on again

When the gain is being selected, the small feedback resistor in the input stage is switched in (-18 dB). Simultaneously, the small time constant for the regulator circuit is switched in for $\tau 1$ (fast offset elimination).
When the large time constant is reselected, the circuit cannot respond fast enough to maintain a zero offset at the output. At first there is a short rise and then the remaining offset is eliminated (waiting time to start of measurement).

9.2.28 SWITCHING PANEL [984-AF] (3)

Description using circuit diagram 984-7503

The following subassemblies are accommodated on the switching panel board [984-AF]
- Signal path selection
- Overdrive protection circuit
- Buffer amplifier from the test bridge to the preliminary stage (balanced amplifier)

Signal path selection

The analog signal can be directed anlong the following paths by means of the relay circuits.
RX - preliminary stage (relays 2, 4, 6, 8)
RX - via test bridge 1 or test bridge 2 to the preliminary stage (relays 2, 4, 5, 6, 7, 8)
RX/TX - preliminary stage (2-wire receive relays 10, 2, 4, 6, 8)
Generator int - TX/RX (2-wire receive relays 3, 10)
Generator int - test bridge, preliminary stage relays 3, 7, 8)
Generator int - preliminary stage (CAL 2 loop relay 2, 3, 4, 6, 8)
Calibraion 1 - preliminary stage (CAL -1 loop relay 9)

The relays are driven via a D latch IC 6 which is connected to the data bus and a following driver module IC 5. The matching to the 24 V relay is provided by transistors T3 and T10.

Overdrive protection

The input signal is tapped before the contacts of relay 4 and monitored by means of a rectifier bridge (Gl 7 to Gl 10) and the zener diode Gl 11.

The overdrive condition is detected by optocoupler IC 1; a 45 ms long pulse is generated by IC 3, the former energises relay 4 via the driver transistors T1 and T2 and so interrupts the signal path.
This can also be carried out by means of the "signal disconnection" path (from input 1 board).

The rectifier Gl 33 bypasses monostable IC 3 and ensures input signal isolation - even at very low frequencies (< 20 Hz) or dc. The drive for relay 1 is also disabled by an overdrive pulse.

Buffer amplifier between the test bridge and the prelimianry stage

The buffer amplifer has a balanced input and an unbalanced output. The gain is 0 dB. The input of the amplifier can be connected to the output of bridge 1 or the output of bridge 2.

Common mode suppression is adjusted with P1, the offset is adjusted with P2.

9.2.29 TEST BRIDGE [984-AG]/[984-AH] (6)

Description using circuit diagram 984-7506

The test bridge is an optional circuit for the PCM-4.
Application: measuring return loss and signal balance ratio.

Circuit:

The main components in the circuit are two transformers. Depending on the measurement mode that has been selected, the transformers are connected to the appropriate bridges by means of relays. The relays are controlled by the test processor I/O bus. The data word (relay configuration) is stored in the latch memory IC 11, IC 13. The relays are switched by the driver modules IC 10 and IC 12 and the following transistors.

The opamp circuit containing IC 1 acts as a buffer amplifier in the bridge feed path.

The basic test circuits and the signal paths of the PCM test bridge are shown in the following. The signal paths for the reference measurements carried out in the PCM-4 test bridge are not shown.

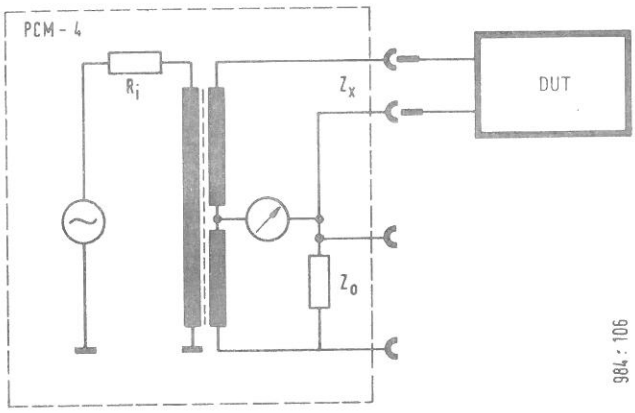
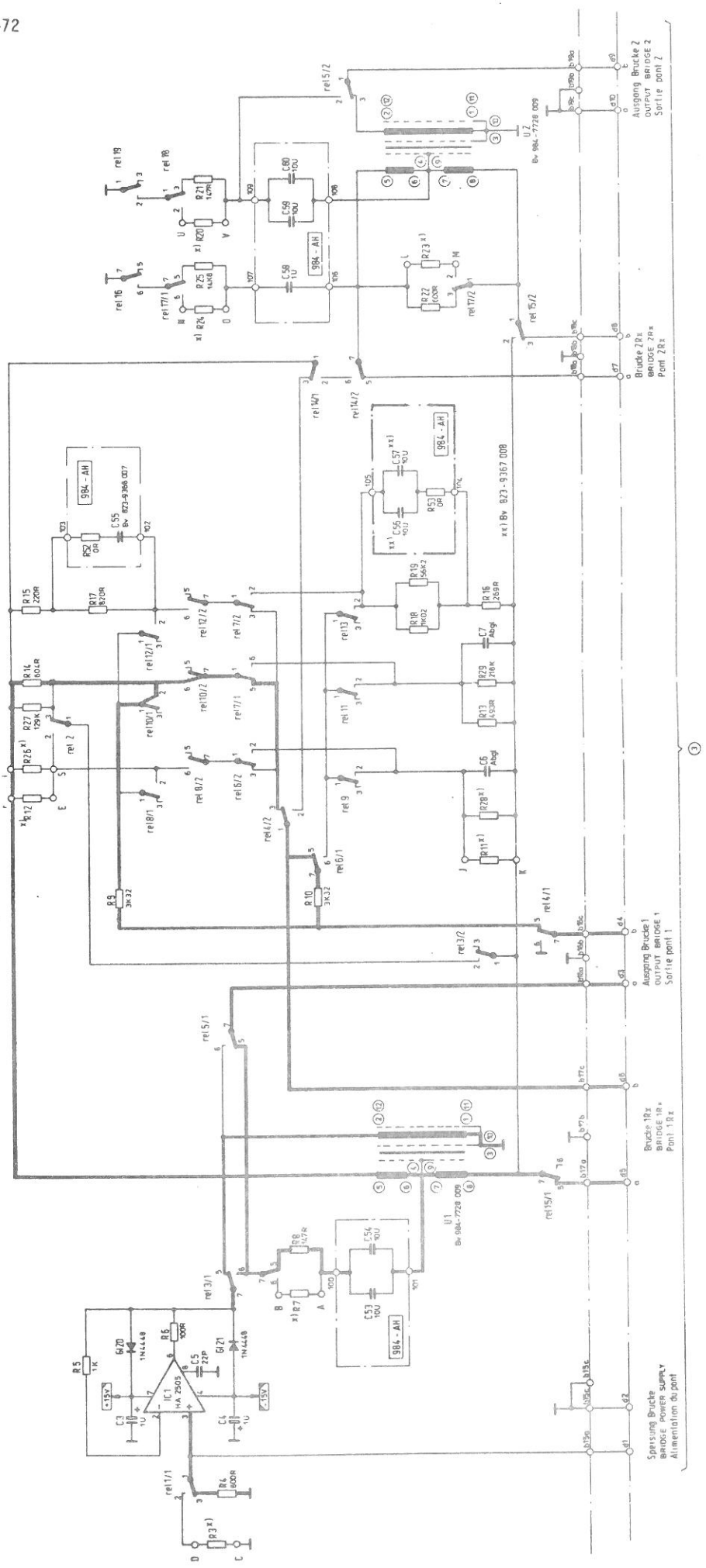


Figure 9.2.29-1 Measuring return loss



Data / Addr.	7	6	5	4	3	2	1	Ø
W53	Ø	Ø	1	Ø	Ø	Ø	Ø	Ø
W54	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø

Figure 9.2.29-2 B11 measuring return loss

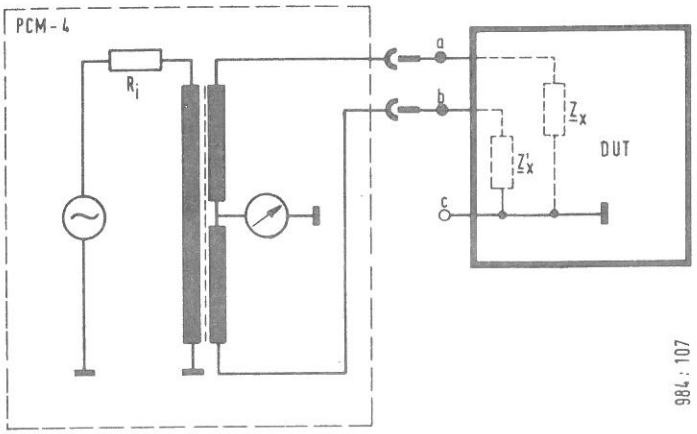
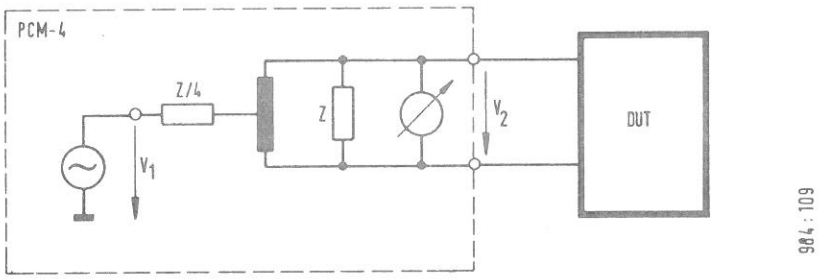


Figure 9.2.29-3 Longitudinal conversion transfer

Measuring longitudinal conversion loss to CCITT O.121

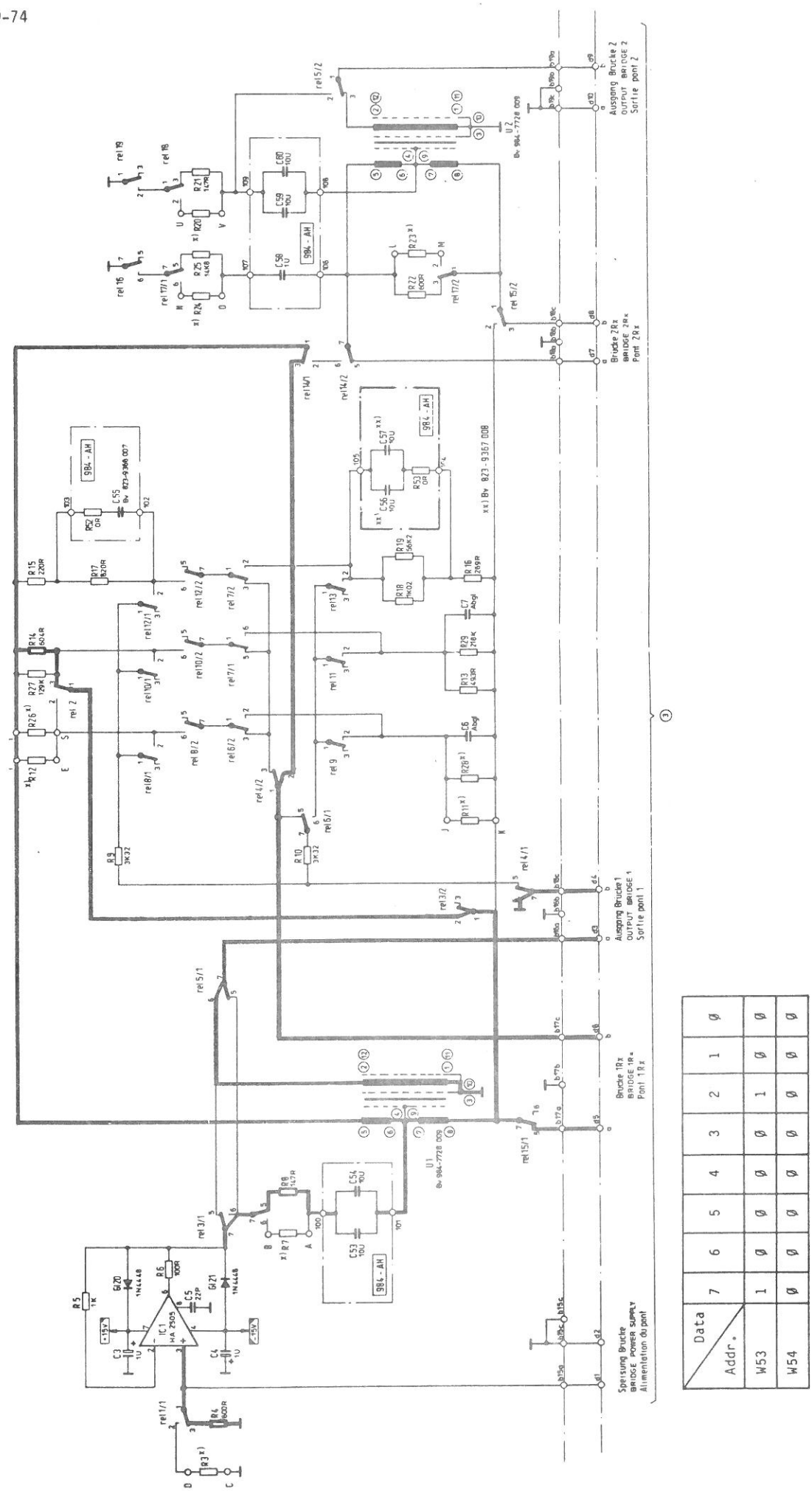


signal balance ratio

$$a_B = 20 \log \left| \frac{V_1}{V_2} \right| \quad dB$$

reference impedance: 600 Ω, 850 Ω,(900 Ω)

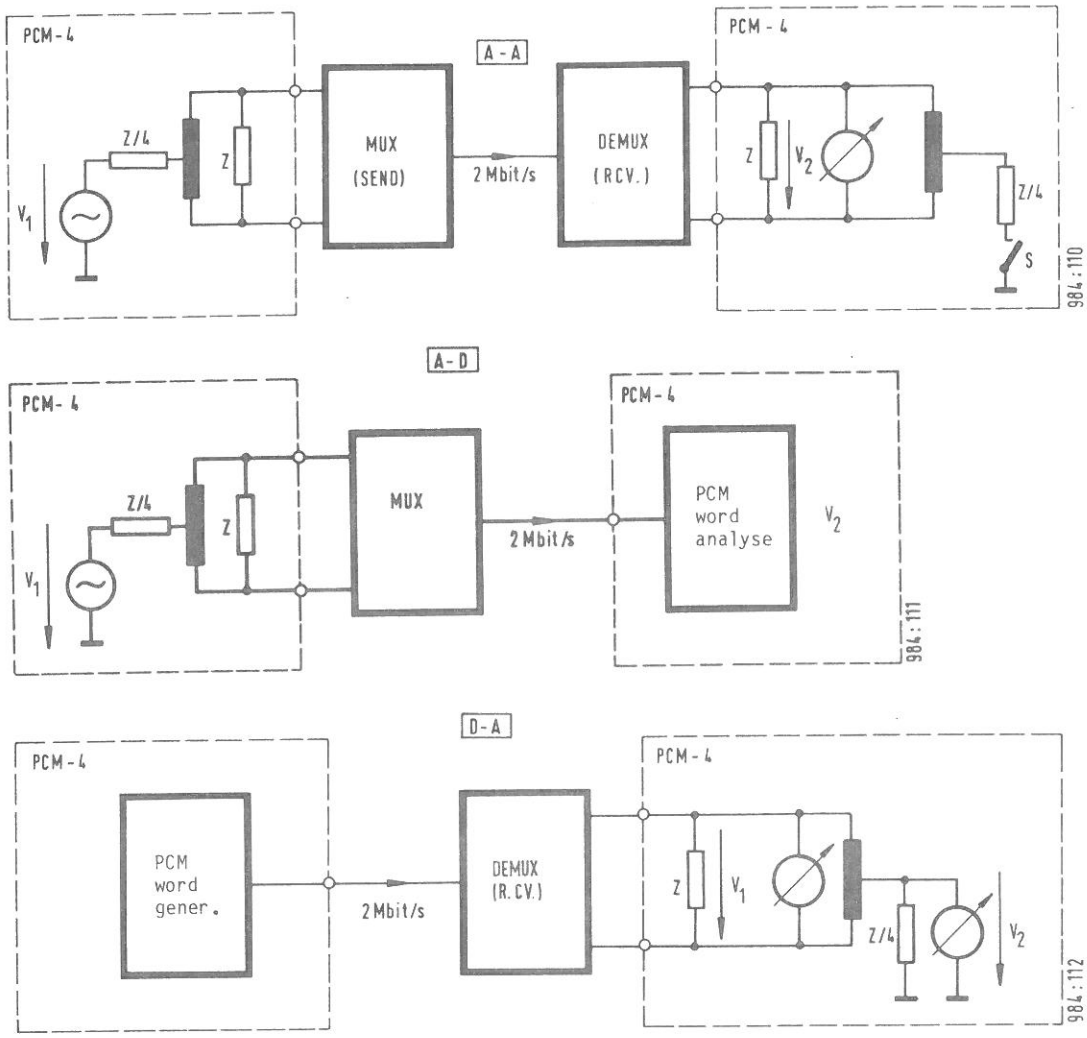
Figure 9.2.29-4 Test method used by the PCM-4



Data / Addr.	7	6	5	4	3	2	1	0
W53	1	0	0	0	0	1	0	0
W54	0	0	0	0	0	0	0	0

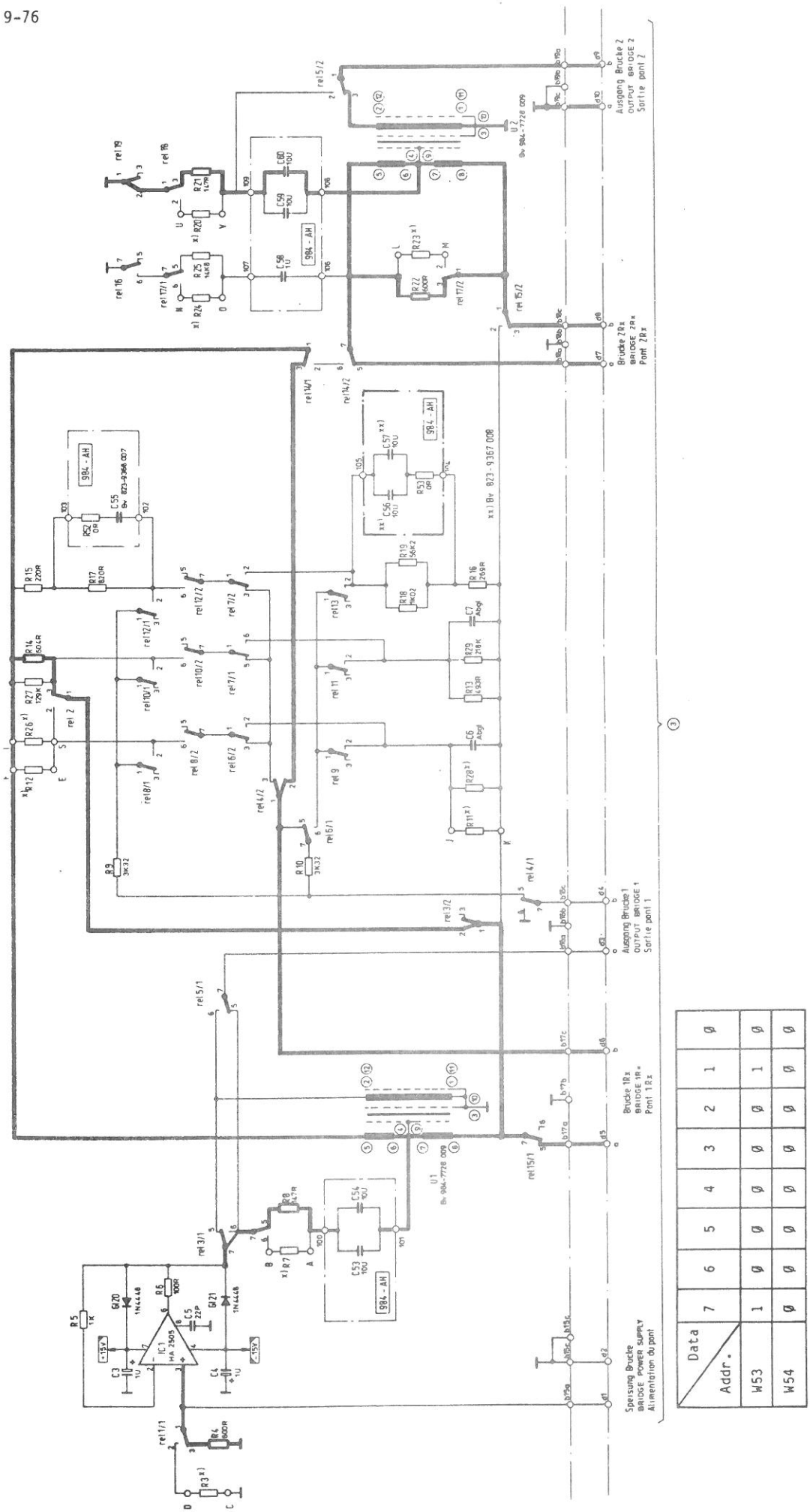
Figure 9.2.29-5 B21 measuring signal balance ratio

Measurement mode



LCTL ≙ longitudinal conversion transfer loss

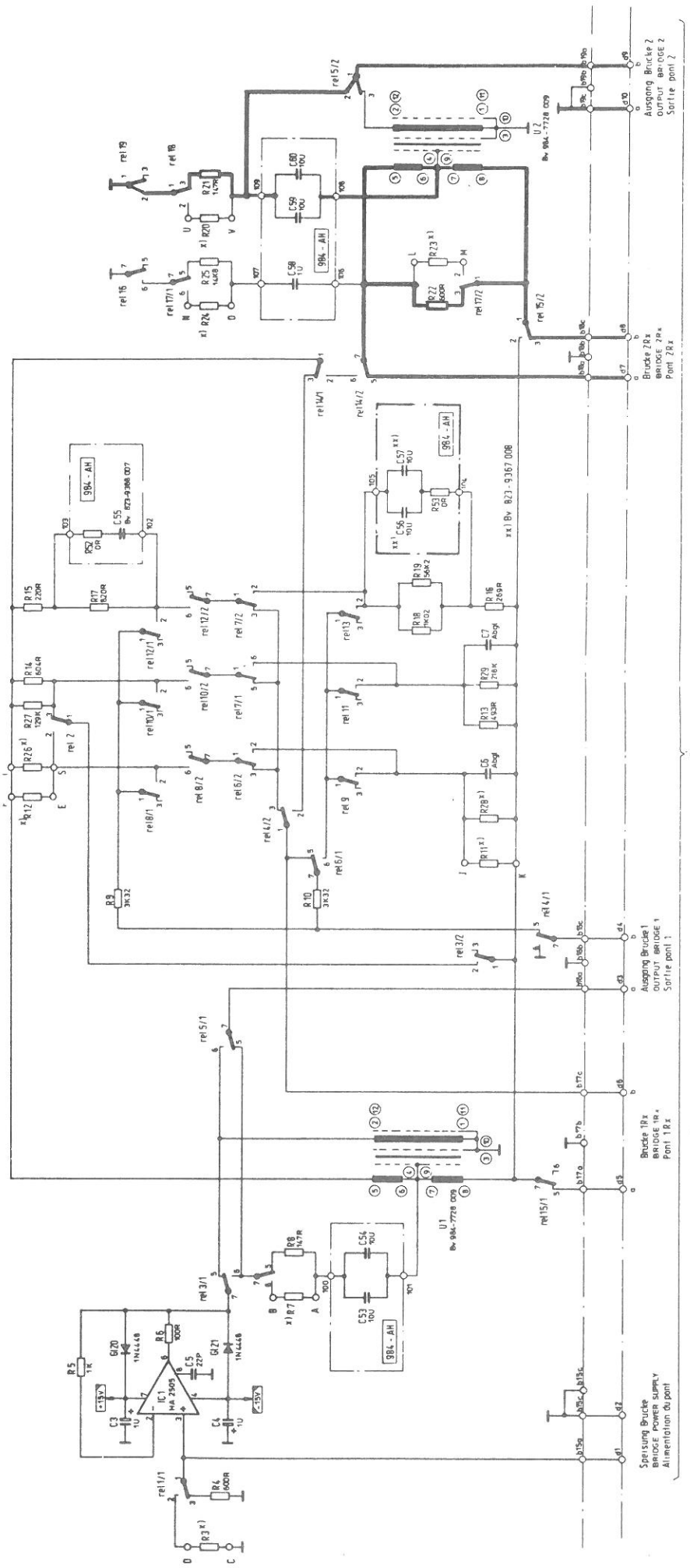
Figure 9.2.29-6 LCTL measurements (measurement mode B 31)



Data / Addr.	7	6	5	4	3	2	1	0
W53	1	Ø	Ø	Ø	Ø	Ø	1	Ø
W54	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø

LCTL ≅ longitudinal conversion transfer loss

Figure 9.2.29-7 B31: LCTL measurements [A-A], [A-D]



Data / Addr.	7	6	5	4	3	2	1	Ø
W53	1	Ø	Ø	Ø	Ø	1	1	Ø
W54	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø

Figure 9.2.29-8 B31: LCTL measurements [D-A]

9.2.30 CODIRECTIONAL OUTPUT 120 Ω [984-AJ] (15)

Description of option using circuit diagram 984-7515

Function in PCM-4:

Option 984/00.02 provides the PCM-4 with an output interface for codirectional 64 kbit/s CCITT signals.

Operating modes of option 984/00.02

TX 64:

The interface derives the "8 kHz PDG-64" clock (4a) and the "64 kHz PDG-64" clock (5a) from "64 kHz RX64" (9c) or "64 kHz TX2M" (8a), the derived clocks are used by the PDG-64. The bit stream received by the PDG-64 "64 kbit/s PDG-64", is integrated into a 64 kbaud signal which also contain the 8 kHz octet information and the 64 kHz clock information are stipulated by the CCITT. The 64 kbaud signal can be jittered at Bu 1 if a jitter generator is looped in between connector II and connector III.

DEMUX:

In the DEMUX mode the "64 kbit/s RX2M" (7c) signal is inserted in the 265 kbaud signal, which synchronises the PLL to the "DEMUX 8 kHz RX2M" signal.
Connectors II and III for jittering the signal in the TX64 mode have no purpose when this mode is selected.

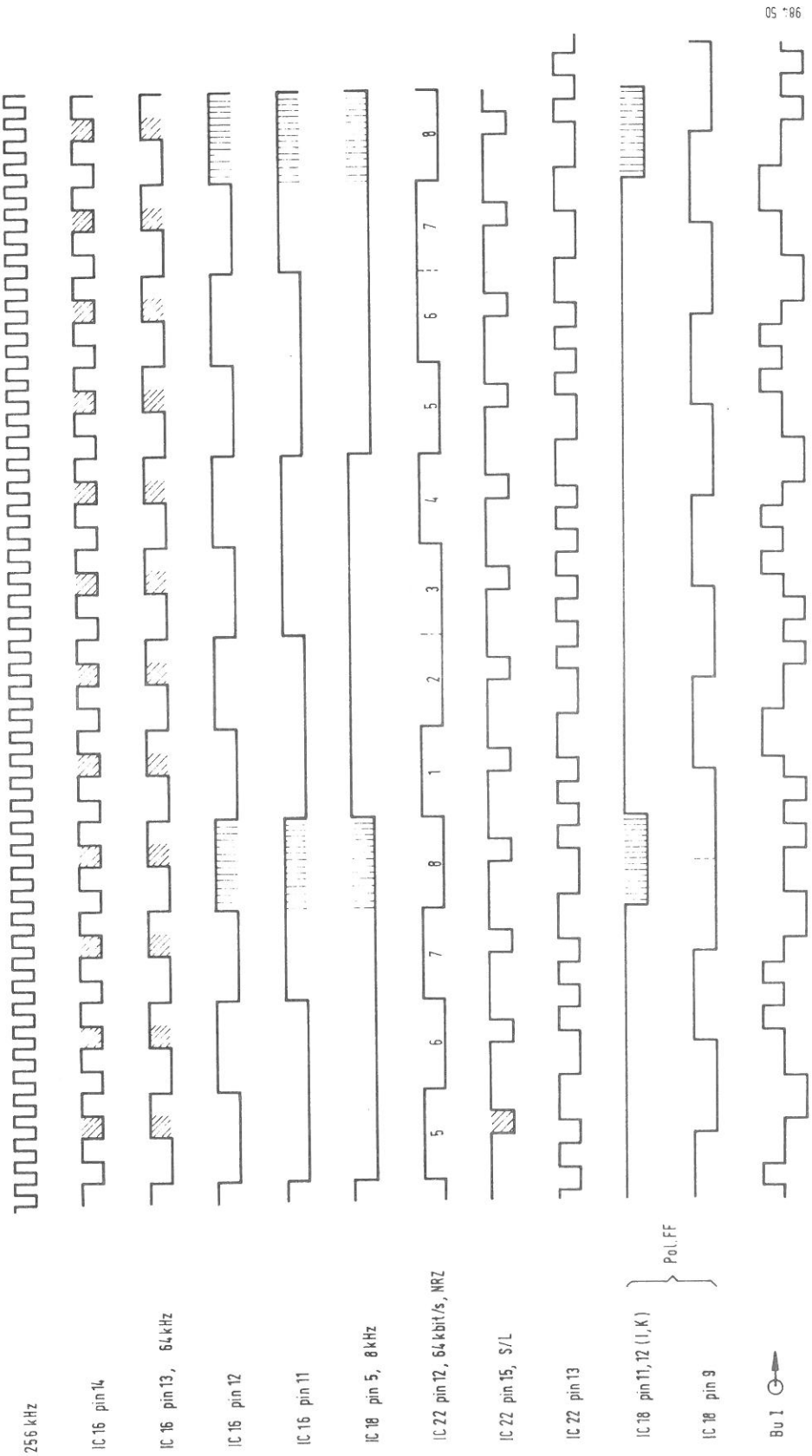


Figure 9.2.30-1 Timing diagram

9.2.31 64 kbit/s SERIAL TTL INPUT [984-AM] (30)

Description using circuit diagram 984-7530

Function:

Option 984/00.05 makes it possible for the PCM-4 to receive both codirectional and contradirectional serial TTL signals at the 64 kbit/s level.

Operating modes provided by option 984/00.05:

RX64 mode:

When this mode is selected, the codirectional receive signal is fed to the PDG-64 via IC 17/5, IC 4/2 and the board connection point b8. The 8 kHz clock signal and the 64 kHz clock signal are also connected to the PDG-64 without passing through any logic circuits.

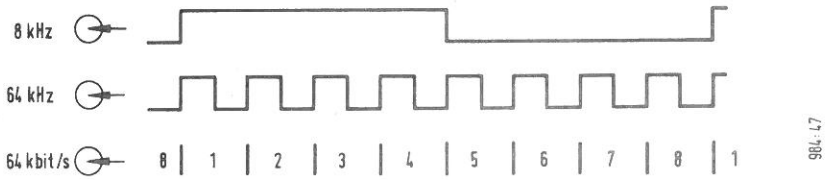


Figure 9.2.31-1 Timing diagram

MUX CODIRECTIONAL:

The 64 kbit/s signal which has been received is passed via board connector point ab to the PCM-30 generator where it is transferred to the 2 Mbit level.

Option 984/00.05 generates an 8 kHz signal which is delayed by 4 bits from the 8 kHz clock signal [47] and the 64 kHz clock signal [48]. The PLL in the PCM-30 clock circuit is synchronised to this signal. The "8 kHz input" clock and the "64 kHz input" clock are derived from this jitter-free PCM-30 clock, and so are available for the PSW (IC 7). To obtain a tolerance to jitter of half an octet (125 µs), the octet is transferred from memory 1 (IC 6) to memory II ($\frac{125\ \mu s}{2}$), the octet is transferred from memory 1 (IC 6) to memory II (IC 7) immediately after bit 4.

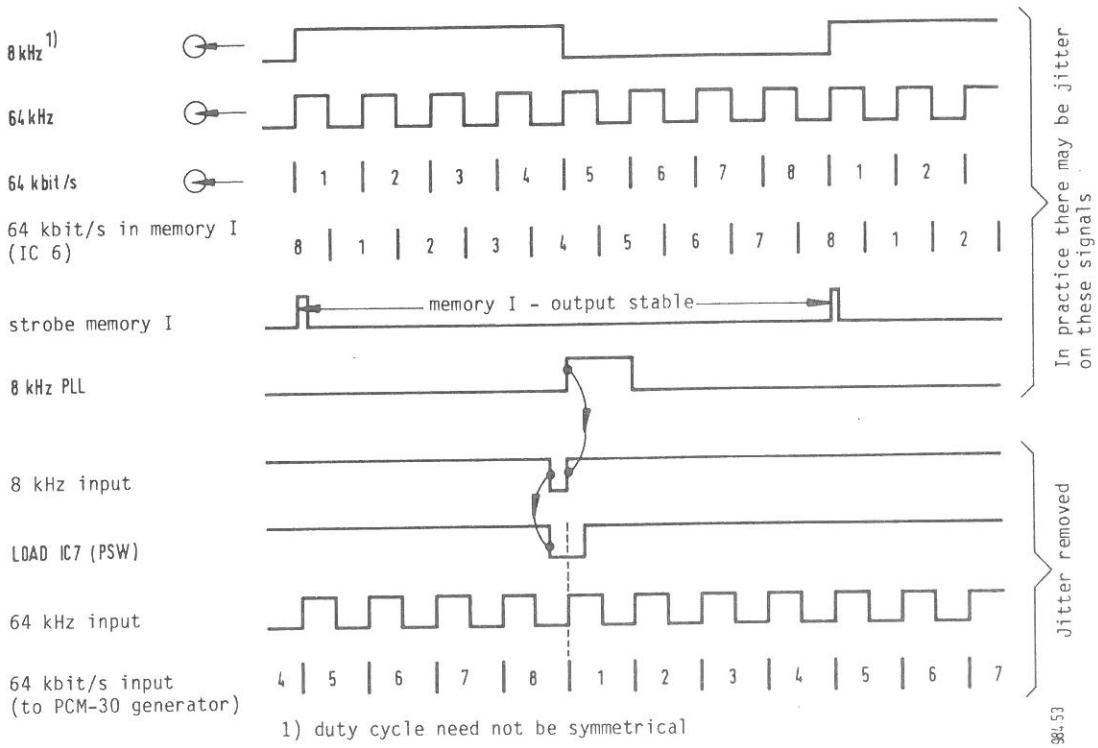


Figure 9.2.31-2 Timing diagram

MUX CONTRADIRECTIONAL:

The difference between contradirectional multiplex operation and codirectional operation is that the "8 kHz" clock and the "64 kHz" clock are sent instead of received. The 8 kHz balancing logic (IC 12, IC 13) ensures that the duty cycle of the 8 kHz clock is balanced [47].
ICs 6 and 7 have the same function as they did in the contradirectional MUX mode.

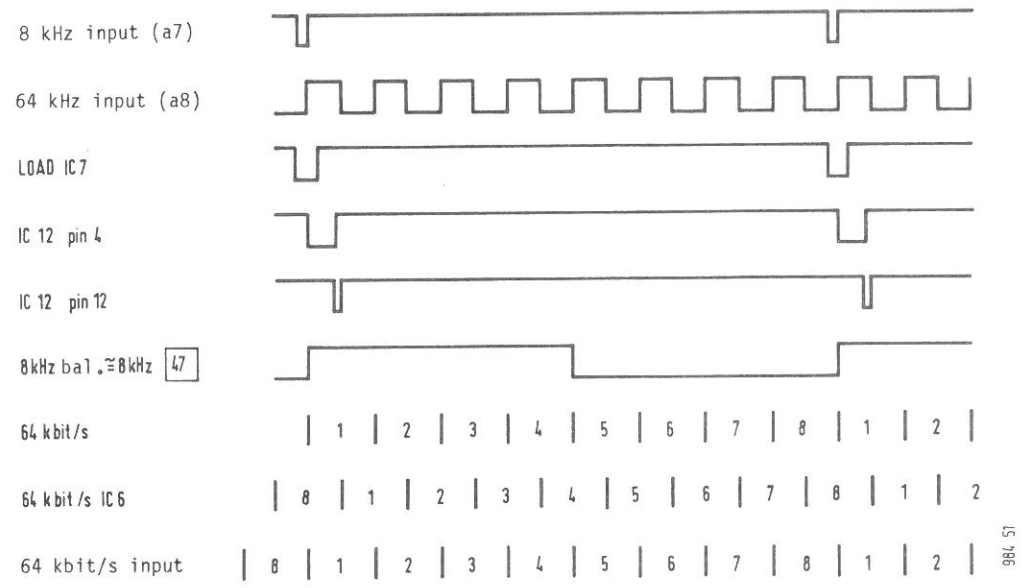


Figure 9.2.31-3 Timing diagram

MUX DF-64:

The contradirectional 64 kHz clock passes via C5 to Bu [48]. The 8 kHz data signal is not affected by the DF-64.

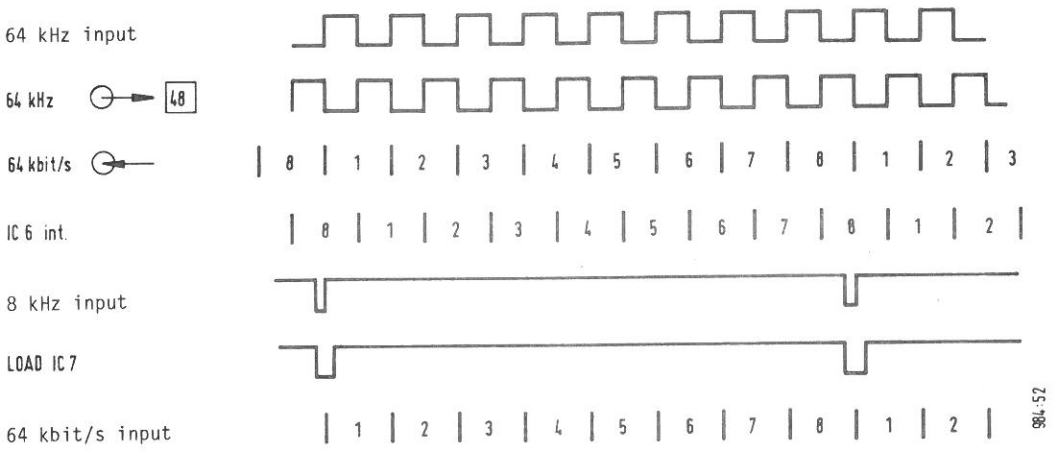


Figure 9.2.31-4 Timing diagram

CONTRADIRECTIONAL MUX PO-1:

PO-1 requires the 8 kHz information at the start of bit 8 and for a duration of $\frac{1}{2 \times 64\ kHz}$.

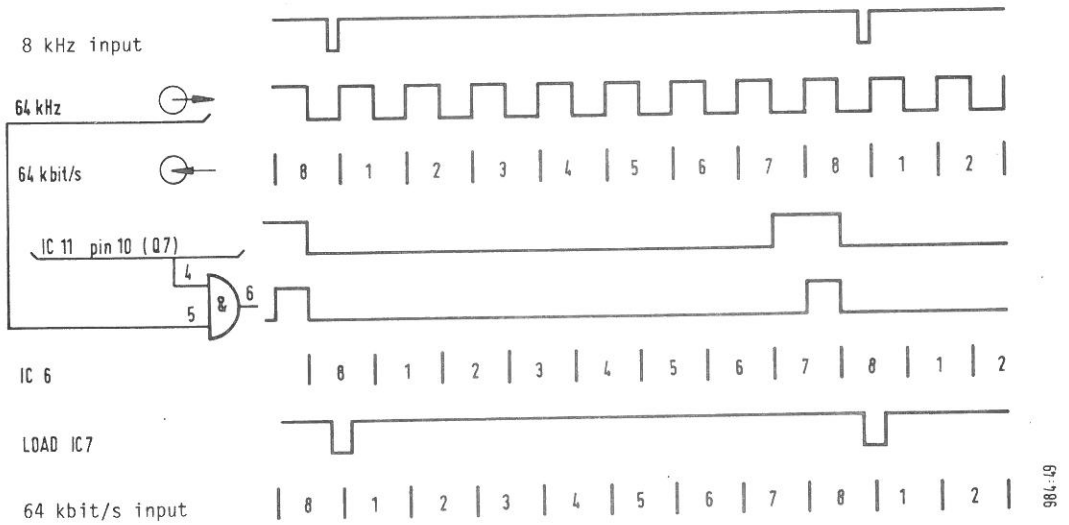


Figure 9.2.31-5 Timing diagram

CODEC-LOOP:

The 64 kbit/s input operates in the codirectional mode as a codec loop. The 64 kbit/s signal [46] undergoes serial/parallel conversion and is passed to the 64 kbit/s output via IC 1.

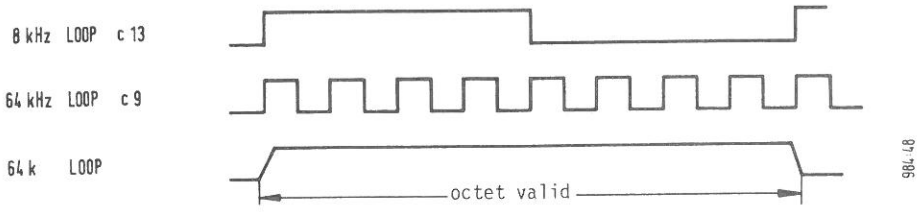


Figure 9.2.31-6 Timing diagram

9.2.32 64 kbit/s SERIAL TTL OUTPUT [984-AN] (31)

Description using circuit diagram 984-7532

9.2.32.1 Description of the 64 kbit/s output

Function:

Using this option, the PCM-4 can send serial TTL signals in both the codirectional and contradirectional mode at the 64 kbit/s level.

Option 984/00.06's operating modes

TX64 CONTRADIRECTIONAL (8 kHz, bit 1):

The difference between this operating mode and the TX 64 contradirectional mode (8 kHz 1 bit) is the positive going edge of the incoming 8 kHz signal which indicates the start of bit 8. The PDG-64 however needs this edge at the start of bit 1. IC 22 provides the necessary 8 kHz delay of 1 bit.

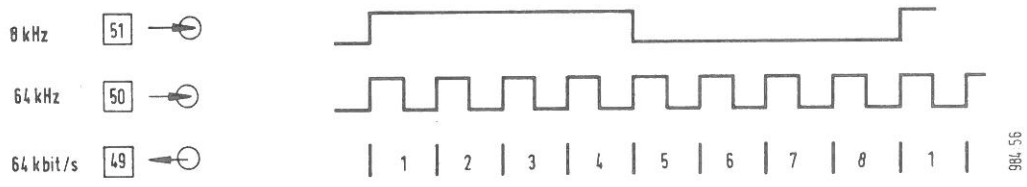


Figure 9.2.32-1 Timing diagram

TX 64 contradirectional (8 kHz, bit 8):

The difference between this operating mode and the TX64 contradirectional mode (8 kHz 1 bit) is the positive going edge of the incoming 8 kHz signal which indicates the start of bit 8. The PDG-64 however needs this edge at the start of bit 1. IC 22 provides the necessary 8 kHz delay of 1 bit.

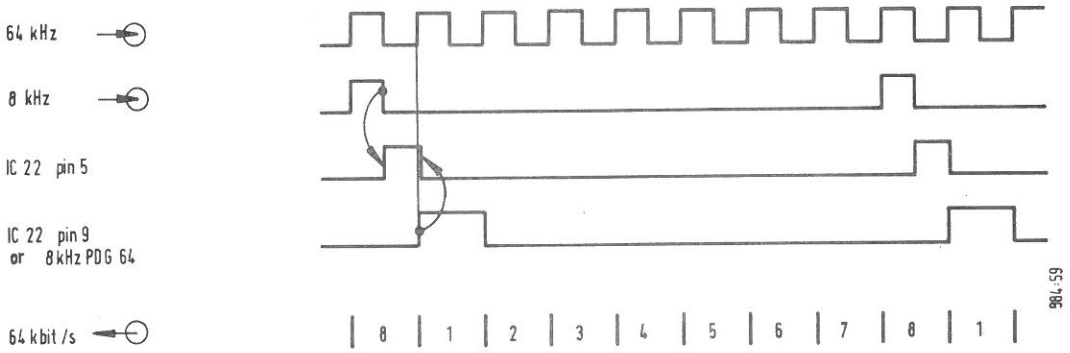


Figure 9.2.32-2 Timing diagram

TX CODIREKTIONAL:

Both clocks at [50] and [51] are output by the 64 kbit/s TTL output in codirectional mode. The board gets these clock signals either from the board connection points 9c, 13c from 4a or from 7a, 7b.
In order to send the 8 kHz signal at [51] with a balanced duty cycle, it is passed through the balancing logic circuit comprising IC 18/1/2 and IC 20.

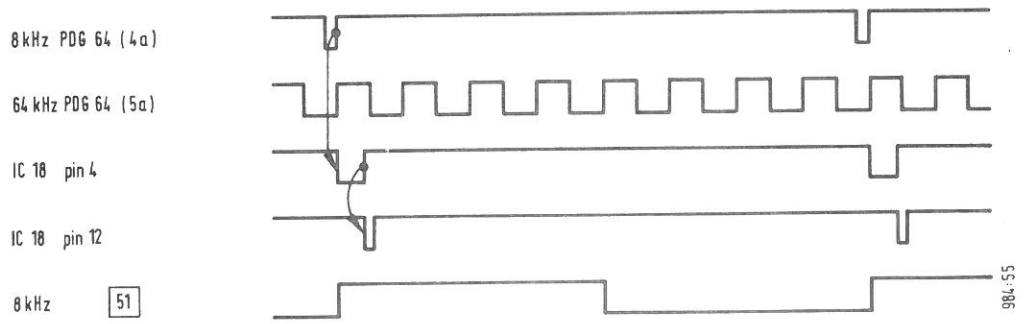


Figure 9.2.32-3 Timing diagram

CODEC LOOP CONTRADIRECTIONAL:

In the contradirectional CODEC loop, the octet transfer control, generated by the three clocks at [50], [51] and 13c, converts the parallel "64 k LOOP" octet into the serial "64 kbit/s" signal at [49].

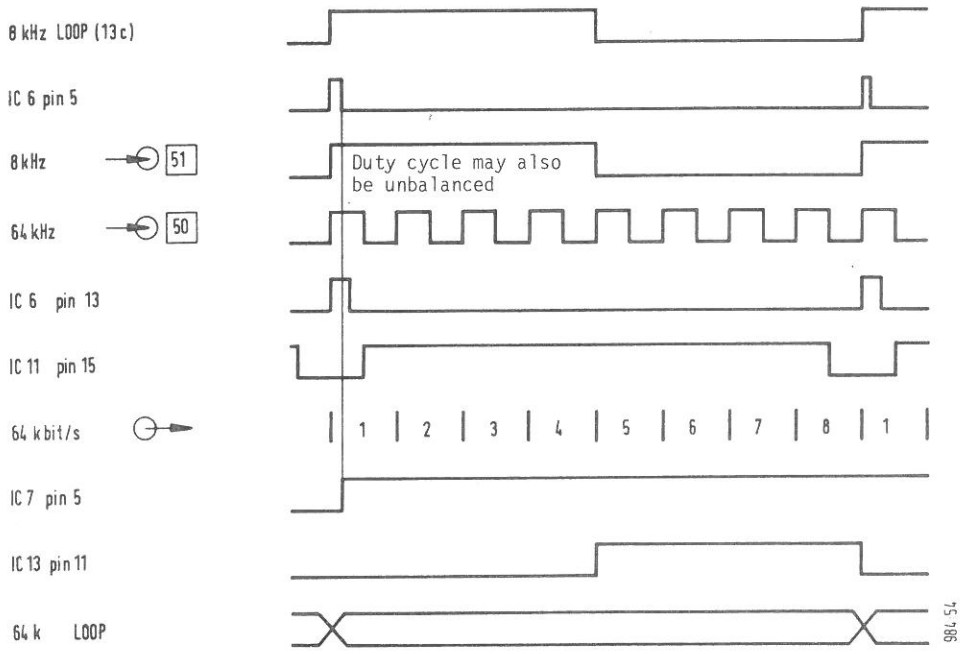


Figure 9.2.32-4 Timing diagram

CODEC LOOP CODIRECTIONAL:

The main difference between the codec loop mode and the contradirectional loop mode is that the clocks at [50] and [51] are sent and not received by option 984/00.06.

DEMUX:

In the DEMUX mode, option 984/00.06 sends the "64 kbit/s output" signal at board connection point 7c in codirectional mode.

9.2.33 64 KBIT/S PARALLEL INPUT [984-AO] (32)

Description using circuit diagram 984-7532

Function:

Option 984/00.07 makes it possible for the PCM-4 to receive parallel octets at the 64 kbit/s level.

Option 984/00.07's operating modes:

RX 64:

The option receives parallel octets and an 8 kHz signal, the 8 kHz signal indicates the following incoming octets.

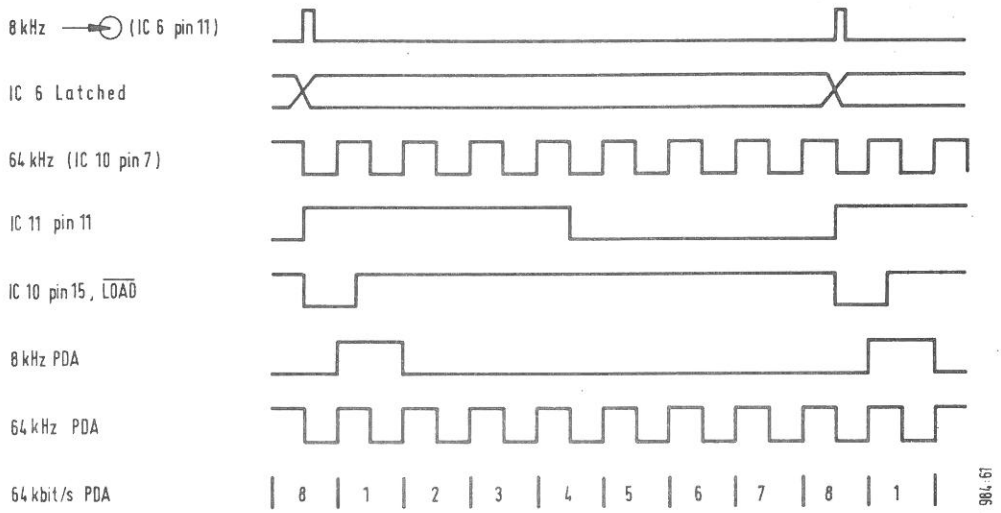


Figure 9.2.33-1 Timing diagram

MUX CONTRADIRECTIONAL:

In multiplex mode, the 64 kbit/s signal to be received by option 984/00.07 is connected to board connection point a6 (64 kbit/s input).

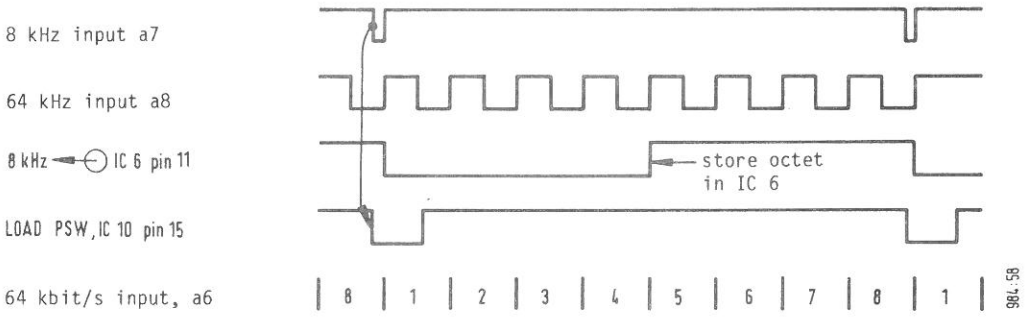


Figure 9.2.33-2 Timing diagram

CODEC LOOP:

In this operating mode, the board receives the 8 kHz signal (pin 6) as well as the octet (bit 1 to bit 8) via Bu 1. The PLL (IC 8) and the divider (IC 11) derive the "64 kHz signal from REC" and the "8 kHz signal from REC" from the 8 kHz signal. The octets are looped in parallel mode via IC 6 to IC 20.

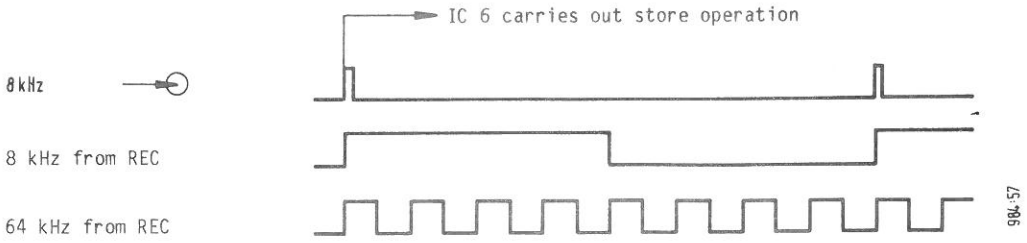


Figure 9.2.33-3 Timing diagram

9.2.34 64 KBIT/S PARALLEL TTL OUTPUT [984-AP] (33)

Description using circuit diagram 984-7533

Using the 984/00.08 option the PCM-4 can send octets in parallel in both co- and contradirectional modes.

Option 984/00.08's operating modes:

TX 64 contradirectional:

Both clocks, i.e. "8 kHz PCG-64" and "64 kHz PDG-64" (derived from the 8 kHz signal at Bu 3, pin 6 using PLL (IC 22) and the divider IC 21) clock the PDG-64 which applies the 64 kbit/s signal to 6a.
This serial data stream undergoes serial to parallel conversion in IC 18 and is fed to IC 23.

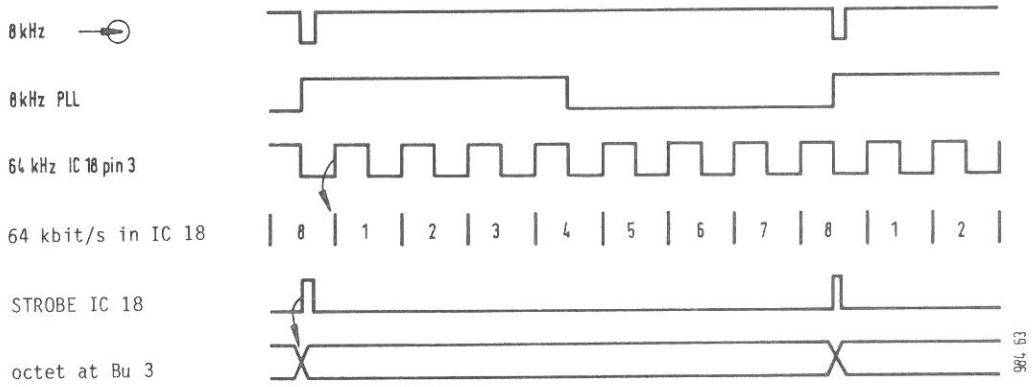


Figure 9.2.34-1 Timing diagram

CODIRECTIONAL:

The main difference betweeen the codirectional mode and the contradirectional mode is that the 8 kHz clock is sent instead of being received.
In order to send this 8 kHz clock with a balanced duty cycle, it is passed through a balancing logic circuit (IC 17/1/2, IC 20). The clock can be provided by the board connection points 7a, 4a or 13c.
The following timing diagram is for the DEMUX mode.

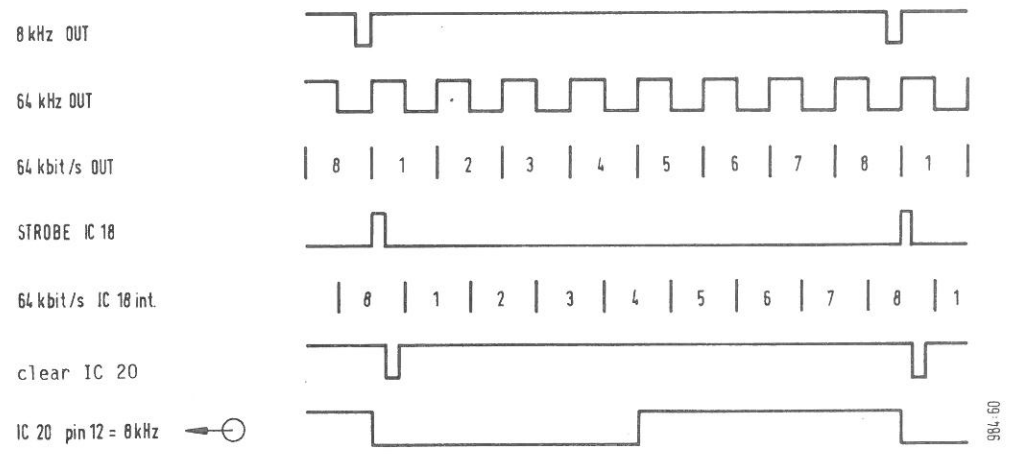


Figure 9.2.34-2 Timing diagram

CODEC LOOP contradirectional:

The octet tranfer control makes it possible for the 8 kHz signal (Bu pin 6) to loop through the octet "64 k LOOP" to Bu 3 at any time. The 64 k LOOP signal and the 8 kHz signal (Bu 3 pin 6) must not be allowed to meet.

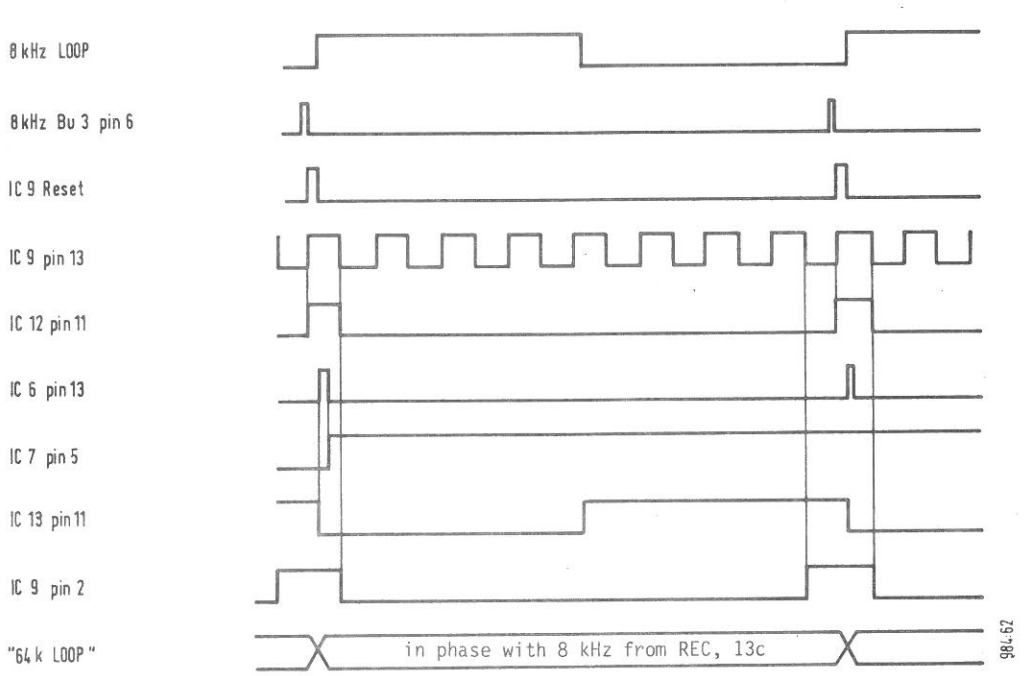


Figure 9.2.34-3 Timing diagram

CODEC LOOP codirectional:

Unlike the codirectional codec loop mode, the 8 kHz signal (Bu pin 6) is sent instead of being received. Depending on the clock that has been selected, it is derived from either the 8 kHz LOOP signal (13c) or from the 8 kHz PDG-64 signal (4a).

9.2.35 REGULATOR (2)

see section on the preliminary stage 9.2.27

9.2.36 ADC 2 (34)

see section 9.2.9 (ADC 1)

9.2.37 PCM-30 RECEIVER 2 [984-AS]

Description using circuit diagram 984-7508

PCM-30 receiver 2 is connected to PCM-30 receiver 1 via the parallel 8 bit bus B1 to B8 to split up the PCM frame into its constituent frame and time slot words.

The computer interface is bi-directional so that data can be sent and received. The direction of flow of the data is changed by the bus transreceiver IC 4. When a write procedure is taking place the direction A → B is selected for IC 4. The $\overline{\text{W PCM-IF}}$ pulse is connected to the addressed memory module via decoder IC 1 and the setting data are stored.

There is a memory for each of the following between the PCM bus B1 to B8 and the data bus D0 to D7: frame alignment word, not frame alignment word, TS 16 frame Ø, TS 16 frames 1 to 15 and the telephone channel octet. The memories are clocked using appropriate frame of time slot clocks from the frame circuit (on the PCM-30 rec. 1). When a read operation is being performed in IC 4 the direction is B → A. The $\overline{\text{R PCM-IF}}$ pulse is connected to the addressed memory module via decoder IC 2 and its tristate outputs are selected.

When a memory is being stored no attempt must be made to store a new data word. The OR gate IC 24/3 checks whether the $\overline{\text{R PCM-IF}}$ pulse and one of the frame or time slot signals overlap. If this is the case, a memory pulse is prevented with flip-flop IC 9/2 and the OR gate IC 24/2. The four alarm signals $\overline{\text{NO SIGNAL}}$, $\overline{\text{AIS}}$, $\overline{\text{NO FRAME}}$ and $\overline{\text{NO EXTENDED FRAME}}$ are output as interrupt signals via IC 38/1 and IC 10/1 (23a). At the same time monostable IC 37 generates a memory pulse for the alarm latch IC 40. This latch can be read with the decoded addresses $\overline{\text{RD1}}$ and $\overline{\text{RD2}}$. $\overline{\text{RD1}}$ is used to read the current status of the alarm signals, $\overline{\text{RD2}}$ is used to read the last stored alarm status. The signalling bits for the occupied receive time slot are stored in the 4-bit memory IC 12 and fed via 11a, 12a 11b and 12b to connector 1 [62] to the PCM-30 receiver 1. Using multiplexer IC 15 one of the four signalling bits is connected via 10a to the signalling distortion board. The TRISTATE buffer IC 11 is in its high impedance state in normal operation. The PCM-30 generator provides display multiplexer IC 20 via 17a, 18a, 19a and 20a with the signalling bits of the occupied send time slot. In the LOOP SELECTED TIME SLOT mode the signalling bits in the occupied receive time slot are connected to the PCM-30 transmitter via IC 11.

The LED display below the screen is driven by PCM-30 receiver 2 IC 19 when the RX 2048 kbit/s mode has been selected and by the 64 kbit/s input when the RX 64 kbit/s mode has been selected. Multiplexer IC 18 selects the memory clock for IC 19 according to the selection shown by the display.

The 64 kbit/s interfaces to the clock filter (PDA-64) or to the 64 kbit/s output are basically the same. The 365 kHz octet signal T 8 is divided down to 64 kHz by IC 30 or IC 35. The flip-flops IC 31/1 or IC 31/2 supply the charging pulse for the parallel/serial converter IC 33 or IC 36.

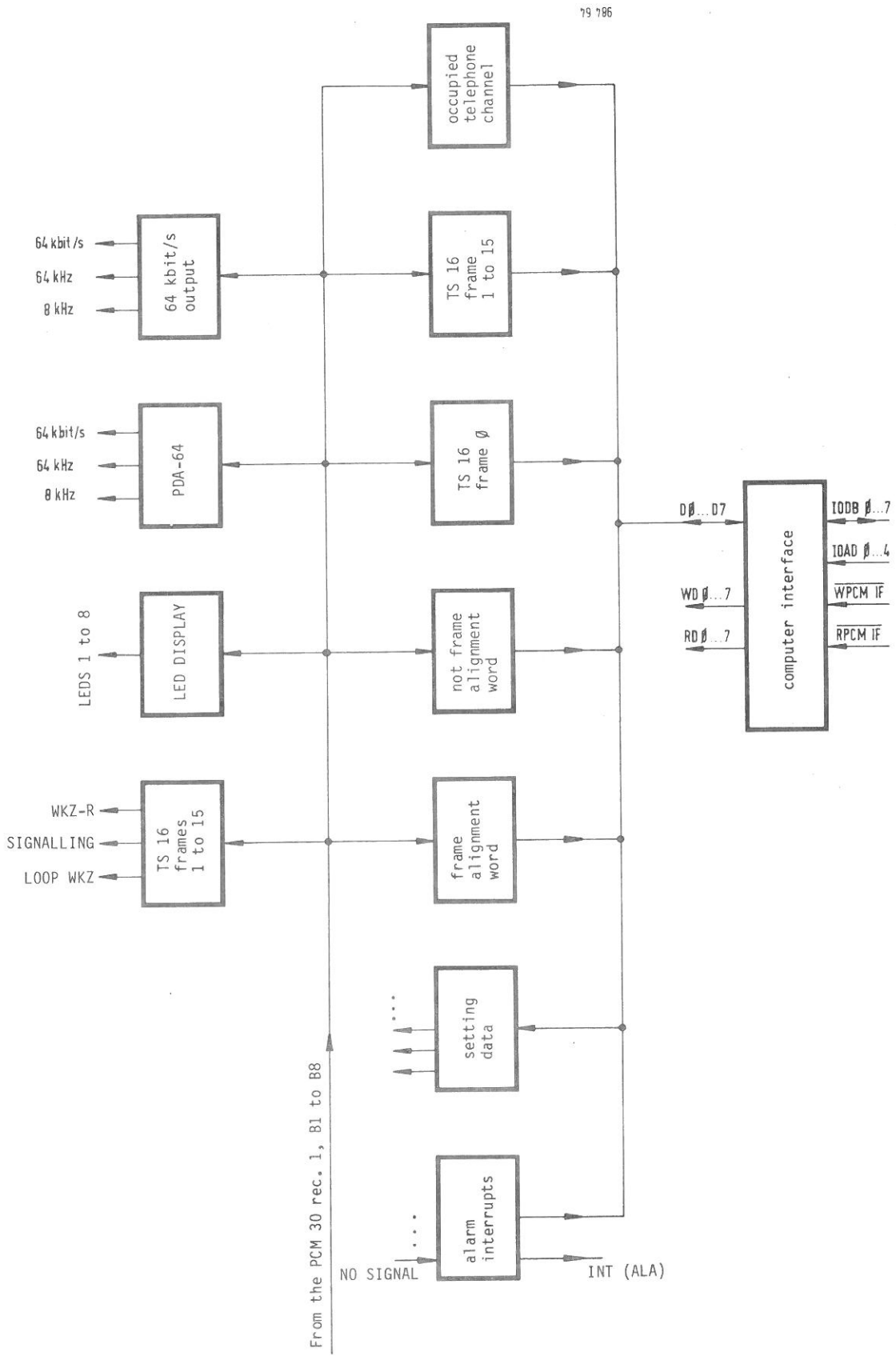


Figure 9.2.37-1 Block circuit diagram of PCM-30 receiver 2

9.2.38 DATA BACKUP [959-AV] (1)

Description using circuit diagram 959-7501

When the PCM-4 is switched off, one wants to retain the data in the RAM of the master processor CPU-2A/1. The following are required:

- Batteries to supply the RAM
- Charger for the batteries
- Battery power/mains power switchover
- Sense line to indicate the current status fo the power supply

1. Battery supply

Batt 1 to batt 3 supply the RAMs via Gl 2 and R4 (3 V $\leq V_{bat} \leq$ 5.5 V). Gl 2 prevents uncontrolled charging. R4 limits the short circuit current.

2. Charger

T1 is used as a charger (connected up as a current source).

3. Battery/mains selection

Using T2, V_{bat} is connected at low impedance to the +5 V rail. The base current is basically determined by R7. If the current through T2 is too large, then T3 conducts and T4 is cut off. The base current through T2 is reduced to a level that prevents thermal overloading when a short-circuit occurs.

When the 5 V supply drops below a threshold of 4.2 V, T6, T5 and consequently T2 are cut off. The batteries then take over the power supply to the RAMs. the same applies when the +12 V supply drops below a certain level.

4. Alarm line

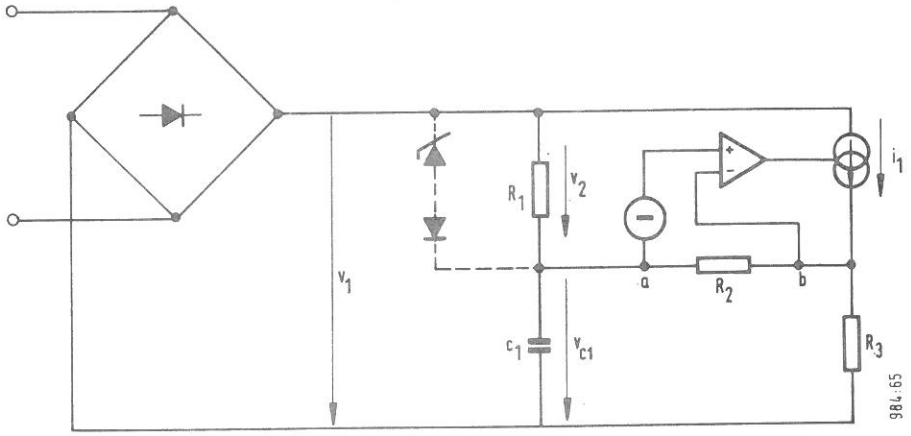
To allow a proper master processor power-down, MAINS OFF must be used to indicate that the power supply will only remain in tolerance for a short time ($\leq$ 1 ms). This requires special program to carry out all the necessary precautions. When the voltage across the electrolytic capacitor in the regulator (unregulated voltage) drops below 16 V, these conditions are met (comparator IC 21/1). A hysteresis of about 3 V (referred to the unregulated voltage) is produced by R26 and Gl 23. When the instrument is switched on a check is carried out to find out if the +5 V supply is below 4.6 V (IC 21/2). MAINS OFF is therefore high if the unregulated voltage is < 16 V or the +5 V supply is below about 4.6 V.

9.2.39 DC LOOP HOLDING CIRCUIT [984-BA] (37)

Description using circuit diagram 984-7537

The two-wire send and the two-wire receive modes, the dc exchange loop is maintained by a special circuit when measurements are being made on telephone networks. This circuit presents a high impedance to ac signals and ensures a minimal dc operating voltage.

The circuit that provides an inductance of about 1000 H is connected in parallel with the input section or the generator section. It is connected into one of the branches of a diode bridge and so will function whatever the polarity at the input is. The circuit is dimensioned for a frequency range of 20 Hz to 20 kHz, dc currents of 0 to 100 mA and levels to +13 dB.



Simplified circuit diagram

The voltage (a-b) of the frequency dependent bridge is monitored. An ac current equal to V_{C1}/R_3 and controlled by the regulator amplifier flows through R3 no matter how large the dc current is. Because

$V_1/(1 + jw\ C_1\ R_1) = V_{C1}$ and

$Z = V_1/i_1 = R_3 + jw\ C_1\ R_1\ R_3$, L is $C_1\ R_1\ R_3$.

The dc voltage component V_1 is given by the equation

$V_1 = i_1\ R_3 + V_2\ (1 + R_1/R_2)$.

Because of the large value of the time constant, $\tau = R_1C_1$, C_1 is charged rapidly via the diode array.

The diodes also limit the voltage so preventing damage.

Description using circuit diagram:

Assume that C7 is not charged and a current whose polarity is not material is applied to the circuit. Initially the diode bridge Gl 1, 2, 5, 6 determines the direction of current flow. If the current is below 2 mA it will flow via R11, Gl 9, Gl 10 and C7, this will cause C7 to be charged to approx. 1.2 V. The voltage at these points (a-b) causes T2 and T6 to conduct and take the current flowing through R11 using the cascade stage (T1, T5). The circuit has been dimensioned so that the operating point voltage is less than the initial holding voltage (22 V → 16 V). This means that the spurious capacitance of the zener diode Gl 9 is decoupled via the diode Gl 10 which is off.

If the holding current is greater than 2 mA, the excess current is taken by transistor T9. R13 reduces the feedback of T9 and largely determines the high impedance of the whole circuit.

If the part of the circuit that carries the current has an ac current applied to it, then this current is superimposed on the collector base voltage of T9 and the base stage containing T1 and T5. The base stage prevents the ac voltage from reaching T2 to prevent feedback. T2 is operated at V_{CE} = 1 V and I_B = 10 nA. The loop gain is ≈ 40 dB.

9.2.40 CRC CIRCUIT [984-AY] (9)

Description using circuit diagram 984-7509

The CRC circuit can be used for CRC-4 for the 2 048-kbit/s interface and CRC 6 for the 1544 kbit/s interface. This means that this board can be used for both versions of the PCM-4. The abbreviation CRC stands for cyclic redundancy check, the number 4 or 6 indicates the length of the shift register with feed back that has been used. The circuit is divided into a generator section and a receive section. The main component in the circuit is the PCM-CRC 4/6 gate array IC 5. When the loop through mode has been selected, the generator section inserts the checksum that has been found by the CRC register into the PCM bit stream. In the CRC 4 mode, the CRC-4 multiframe alignment word (CRC-4 mfas) and the spare bits S_1 and S_2 are also inserted.

The CRC error generation circuit on the send side is accommodated on the CRC circuit and the PCM-30 generator. The time base which comprises the counters IC 8 and IC 9 delivers the $\overline{\text{CRC ERR START}}$ signal to a2 at intervals of 1 s (CRC 4) or 999 ms (CRC 6). In this way, the port circuit for the error pulses (IC 16, IC 12/2) are opened; at the same time the error counter on the PCM-30 generator or the T1 generator is started. This error counter closes the gate circuit when the required error count has been reached. The counter uses the signal CRC ERR STOP to do this. In the CRC 4 mode, the SMFRMS-T signal is used as the actual error signal, the interval between pulses is 1 ms. In the CRC 6 mode the FRM1-T signal is used, the interval between pulses is 3 ms. This means that an error rate of 1 in 1000 (0.1%) to 999 in 1000 (99,9%) can be reached in the CRC 4 mode and error rates of 1 in 333 (0.3%) to 332 in 333 (99.7%) can be reached in CRC 6 mode. In the CRC 4 mode it is necessary to delay the error pulses using IC 10 to match their timing to the internal part of the CRC error injection circuit in gate array IC 5. A CRC error is equivalent to the inversion of bit 2 in the CRC checksum. The error is equivalent to the inversion of bit 2 in the CRC checksum. The error input MFAS ERR IN (IC 5, pin 5) generates the CRC 4 multiframe alignment words with a 1 in bit position 4. In the CRC 4 mode the receive section synchronises itself to the incoming PCM frames and outputs a pulse at the TRUE MFAS output (IC 5 pin 28) each time a correct CRC 4 multiframe alignment word is received. The CRC 4 MFAS monitoring circuit, comprising the counter for correct CRC 4 MFASs (IC 15) and the 8 ms counter IC 14, checks that at least two correct CRC 4 MFASs have been received with defined periods of 8 ms. If this is not the case, output $\overline{Q}$ of IC 13/2 goes high and so triggers IC 17/1. Output $\overline{\text{SYNC. RESET}}$ (b8) then goes low and initiates a new synchronisation procedure.

If at least two correct CRC MFASs have been detected within 8 ms, the CRC error evaluation mode is selected. No further monitoring of the CRC 4 multiframe alignment takes place.

The CRC checksum for the incoming PCM frame is compared with the reference check sum generated by IC 5 in the receive section. If the checksums are not the same, an error pulse is output at the CRC ERR OUT output (pin 27). Counters IC 30 and IC 31 form the time base (TP 5) for the error evaluation circuit in the receive section. The time base output signal (TP 5) resets the error counter, comprising IC 28 and IC 29, at 1 s intervals in the CRC 4 mode and at 999 ms intervals in the CRC 6 mode. If counter overflow occurs a new synchronisation procedure is initiated via b8; the alarm signal NO EXTENDED FRAME is output at a8. The DIL switches S1 and S2 can be used to set the overflow threshold.

In the CRC 6 mode, the shift register IC 33 delays the enablement of the time base and the error counter by two multiframes (6 ms).

In the CRC 4 mode the spare bits S1 and S2 are decoded from the received PCM frame by IC 5. The results are stored in IC 22 and so can be interrogated via the processor interface.

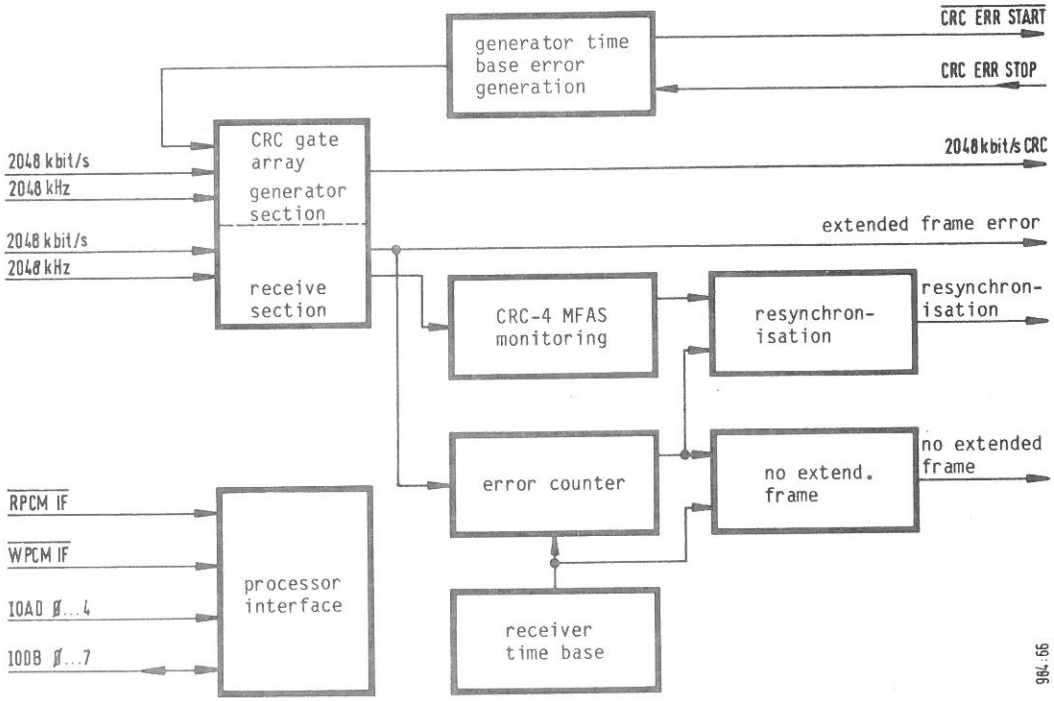


Figure 9.2.40-1 Block circuit diagram of the CRC circuit

Setting the CRC error detection facility with the DIL switches S1 and S2

a) BN 984/01, CRC 4:

The error threshold is set to 91.4% in the factory, i.e. to 914. Errors in any interval will cause a resynchronisation.

$$\text{Error threshold in \%} = \frac{\text{Number of CRC errors per interval (1 s)}}{1000} \times 100$$

$$= \frac{914}{1000} \times 100 = \underline{91.4\%}$$

Switch settings S1, S2

N = error threshold -1

i.e. for the standard setting is N = 914 - 1 = 913

$N = 913_{dec} \cong \underbrace{\emptyset\ \emptyset\ \emptyset\ \emptyset\ \ \emptyset\ \emptyset\ 1\ 1}_{S2}\ \ \underbrace{1\ \emptyset\ \emptyset\ 1\ \ \emptyset\ \emptyset\ \emptyset\ 1}_{S1}{}_{bin}$

S2/8 S2/1 S1/8 S1/1

b) BN 984/02, CRC 6:

The error threshold is set to 91.9% in the factory. i.e. to 306. Any errors that occur in a 999 ms interval cause resynchronisation.

$$\text{Error threshold in \%} = \frac{\text{No of CRC errors per interval (999 ms)}}{333} \times 100$$

$$= \frac{306}{333} \times 100 = \underline{91.9\%}$$

(rounded off to the 1st decimal place)

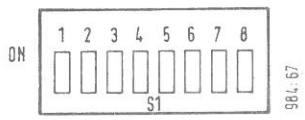
Switch settings S1, S2

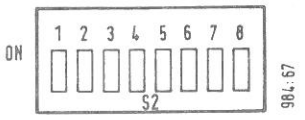
N = error threshold -1

i.e. for the standard setting N = 304 - 1 = 305

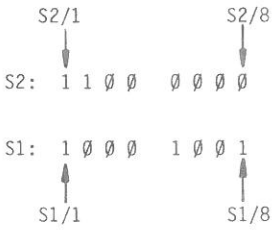
$N = 305_{dec} \cong \underbrace{\emptyset\ \emptyset\ \emptyset\ \emptyset\ \ \emptyset\ \emptyset\ \emptyset\ 1}_{S2}\ \ \underbrace{\emptyset\ \emptyset\ 1\ 1\ \ \emptyset\ \emptyset\ \emptyset\ 1}_{S1}$

S2/8 S2/1 S1/8 S1/1

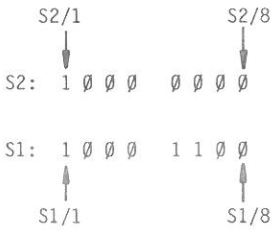




PCM-4 CEPT version BN 984/01



PCM-4 US version BN 984/02



9.2.41 LOWPASS FILTER 120 KHZ [OPTION]

Description using block circuit diagram 984-7541

If you want to measure low signal levels (e.g. in A81), the attenuator settings which are determined by the test program may be altered if the input amplifiers are overdriven by out-of-band spurious signals (magnitude of the spurious signal is considerably greater than the test signal); this will cause incorrect results.

As internal lowpasses are connected after the preamplifier and attenuator circuits, these spurious signals are only attenuated when they leave the input path. Due to this attenuation a normal test cycle will not recognise the spurious signal as a selective signal.

To stop incorrect results of this kind, the 120 kHz lowpass option can be connected to the input of the preliminary stage [984-AE].

The lowpass is used at spurious frequencies from about 220 kHz, return loss > 18 dB. Pole at 256 kHz $\pm$ 5 kHz a > 40 dB

9.2.42 IEEE 488 / <IEC 625> INTERFACE BUS CARD, BN 958, CIRCUIT DIAGRAM (91)

9.2.42.1 Functional description based on the block circuit diagram

Figure 9.2.42-1 is a simplified block circuit diagram of the <IEC 625> interface card.

The interface to the IEC bus with the necessary driver and receiver circuits is shown on the right-hand side.

The connection to the I/O bus of the device-internal microprocessor is shown on the other side.

For the microprocessor, the IEC bus interface represents a collection of input and output gates. It is via these gates that data are exchanged between the IEC bus and the device.

Data transfer between the IEC bus interface and the device is controlled by the IEC bus program. The PROMs in which this program is stored are located not on the IEC bus interface card, but in the device.

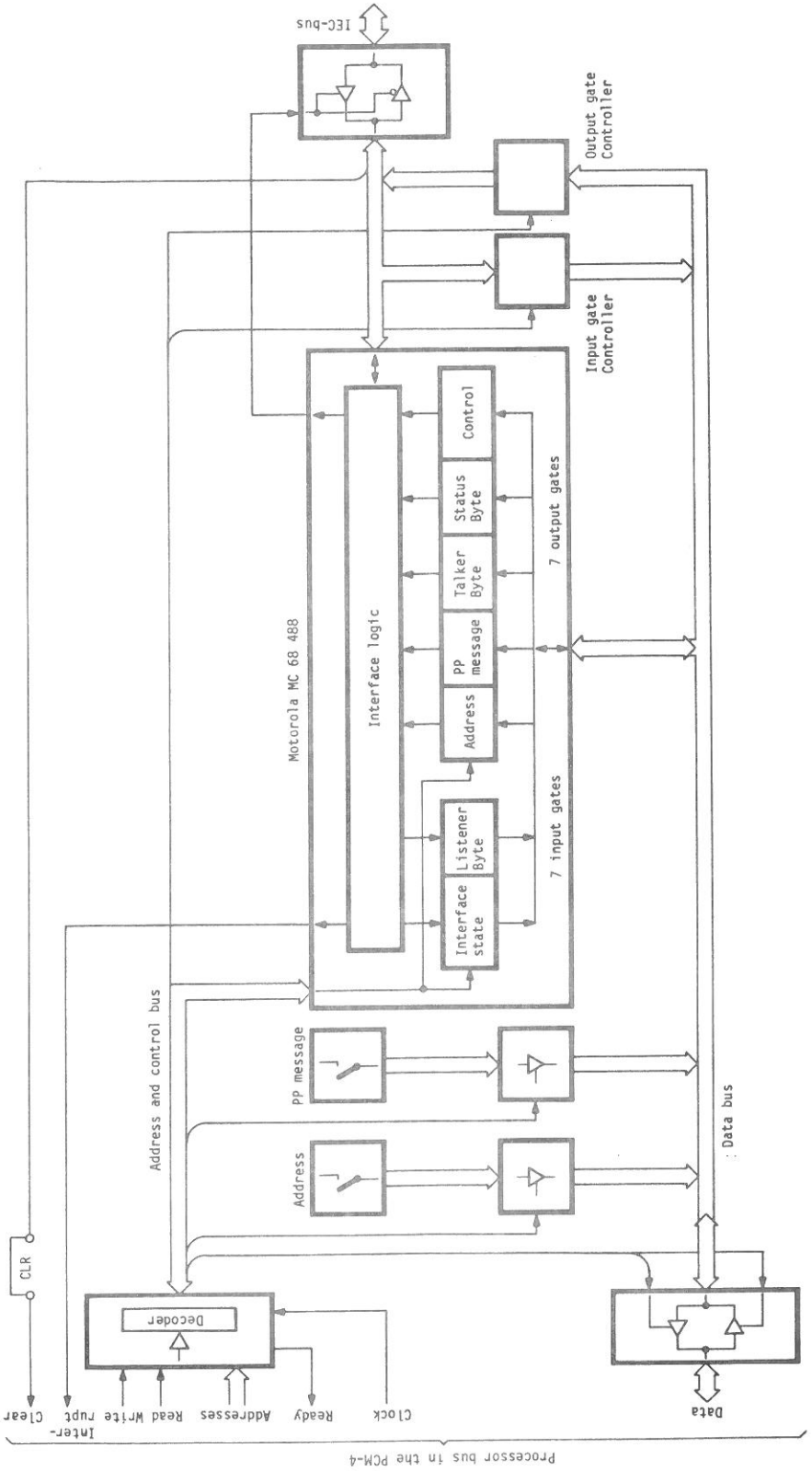


Figure 9.2.42-1 Block circuit diagram of the IEEE 488 / <IEC 625> interface bus card

9.2.42.2 Functional description of the card

The actual interface logic is located in the IEC bus interface module MC 68 488 from Motorola. This module handles the greater part of the interface tasks independently, i.e. without calling on the device-internal microprocessor. For example, it independently takes part in the IEC bus handshake cycle and decodes all messages transmitted on the IEC bus.

The interface states assumed on the basis of these messages are written into the corresponding input gates.

A further input gate acts as the transfer register for listener bytes. Listener bytes are the data transmitted from the IEC bus to the device while the device is addressed as listener, i.e. when setting parameters for the device are transmitted.

In addition to the input gates, the module also has output gates.

These are used

- to accommodate control commands which the microprocessor uses to influence the behaviour of the interface logic (e.g., among numerous other possibilities, it can stop the handshake cycle or send a Service Request SRQ via the IEC bus);
- as shift registers for bytes to be transmitted from the device to the IEC bus, e.g. talker bytes and status bytes. Talker bytes are the data transmitted from the device to the IEC bus while the device is operating as talker, e.g. when the measuring result is transmitted.

  The status byte is the devices response to a Serial Poll and contains the current device status.

  The "Address" switch is used for setting the device address.

  The "PP message" switch determines the IEC bus line on which the device is to transmit its Requested Service (RQS) status bit when the controller asks for its status by way of a Parallel Poll.

  In order to allow the BN 958 IEC bus interface to operate as the IEC bus controller the device-internal microprocessor must have direct access to certain IEC bus lines. This access is possible via the controller input gate and the controller output gate.

Interplay of device and IEC bus interface

When the IEC bus reaches a status requiring control by the device-internal microprocessor, the IEC bus interface sends an interrupt to the device. This interrupt then causes the microprocessor to execute the IEC bus program (see Fig. 9.2.42-2). This is the case if, for example,

- the device is to be switched from local to remote control or vice versa,
- a listener byte has been transmitted via the IEC bus. The interface logic has then written this byte into the transfer register for listener bytes and stopped the handshake cycle. The handshake cycle remains interrupted until the microprocessor reads this byte (whereupon the IEC bus line NDAC goes HIGH). Once the listener byte has been processed and stored, the IEC bus line NRFD also goes HIGH.
- the device must provide a new talker byte. When the new talker byte is written into the corresponding output gate, the handshake cycle is started by the IEC bus line DAV being switched to LOW.
- the device is to be triggered by the IEC bus command "Device Trigger (GET)" in order to perform a measurement. The interface logic has then stopped the handshake cycle. It remains interrupted until the microprocessor has started the measurement and then re-enables the handshake cycle (NDAC = HIGH and NRFD = HIGH).

- the device is to be set to a defined initial status by the IEC bus command "Device Clear (DCL or SDC)". Again, the interface logic will have stopped the handshake cycle. It remains interrupted until the microprocessor has set the device to the initial status and then re-enables the handshake cycle (NDAC = HIGH and NRFD = HIGH).

If the CLR jumper is fitted on the IEC bus or if switch S 3 is closed, the IEC bus signal IFC (Interface Clear) causes initialization of the device. In the event of an interlock condition, the device can always be initialized via the IEC bus. (This is important for devices in unmanned stations where an interlock condition caused by external disturbances cannot be eliminated by switching the mains power off and back on.)

9.2.42.3 Structure of the IEC bus program (The program is implemented on the CPU board)

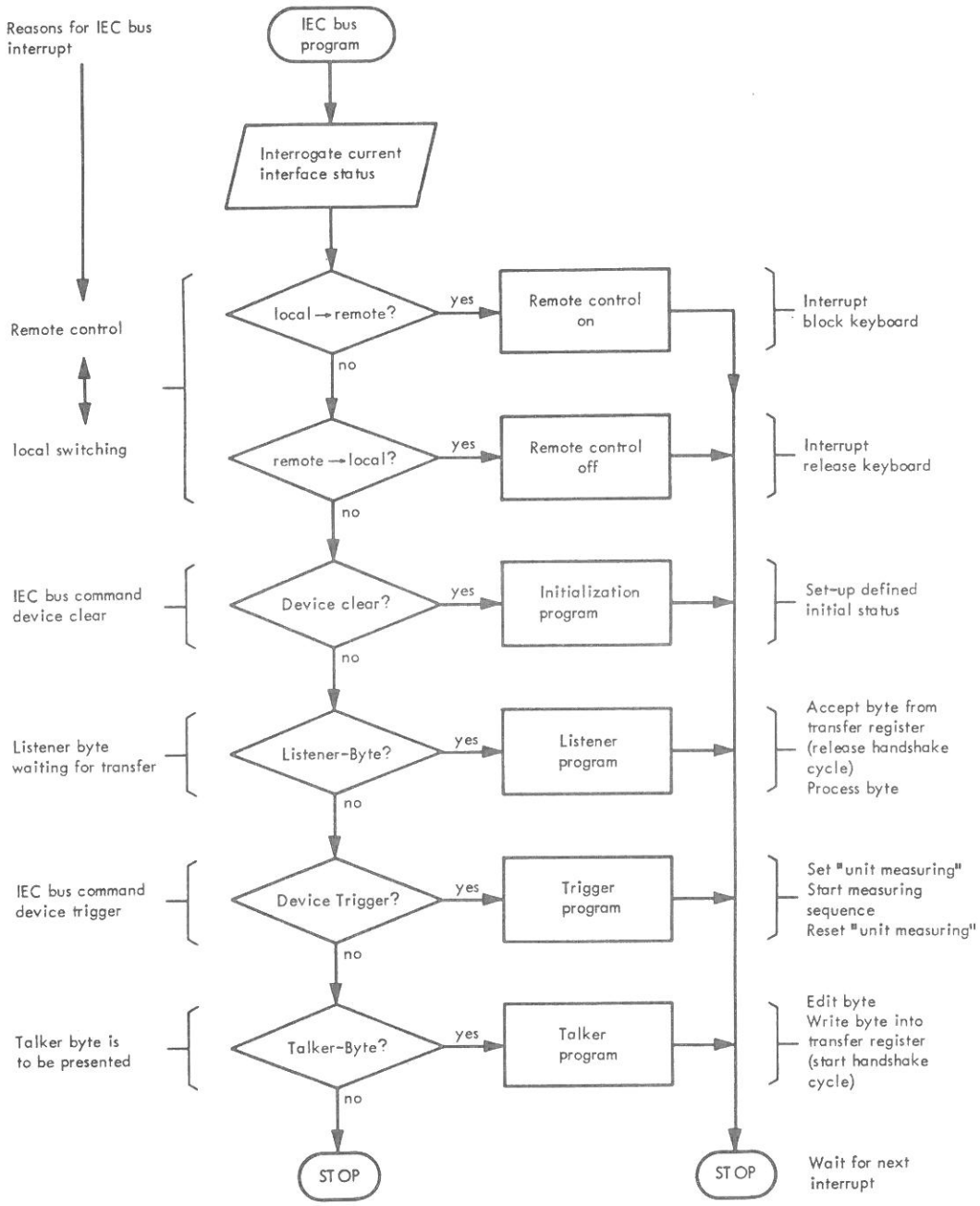


Figure 9.2.42-2 Structure of the IEC bus program

9.2.43 SCREEN CONTROL BOARD BSK-1, BN 962, CIRCUIT DIAGRAM (92)

9.2.43.1 Introductory remarks

Before reading the circuitry description below, make sure you are familiar with the following subjects:

- The standard monochrome TV signals
- Characteristics of the EF 9365/9366 GDP
- Basic functional principles of dynamic RAMs

A knowledge of the following is also assumed:

- TTL circuits
- Simple transistor technology
- Microprocessor technology

9.2.43.2 Functional principle

In order to produce a still picture on a TV monitor, all the image data must be stored in a refresh memory. The data is read out of the refresh memory as the beam travels across the screen. Depending on the memory contents, the beam is either unblanked or blanked. In the simplest case, one bit in the refresh memory is assigned to each pixel on the screen. This principle is illustrated in Fig. 9.2.43-1: the microprocessor system causes the character and vector generator to build up the image data in the refresh memory. The controller guides the monitor beam via the blanking and sync. signal, addressing the memory bit associated with the beam position in each case (picture signal). The three signal components are than combined to form the standard composite video signal and passed to the monitor.

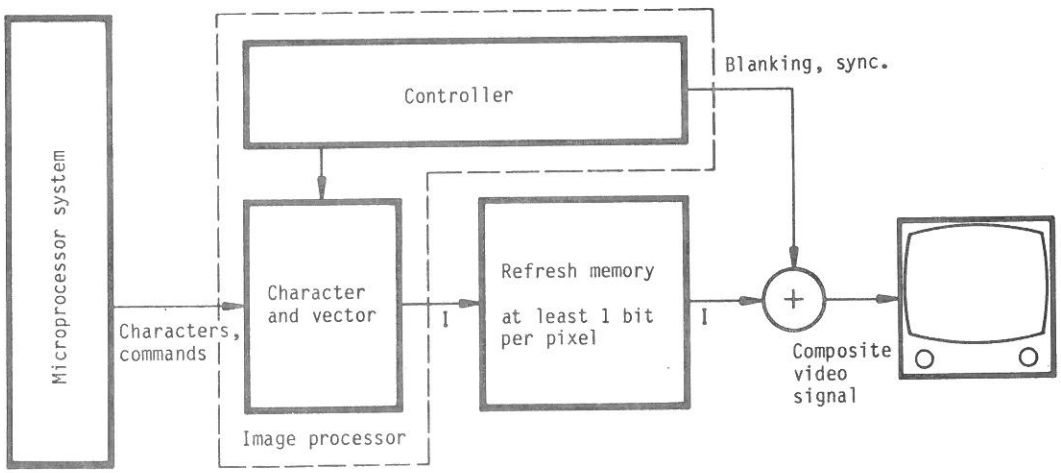


Figure 9.2.43-1 Pixel-oriented screen

a) Block circuit diagram, BSK-1

The circuitry for conditioning the composite video signal and the refresh memory with three memory banks are shown on the right of the diagram. The picture stored in Bank 1 is displayed with reduced brightness, while those in Bank 2 and Bank 3 are displayed at full brightness (Bank 1 is for rasters, etc., Bank 2 for test results and Bank 3 for text). The image processor on the left-hand side builds up the image data in the individual memory banks and usually also controls the display of the stored pictures. Switch S 2 can be used to transfer display control for Bank 3 to a special addresser which allows expansion of the display. (The reason for this is explained in Section b). S 2 to S 8 can be controlled directly from the microprocessor via the output gate, meaning that the following decisions can be made via the program:

- Which memory bank is to hold the image data (S 3, S 4, S 5)
- Whether or not the contents of a memory bank are to be displayed (S 6, S 7, S 8)
- Whether the contents of memory bank 3 are to be displayed in normal or extended form (S 2).

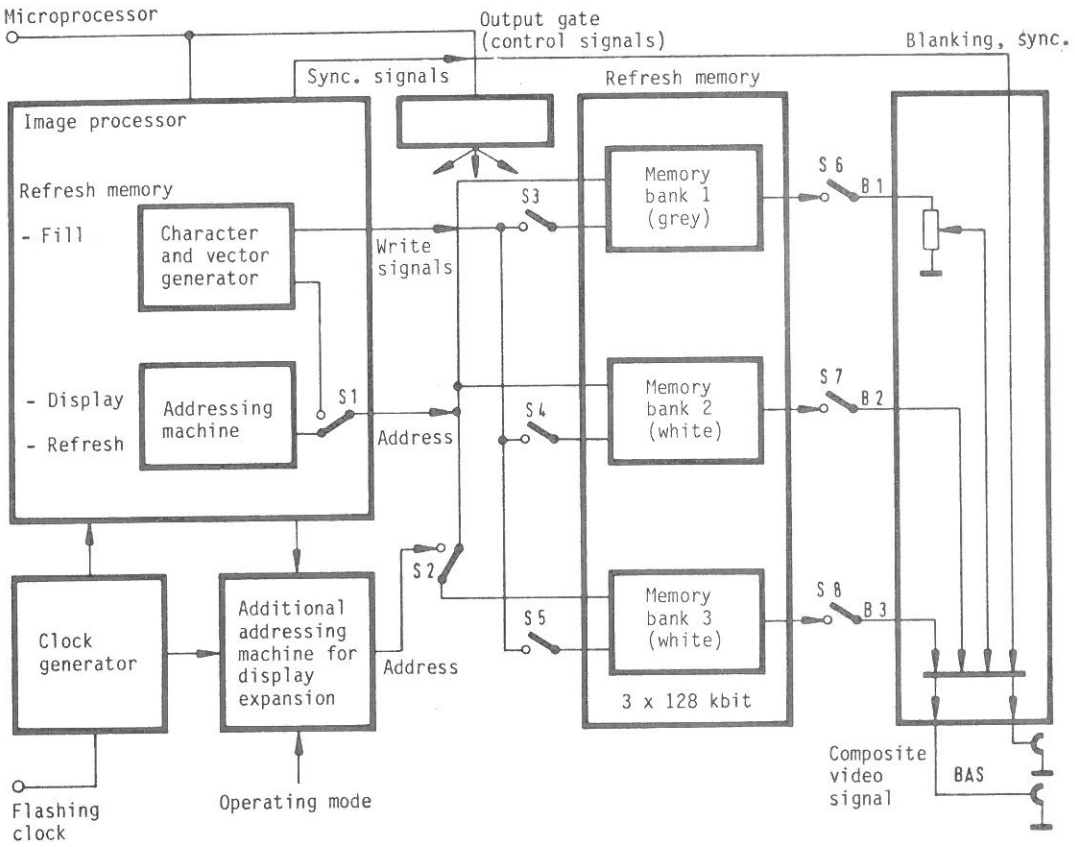


Figure 9.2.43-2 Block circuit diagram, BSK-1

b) Image formation

The image is formed without interlacing, meaning that 312 raster lines are obtained. A maximum of about 302* of these lines are displayed on the screen.

The memory banks of the refresh memory are designed for 512 x 256 pixels. Thus, unless special measures are taken, 46 raster lines cannot be written on. In order to produce a balanced picture, the image processor does not distribute the 512 pixels in X direction over the full screen width, but generates a roughly square field in the middle of the screen, meaning that there is an unusable margin at both sides.

* Note: This is the theoretical maximum value. The number of lines which can actually be displayed depends on the time required for frame repetition on the monitor used. (raster fly-back blanking.)

Division of the screen into sub-areas

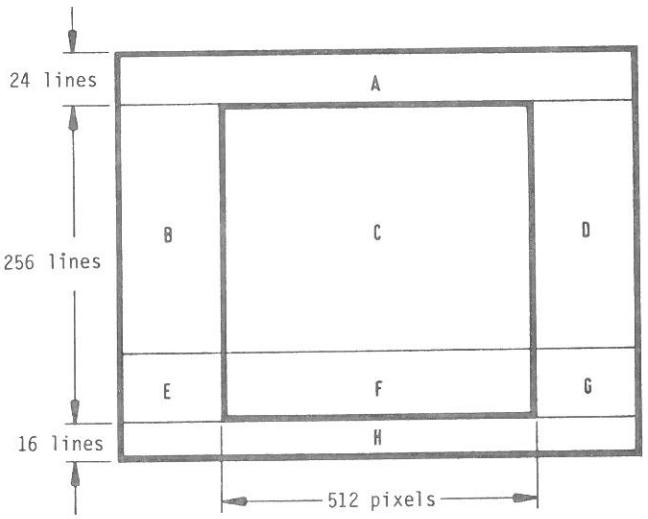


Figure 9.2.43-3 Division of the screen into sub-areas

Refresh memory assignments

Memory bank 1:
- Sub-areas C and F
- Brightness variable between grey and white via trimming potentiometer P 1 (accessible from the rear of the unit)
- Raster: 256 pixels in Y direction
  512 pixels in X direction

Memory bank 2:
- Brightness white
- Otherwise same as memory bank 1

Memory bank 3, mode 1 (non-expanded):
- Same as memory bank 2

Memory bank 3, mode 2 (expanded):
- Covers the entire screen
- Brightness white
- Each pixel in the refresh memory is output to the screen twice (expansion in X direction)
- In addition, each raster line in sub-areas B to G is also output to the screen twice (expansion in Y direction)
- Thus, the fresh memory contains more pixels than the screen can display.

Memory bank 3, mode 3 (expanded):
- All raster lines are output to the screen once only; however, since the refresh memory can only hold 256 screen lines, sub-areas E, F and G cannot be addressed by memory bank 3.
- Otherwise same as mode 2.

Switching from mode 2 to mode 3 is controlled via the $\overline{B3BA2}$ input on the external addresser

The characteristics of memory bank 3 seem to be unsystematic. However, they represent a good compromise between our requirements and the cost of implementation.

c) Circuitry details

Microprocessor interface

The data bus and address lines of the image processor IC 60 are connected directly to the slow bus of the microprocessor system. The remaining address lines of the bus system are connected to A4 and E1, E2 or $\overline{E3}$. Thus, if A4 = $\overline{E3}$ = Ø and E1 = E2 = 1, the data strobe $\overline{LSS}$ is connected through to the control input E on IC 60 (IC 58). The data direction is reversed with R/W at IC 60.

R 4 is used to adapt IC 60 to the CMOS bus and to protect the inputs of IC 61.

If A4(E3) = 1, the data strobe $\overline{LSS}$ acts on the output gate (control gate) IC 61. Address decoding is incomplete: AØ ... A3 remain un-decoded and no distinction is made between write and read operations. Thus, an accidental read operation with the address of this output gate can destroy its contents.

$\overline{INT1}$ is an open-collector output.

The counter module IC 59 is incremented by the VB output of IC 60 at 50 Hz. It can be reset by the software via IC 61. In normal operation, it is used to generate the flashing interrupt (usually, only one of the three outputs on the motherboard is wired), and in test mode for synchronizing the image processor and the microprocessor (refer to "Function of memory bank 3, mode 2 and 3 (expanded)" for a description).

Central clock supply

All operations on the BSK-1 which are not controlled directly by the microprocessor are timed by the central clock supply. Eight additional phase-locked clocks are derived from a 14 MHz clock for this purpose.

Principle:

OS1 generates a 14 MHz clock, which is distributed through the circuitry via IC 66 and IC 56/2. This clock is also used for counter IC 2. When it overflows, it is set to Ø or 8, depending on the Sync' signal. The signal profiles of the eight derived clocks required are stored in the PROM IC 3. In order to provide the clocks in spike-free form, they are stored in register IC 4.

Details:

The edge which stores the clock status in IC 4 also increments counter IC 2 at the same time. This is why counter reading and address in the PROM are shown separately in Fig. 9.2.43-4. For example when counter IC 2 has a reading of 1, the status present at the output of IC 4 is actually as assigned to the preceding counter reading, which are stored at address Ø in the PROM.

The signal shape in bits 1 to 5 is stored twice, for counter reading Ø to 7 and for readings 8 to F. Only one half need be considered.

- CK: Clock for IC 60 (image processor EF 9366). The positive edge also stores the status signals in IC 63.
- RAS, CAS: Control signals for the dynamic RAMs (refresh memory). Both signals are inverted before being passed to the RAMs. Thus, they are stored in positive logic in the PROM (but shown in negative logic in Fig. 9.2.43-4).

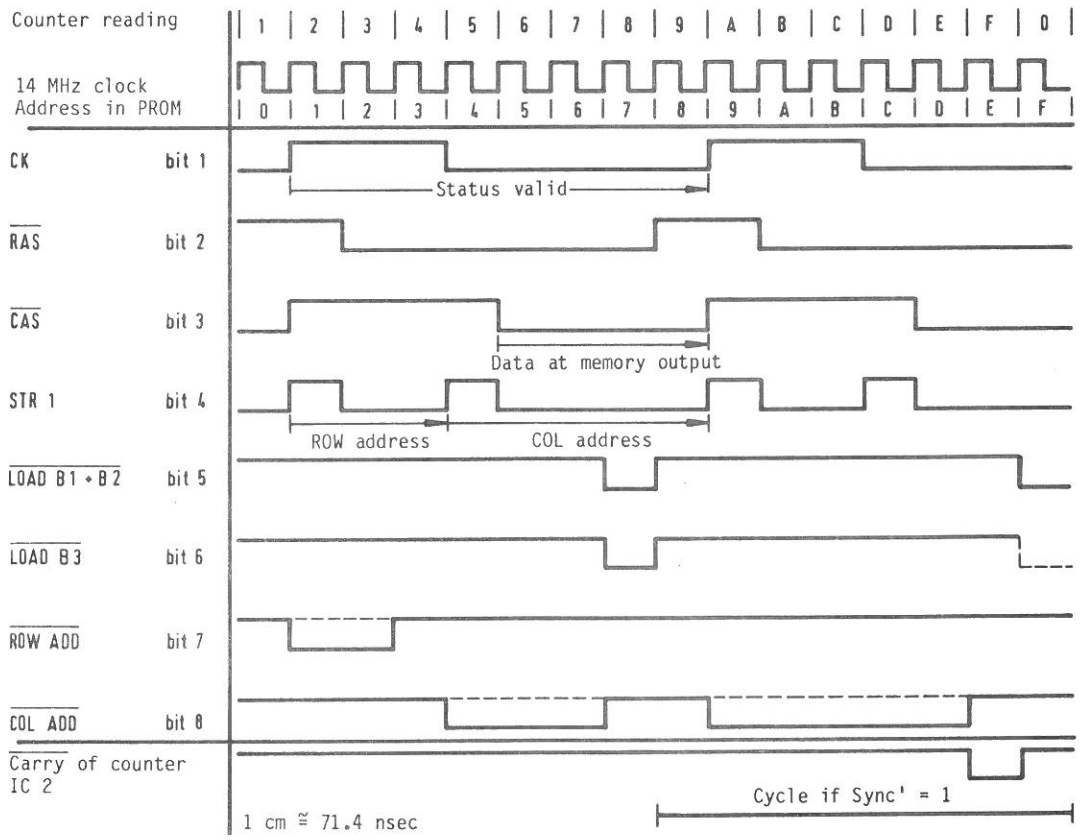


Figure 9.2.43-4 Central clock supply

- STR1: Control strobe for address register IC 62. The positive edge of the first pulse buffers the ROW addresses of IC 60, so that they are still valid after the leading edge of the $\overline{RAS}$ signal. The same applies for the second pulse and the $\overline{CAS}$ signal.
- $\overline{LOAD\ B1 + B2}$: Signifies that the data at the output of the refresh memory RAMs are valid.
- $\overline{LOAD\ B3}$, $\overline{ROW\ ADD}$, $\overline{COL\ ADD}$: Control signals for memory bank 3. The signal profiles shown as solid lines apply for expanded-display modes, those shown as dotted lines being valid for the non-expanded modes. Switching is accomplished via the ADE input on IC 3 or the signal EXPAND (DEHNEN). Thus, the PROM IC 3 in fact contains all the signal profiles shown in Fig. 9.2.43-4 in two forms: solid-line and dotted-line. The addresses ADA (≅ A0) to ADD (≅ A3) are used in the same way in both cases, meaning that ADE can virtually be switched over on the flyback.

Function of memory bank 1 (IC 9 to IC 18)

- Write operation:

The positive edge of the clock causes the status of IC 60 to be stored in IC 63:

MSLØ ... MSL2	determine the RAM IC in the memory bank into which the bit is to be written
$\overline{ALL}$	= HIGH for write operations*
$\overline{DW}$	= LOW for write operations
DIN	= Data to be written (1 bit)

When $\overline{ALL'}$ = HIGH, the Poc input of IC 9 is high. The RAS signal (inverted) only reaches the RAM determined by MSLØ ... 2 via IC 9 as a result.
The microprocessor determines which memory bank is opened for writing via control gate IC 61. When writing to memory bank 1, the $\overline{DW'}$ signal is only connected through via IC 64 to the RAMs of memory bank 1.

The data bit to be written on DIN is applied to all RAMs present.

Before the selected $\overline{RAM}$ module receives its RAS, the associated address is applied to its address inputs by IC 60 via IC 62 and IC 1. The same happens for $\overline{CAS}$, except that all RAM modules are activated.

- Read operation and display:

The pixels are approx. 71 ns apart. Since the access time of the RAMs is far longer, all eight RAM modules of a memory bank are addressed simultaneously, the data at the output loaded into a fast shift register (IC 18) and then passed to the monitor at full speed.

Status lines:

$\overline{ALL'}$	= LOW
$\overline{DW'}$	= HIGH

$\overline{E1}$ of IC 9 is HIGH. Thus, RAS is connected through to all RAMs simultaneously via IC 8/2 and POL on IC 9. In other words, there are eight valid data bits at the inputs of shift register IC 18 at the end of the read operation. The LOAD signal (cf. Fig. 9.X.X-4) then appears at the output of IC 7/1, provided that the microprocessor has enabled the display via $\overline{VIDEO\ B1}$ and that the beam is somewhere in the central square (sub-areas C and F) on the screen (BLK or BLK' = LOW). The next edge of the fast clock HCK transfers the image data into shift register IC 18.

---

* $\overline{ALL'}$ may be LOW when erasing the entire memory bank.

The output of IC 7/1 then goes LOW and the image data are passed bit-by-bit to the conditioning circuitry for the composite video signal (IC 28, T 1 to T 5).

Refresh:

The memories are organized in such a way that the refresh is carried out by the read operations during the display. The additional refresh cycles performed by the image processor IC 61 are performed in the same way as read operations. However, they remain invisible as BLK stays HIGH.

Function of memory bank 2 (IC 9, IC 19 to 27)

Identical to memory bank 1.

Function of memory bank 3 (non-expanded) (IC 39 to 48, IC 30)

The microprocessor sets $\overline{\text{EXPAND}}$ to HIGH, thus disabling the expanded display. As a result, QØ on IC 31 goes HIGH, while $\overline{\text{Q3}}$ goes LOW. This means that $\overline{\text{Q}}$ of IC 33/2 is always HIGH and S 1 of IC 48 always HIGH. IC 30 is connected through constantly. Apart from the fact that IC 37/1-2 are connected in the BLK' line, the functions are identical with memory bank 1. (The central clock supply shown in Fig. 9.2.43-4 generates the dotted-line signals, i.e. $\overline{\text{LOAD B3}} = \overline{\text{LOAD B1}} + \overline{\text{B2}}$, $\overline{\text{COL ADD}} = \overline{\text{ROW ADD}} = \text{HIGH}$.)

Function of memory bank 3, modes 2 and 3 (expanded)

Principle:

The microprocessor clears the connection between memory bank 3 and the image processor IC 60 via the $\overline{\text{EXPAND}}$ control line. Naturally, the clock continues to be provided by the central clock supply. However, the addressing of memory bank 3 is transferred to an additional addresser (IC 32 to 35, IC 49, 50). Addressing in X direction is performed at half the clock rate and starts at the beginning of every raster line (expansion in X direction). Addressing in Y direction is advanced every raster line or every second line (conditional expansion in Y direction). This mode can only be used to display the contents of memory bank 3. The non-expanded mode is selected again for write operations.

Details:

Since the $\overline{\text{EXPAND}}$ signal interferes with fundamental functions, such as central clock generation, it cannot be activated at any desired time and is thus synchronized in IC 31. Although IC 31 is essentially designed to function as a shift register, it is only used for synchronizing the $\overline{\text{EXPAND}}$ signal: when $\overline{\text{LOAD B3}}$ is LOW, the positive edge of HCK transfers the status of $\overline{\text{EXPAND}}$ to QØ and Q3. If a mode with expanded display has been set in this way,

- the address bus of memory bank 3 is no longer activated by the image processor via IC 30,
- the signals shown as solid lines in Fig. 9.2.43-4 are generated by the clock generator. This means that $\overline{\text{LOAD B3}}$ is only generated for every 16th pixel, the ROW address of memory bank 3 is switched to the address bus via IC 49 ($\overline{\text{ROW ADD}}$ signal) and, similarly, the COL address by IC 34 ($\overline{\text{COL ADD}}$ signal).

The second pulse of the $\overline{\text{COL ADD}}$ signal is merely designed to guarantee unambiguous states on the address bus during the leading edge of RAS and CAS, since RAM malfunctions could otherwise occur and problems might arise with signature analysis. In this way,

- the loading operation of IC 48 is no longer influenced by BLK' (IC 37/1),
- IC 33/2 is "cocked",
- the clock Ø/2 is connected through to S 1 on IC 48.

This means that every second clock is a HOLD clock, i.e. shifting only takes place with every second clock edge. One shift register "load" will then suffice for 16 pixels.

The additional addressing machine:

The addressing machine essentially consists of 2 counters, the Y counter (IC 35, "line counter") and the X counter (IC 50, "pixel counter"). They are controlled by the image processor and the central clock supply in such a way that their outputs can be used directly as the address for memory bank 3.

The X counter is incremented by one each storage cycle ($\overline{\text{LOAD B1 + B2}}$). However, since a new address is only required for every second storage cycle, the output 1Q A (IC 50.3) in not used (expansion in X direction). At the end of a raster line, the SYNC signal sets IC 32/2, thus resetting IC 50.

The Y counter is incremented at the end of each raster line (no expansion in Y direction), or at the end of every second raster line (expansion). Since the address bus is designed with negative logic, this represents a decrease in the Y counter reading in logic terms. The most significant bit of the X counter is used as the counting pulse. Thus, the Y counter receives a valid edge when the X counter is reset at the end of the raster line. If the VB signal is HIGH, all counter pulses pass via IC 36 to the Y counter IC 35 (no expansion in Y direction). This is the case when the beam is in sub-areas A and H. If $\overline{\text{B3BA2}}$ is LOW, IC 33/1 becomes active as a pre-divider in the other sub-areas (VB = LOW), and IC 35 is only incremented at the end of every second line (mode 2, expansion in Y direction in sub-areas B to G). VB goes HIGH at the end of sub-area G, setting IC 32/1 and thus resetting the Y counter. IC 32/1 is reset via $\overline{\text{SYNC}}$ about 0.5 µs later. Only then is IC 50 reset, and to prevent this producing an undesired counter pulse on the Y counter, it is reset "in advance" via the PRESET input of IC 32/2 at the same time as the Y counter.

IF $\overline{\text{B3BA2}}$ = LOW (mode 3), the Y counter overflows before being reset via VB. This would normally mean that part of the picture would appear on the screen twice. This is why the flip-flop IC 33/2 is set when IC 35 overflows, thus suppressing the display until the VB signal arrives (sub-areas E, F, G).

When the frame is repeated, the vertical synchronization with pre-trigger pulses and after-pulses means that the X counter does not count far enough to set 2 QC. Consequently, resetting does not produce any negative edges at 2 QC, and the Y counter reading is not changed.

In expanded mode, the dynamic RAMs are adequately refreshed by the read operations. There is no need for additional refresh cycles.

Video output stage (IC 28, T 1 ... T 5)

The digital picture signals and the digital sync. signal are combined in the video output stage to form the composite video signal. There is no special blanking signal here. In other words, no distinction is made between blanking level and black level. Apart from this, the digital image data signal is "black" during beam fly-back.

Transistors T 4 and T 5 form a push-pull output stage. Together with R 14 and R 15, the two outputs BAS1 and BAS2 have an R_i of about 75 Ω. The earth of the composite video signal is wired separately and runs as a screen to the connector pins directly adjacent to the composite video signals.

When T 1, T 2 and T 3 are not conductive, the sync. level appears at the output (R 9, R 12). If SYNC' becomes LOW, T 1 conducts and the output switches to the black level. If the image signal "white" now arrives via IC 28/3 or IC 28/4, T 3 conducts and the output level changes accordingly. The same happens if T 2 is connected through via IC 28/1. However, the effect on the composite video signal can be adjusted via P 1 (grey setting) in this case.

If a pixel is activated as "white", for example via IC 28/4, virtually no increase in brightness can be expected if "white" is activated via IC 28/3 at the same time. Thus, T 3 reaches almost its minimum flux voltage with only one "white" signal. The situation is similar if "grey" and "white" are activated simultaneously (T 2 and T 3 conductive).

Gl 1, 2 and 3 are intended to prevent transistor saturation (acceleration).

The unblanked signals are clocked at 14 MHz via IC 56/2 and IC 28/1/3/4. The result is that vertical and horizontal lines on the screen have roughly the same brightness. In addition, this also ensures that a picture signal during the sync. pulse, which can theoretically arrive via IC 28/3, cannot falsify the sync. level of the composite video signal (IC 56/2).

Test mode (IC 66, IC 59)

Various tests require exact microprocessor control of all sequences in terms of both logic and timing. Using TP 1/3 (TEST), the fast clock can be switched over to the read clock RD of the microprocessor via IC 66. This switching operation also activates the STOP signal in IC 66. Obviously, no display on the screen is possible in this mode, nor can the contents of the dynamic RAMs be regarded as reproducible. However, this mode is eminently suitable for troubleshooting, using signature analysis for the greater part of the circuitry.

After switching to test mode, all operations on the BSK-1 are slowed down by a factor of about 12. The first FF of IC 59 toggles when the output VB of the image processor IC 60 goes LOW. The STOP signal then becomes active at IC 2 via IC 66, blocking all other operations until IC 59 is reset again by the microprocessor, whereupon the process is repeated. The stimulus programs in the microprocessor and the operations on the BSK-1 are synchronized in this way.

IC 66 is wired as a simple inverter for the SYNC signal.

9.2.44 7" MONITOR, BN 980

9.2.44.1 General description

The 7" monitor, BN 980, handles composite video signals (picture signal with blanking and synchronization) with 1 V_{pp} at 75 Ω with 64 µs line duration and 50 or 60 Hz refresh rate. Pictures with 296 lines (frame) or 592 lines using interlaced scanning can be displayed. The board is also fundamentally suitable for 24, 28 or 31 cm CRTs.

The board consists of five functional groups:

1. Video amplifier
2. Horizontal-deflection circuit
3. Auxiliary voltage generator
4. Vertical-deflection circuit
5. CRT with mask and (possibly) softkeys

(refer to the circuit diagram in the Appendix)

1) Video amplifier

The video amplifier has two equivalent inputs. Its transient response can be adjusted by means of C 48 or C 49.

Brightness and contrast can be adjusted via a DC voltage (0 to 5 V), the board already containing a brightness potentiometer (P 7).

The video pre-amplifier supplies sync. pulses at one output (IC 3.15), while the video signal is present at a second output (IC 3.10) after being pre-amplified in accordance with its contrast and shifted in terms of absolute position in accordance with its brightness. The latter signal is amplified in the video output stage (T 3 and T 4). Gl 9 prevents saturation and protects the CRT against unacceptable cathode voltages. The load resistor for the output stage is R 43.

2) Horizontal-deflection circuit

The horizontal-deflection circuit is the same as that of a monochrome TV receiver. It uses a negative circuit.
The feed voltage is boosted to 25 V, so that the line coils can be activated directly. The linearity control (L 5), width control (L 4), line coils and tangential tracking correction capacitor (C 29) are connected directly in series with the output transistor (T 5) or fly-back capacitor (C 30). When T 5 is off, the voltage rises across C 30, the magnetic energy of the deflection coils and line transformer is transferred to C 30 and a magnetic field with the opposite polarity is built up (C 30, C 29, line coils, L 4 and L 5 form a tank circuit.) A negative voltage would normally be built up on C 30 when the maximum field strength is reached. However, this is prevented by a fly-back diode (integrated into T 5), meaning that the tank circuit only comprises C 29, line coils, L 4 and L 2 for the sweep. This results in a fast fly-back in relation to the sweep. The losses are made up from the supply voltage via the line transformer.

T 5 is activated by the integrated circuit TDA 2593 (IC 2). This IC requires a composite video signal with positive sync. pulses, supplied via the pulse-shaping network R 32, C 24, C 15, R 21. The line frequency is determined by C 21 and R 27 and should be adjusted to the nominal value (e.g. 15.625 kHz) in the absence of an input signal. In the presence of a line fly-back pulse (via R 41) and a composite video signal, the line frequency is synchronized with a PLL (PLL filter R 24, C 19, or C 17, R 23, R 24, C 19 for "fast regulating time"). The fast regulating time is set automatically when adjusting the settings. It can also be activated constantly, this being advisable if the monitor is operated in conjunction with a video recorder. If operated with the picture control board, the slow regulating time must be selected, since the line sync. pulses are not equidistant when repeating the frame.

By feeding in a current at IC 2.5, the phase position of the horizontal pulses can be changed in such a way as to shift the picture towards the right on the monitor.

A sync. pulse for frame repetition is available on IC 2.8.

3) Auxiliary voltage generator

The voltage pulse for fly-back is transformed in various ways in the line transformer, with the result that, after rectification,

65V for the video output stage,
-65 V for adjusting the background,
400 V for the 1st accelerating voltage
and
11 kV for the 2nd accelerating voltage

are available. The CRT acts as a filter capacitor for the 11 kV. The diode is potted in the line transformer.

NOTE THAT THE CRT RETAINS ITS HIGH VOLTAGE AFTER BEING SWITCHED OFF!

A booster voltage of 25 V is available via C 34 for vertical deflection.

Since the -65 V supply is based on +12 V (C 36), the CRT is blanked when the operating voltage is switched off.

4) Vertical-deflection circuit

IC 1 (TDA 2653) forms the heart of the vertical-deflection circuit. In the absence of an input signal, the oscillator oscillates at 46.6 Hz. C 2, R 7, R 8 and P 2 are the frequency-determining elements for the deflection operation. R 8 and P 2 are shorted during fly-back, this temporarily setting a higher frequency. This is necessary in order to guarantee fly-back within 1 ms (1.5 to 2 ms on TV sets). The oscillator controls a saw-tooth generator whose amplitude is influenced by P 1, R 3 and C 1 via T 1. The frequency detector in IC 1 establishes whether a refresh rate of 50 or 60 Hz is being used and compensates for the picture amplitude errors resulting from the different refresh rates via R 2. The saw-tooth voltage passes to IC 1.3 via a buffer stage. On the one hand, it is averaged by an active low-pass filter ($f_g \approx 2$ Hz), meaning that the mean DC voltage of the saw-tooth is present at the output of IC 4 and, on the other hand, the saw-tooth is passed to a bridge (comprising R 11, R 14, R 15 and R 76). The pre-amplifier is located in the bridge diagonals. This means that any ripple present is not incorporated into the linearity of the vertical deflection via C 7.

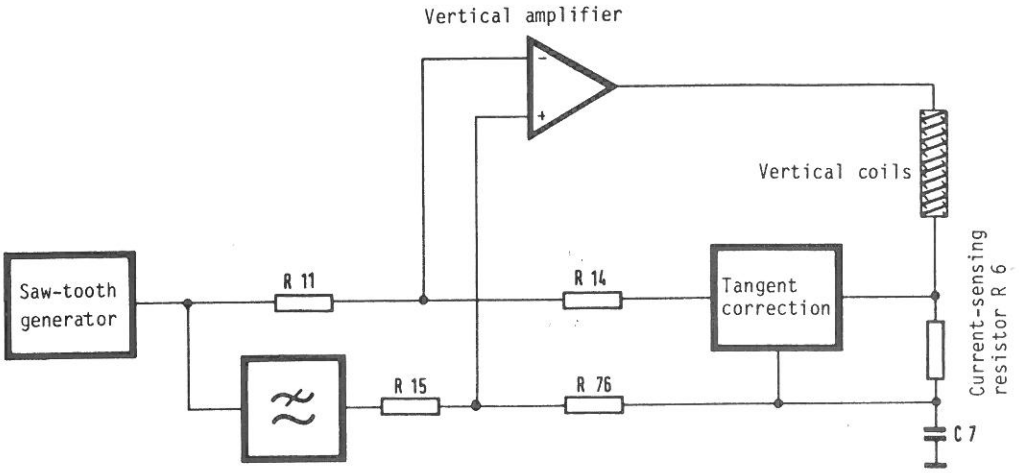


Figure 9.2.44-1 Vertical-deflection circuit

The deflecting current is tapped via R 6 and passed to the vertical amplifier IC 1.4 via the bridge arm R 14/R 11.

In order to achieve rapid vertical fly-back, the operating voltage for the output stage IC 1.5 is boosted to 50 V by the fly-back generator via C 3 for the duration of the fly-back. This pulse is also used for blanking during picture fly-back (R 50, R 56).

In order to assist troubleshooting work, the circuit diagram includes a number of pulse diagrams, which can be used for rapid identification of the faulty circuitry section.

9.2.45 DESCRIPTION OF THE PROCESSOR CARD CPU-2, BN 965, CIRCUIT DIAGRAM (90)

9.2.45.1 Reset and Mains OFF function

When the 5 V supply voltage is switched on, the processor is reset during the charging of R 7/C 4 via the CMOS gates (IC 4). In addition, the reset status is also forced for as long as the data-save input C 18 is not LOW. This data-save signal is usually generated by a so-called data-save circuit of the power supply unit. If it is LOW, i.e. if the operating voltage has reached its set-point value, the system must wait for C 3 to be charged. It then starts to run once the output of IC 4.6 ($\overline{\text{RESET IN}}$) goes HIGH.

If the processor writes into address 4, it resets the FF IC 3/1 (Q1) and thus itself forces a reset. This status is stable as long as the data-save input remains HIGH (even if the 5 V supply decreases).
FF IC 3 Q4 allows the data-save signal to be switched through to the TRAP interrupt.

Figure 9.2.45-1 shows the timing sequence of RESET IN during the power-up and power-down phases. For further details of the data-save function, also refer to Section 9.2.45.5.

In order to ensure a correct system reset in the event of only brief power-downs, capacitor C 3 is rapidly discharged via diode Gl 1 in the event of a self-reset, so that the full time constant of R 6/C 3 is always available at power-up.

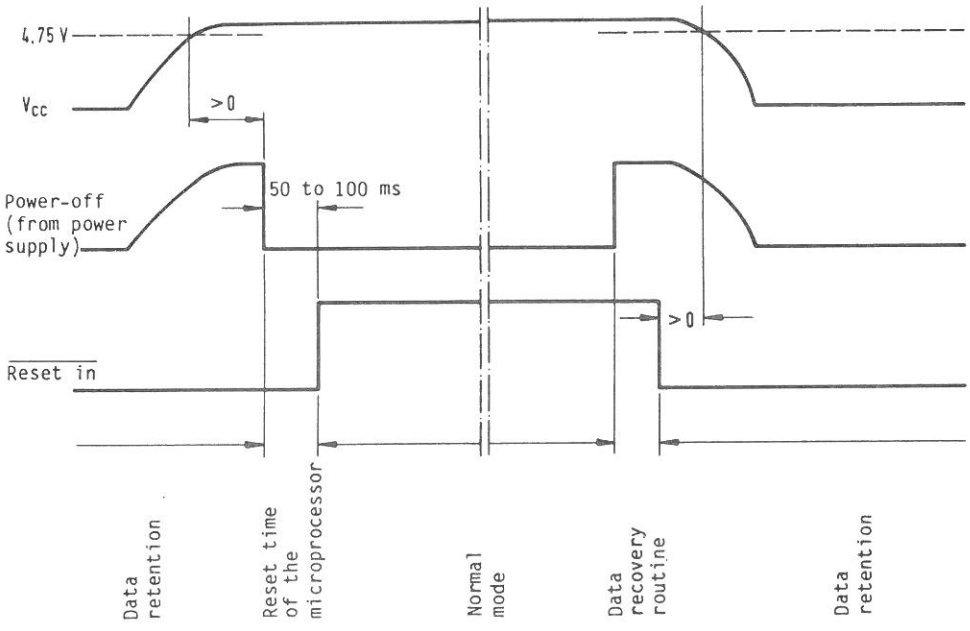


Figure 9.2.45-1 Reset function following a data-save signal

9.2.45.2 Clock generation

The 8085 processor has an one-chip clock oscillator which operates with an 8 MHz crystal between Pin IC 41.1 and .2. The 4 MHz clock signal is available at Pin IC 41.37.

9.2.45.3 Latches, drivers and memories

The latch IC 40 receives the addresses from the multiplex bus ADØ-7 of the processor, so that the full address and data bus is available in parallel form. This latch is loaded by the trailing edge of ALE. The address and data buses are wired to the multi-point connector for DMA applications or memory expansions.

In order to split up the load on the buses resulting from the memories, the ROM and RAM buses are separate and connected to the processor via drivers IC 30 ... 33 and IC 34, 37.
The separate buffering of the RAM is also partly to do with the data-save function (see 9.2.45.5).

During troubleshooting, it must be remembered that the RAM address drivers IC 30 and IC 31 are inverters.

The strobe signals $\overline{RD}$ (= $\overline{OE}$) and $\overline{WR}$ are also buffered by driver IC 32.

Memory selection takes place via the demultiplexers IC 35 and 1/2 IC 36, which also disable the memories for I/O operations or external $\overline{DISMEM}$. The associated bus drivers are also involved in the memory select/deselect operation via corresponding control lines.

The select lines of the RAMs are wired via the analog switches in IC 25 which are closed during normal operation (see 9.2.45.5).

9.2.45.4 Control lines

$\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$:

In normal operation, the processor controls data transfer via these three control lines and the address and data buses. They are provided with pull-up resistors, so that no unintentional read or write pulses can occur in the reset or hold state. $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$ can be operated externally in the hold state.

HOLD, HOLDA:

HIGH at the HOLD input causes the processor to switch to high impedance at the address and data buses, as well as at the control lines $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$. It indicates this state by a HIGH signal at the HOLDA output. The processor resumes its program when HOLD returns to LOW. The LOW address latch IC 40 is switched to high impedance by HOLDA in parallel with the processor. The card is thus DMA-compatible. HOLD is a high-impedance input which must be activated for all events.

READY:

LOW at this input delays termination of the current read/write operation of the processor until it returns to HIGH. It allows adaptation to slow memories or peripherals. The I/O bus speed reduction circuit and the arithmetic processor (AP), both of which are on the card, use the Ready signal to stop the processor until they have completed their operations. Ready thus has a pull-up resistor R 10 and is connected to IC 11 via an open-collector gate and to the bus speed reduction circuit and AP by a wired-AND (see also 9.2.45.9 and 9.2.45.6). Additional speed reduction is possible via open-collector circuits connected via the multiway plug.

SO, S1, ALE, RST 7.5, RST 6.5, RST 5.5, SID, SOD:

These control lines and inputs/outputs are all wired out on the multi-point connector and, except for ALE, are only connected to the processor IC 41. Refer to the INTEL Data Book for their functions. The interrupt input INTR is not available and is connected to earth.

$\overline{\text{CLEAR}}$:

A negative edge at this card input generates a TRAP interrupt via NAND gate IC 5/2. This $\overline{\text{CLEAR}}$ edge can only arrive if the data-save input is LOW or the inhibit flip-flop IC 3/4 (Q 3) is HIGH. The user must ensure that the TRAP is enabled by setting the inhibit flip-flop IC 3/4 (Q 4 = HIGH) or by LOW at the data-save input in the event of interrupt requests by $\overline{\text{CLEAR}}$.

Independently, the LOW edge at $\overline{\text{CLEAR}}$ sets the flip-flop IC 3/3 (Q 2), which can be read in via the I/O switch IC 44. This possibility has been provided so that the program can establish whether a TRAP was triggered by the $\overline{\text{CLEAR}}$ input or the data-save input. This so-called $\overline{\text{CLEAR}}$ flip-flop is reset by writing into address 5 via demultiplexer IC 2. The AP is reset at the same time (see 9.2.45.6).

A number of card-internal control lines are described below:

RWIO:

RWIO goes HIGH for read or write operations in the I/O area.

$\overline{\text{ERAM}}$:

$\overline{\text{ERAM}}$ (Enable RAM) selects the highest 8 K of the address area intended for the RAM/AP.

$\overline{\text{ER3}}$:

$\overline{\text{ER3}}$ (Enable RAM 3) is the chip select for RAM 3. If card input C 19 is HIGH, no arithmetic processor, the top 1/2 K addresses of RAM 3 are suppressed and made available to the AP. In this case, $\overline{\text{ER3}}$ is HIGH from FEØØH to FFFFH.

WRRD:

This line (write or read) is the NAND circuit of the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobe. It is HIGH for every read or write operation.

9.2.45.5 Data-save

In the inactive state, CMOS RAM modules allow data to be retained with little power consumption. Therefore, their supply voltages are combined separately in U_{Bat} and wired out for connection to a battery.

Figure 9.2.45-2 Connection of U_{Bat} to 5 V supply

When switched on, rectifier Gl 6 supplies the RAMs from the 5 V source and tricklecharges a rechargeable battery.

Transition from normal to data-save mode:

A few milliseconds before the operating voltage drops below the low threshold, the power supply emits the "NETZ AUS" (Mains OFF) signal as a warning. If it is connected through to the TRAP, it triggers a non-maskable interrupt. The time remaining gives the processor the chance to store important data in the non-volatile RAM. It subsequently sets a flip-flop, whose output sets the $\overline{\text{RESET IN}}$ signal to LOW (see 9.2.45.1). This causes the analog switch IC 25 to open, thus pulling the chip select inputs of the RAMs to U_{Bat} by means of pull-up resistors R 17-20:

The RAMs are protected and no leakage current can flow via the chip select inputs into the remaining circuitry. If the 5 V supply voltage then disappears completely, all inputs/outputs of the RAMs are pulled to earth by pull-up resistors, this minimizing power consumption. The RAM area is buffered separately to prevent the pull-up resistors from burdening the rest of the system bus.

The FF generating the $\overline{\text{RESET IN}}$, IC 4/1 / IC 4/2, and the analog switch IC 25 are themselves connected to U_{Bat} and thus not affected by the drop in the 5 V supply. The inputs of this FF are also held close to 0 V by resistors.

Transition from data-save to normal mode:

Only when the operating voltage has reached its set-point value does the power supply give the enable signal by setting the data-save input to LOW. After expiry of the reset time R 6/C 3, the CMOS FF IC 4/1 / IC 4/2 can switch, this causing the LOW at $\overline{\text{RESET IN}}$ to disappear. The processor starts to run and the analog switch connects the RAM chip selects through. Refer to 9.2.45.1 for the timing of this sequence.

Checking the battery status:

Capacitor C 2 is connected to U_{Bat} via R 3, following this voltage with the relatively long time constant of

R 3 x C 2 = approx. 8 sec.

Shortly after switching on, a check can be made whether the battery voltage U_{Bat} was above the limit value of 3.2 V. Comparator IC 1 compares U_{Bat} at C 2 with the reference voltage formed from 5 V by R_1/R_2.

When the I/O switch has been switched over (UPW at LOW after writing to address 6), the comparator output IC 1.7 can be read into bit Ø of the I/O data bus.

This allows the processor to check the device to establish whether the battery voltage was still sufficient for data retention just before switching on.

9.2.45.6 Demultiplexer IC 2

Five $\overline{\text{RS}}$ FFs (IC 3/1 ... 4 and IC 6/3-4) are used for controlling these card features; they can be toggled, among other things, by demultiplexer IC 2.

Demultiplexer IC 2 is activated by writing into the address area of ROM Ø; it toggles the FF selected by the address, since its enable inputs are connected to the $\overline{\text{ROM}}$ $\overline{\text{Ø}}$ select and the $\overline{\text{WR}}$ strobe. ROM Ø remains passive during write operations. It should be noted that the address inputs A, B and C are activated with the inverted RAM addresses $\overline{\text{AØ}}$, $\overline{\text{A1}}$ and $\overline{\text{A2}}$.

9.2.45.7 Free-running

The CPU board has a free-running switch (S 1/7 to S 1/10) for this purpose. If the settings of S 1/7 to S 1/10 are inverted, the processor addresses the entire memory area cyclically, incrementing the address by one each time after a RESET. In order to record ROM signatures, the associated ROM select (test point) must be used as the START/STOP signal. The use of the free-running switch, in conjunction with the pull-up resistors of the data bus and the RD2 signal via G1 2 to AD6, ensures that only a subset of the 8085 command set is executed.

Bit number :	7	6	5	4	3	2	1	Ø	
Logic level :	H	L	X	X	X	X	X	H	
Machine code:	1	Ø	X	X	X	X	X	1	= 81H..BFH

X = any, data line not disconnected.

Note: The free-running switch only affects data lines Ø, 6 and 7.

Figure 9.2.45-3 Value of the data bits for free-running

The commands involved are one-byte commands for arithmetic or logic operations which increment the program counter reading by one and thus yield a "program" with consecutive memory addressing.

9.2.45.8 I/O bus

The 8085 processor has input/output commands for serving its own I/O data and address bus. This bus is generally used to control a device. In order to prevent these ramified lines from carrying too much interference into sensitive circuits, W&G uses a special bus concept with the following features:

- Easily damped CMOS drivers/receivers.
- The address bus always has a defined value, only switching when necessary.
- The processor card holds the data bus at the old value when no data transfer is in progress.
- Special strobe signals allow simple connection of address decoders and data latches/drivers as peripherals (see 9.2.45.9).
- READY' input for deceleration of I/O operations as desired (see 9.2.45.9).
- Deceleration of I/O operations by binary input via inputs B1-B3 within fixed limits (see 9.2.45.9).

The following additional possibilities have also been provided:

- The output data can be read back for diagnostic purposes, i.e. the processor can read the output data back in while the connected peripherals are de-activated by the control lines.
- For special purposes (e.g. servicing), the I/O read gate IC 44 and IC 45 can be switched over to read switches S 1/1 to S 1/6, the CLEAR flip-flop (see 9.2.45.4) and the RAM battery monitor (see 9.2.45.5).

The I/O addresses are taken from the system bus by the CMOS latch IC 39 and constantly output externally.

Output data are taken from the system bus by the CMOS latch IC 42 (if LSS is HIGH) and switched to the I/O data bus. This happens during both an OUT and IN operation of the processor. A port range disable (PORT DIS) flip-flop with the complementary outputs PORT DIS and $\overline{\text{PORT DIS}}$ can be controlled via demultiplexer IC 2.

If the $\overline{\text{PORT DIS}}$ output is switched to LOW, the I/O data driver IC 42 is activated constantly, meaning that the data can be read by driver IC 42 during an I/O read operation for diagnostic purposes. The output enable input of IC 42 is pulled to active LOW via diode G1 4.
IC 11/4 is a gate with open-collector output.

Input data are passed to the system bus by latch IC 43 (if IO/M is HIGH and RD is LOW). This latch is loaded with the data of switch IC 44, IC 45 by the LSS (Low-Speed Strobe).

Switch IC 44, IC 45 is set by the flip-flop IC 3/1 (Q3), the flip-flop itself being set by demultiplexer IC 2.

9.2.45.9 I/O timing control

In order to prevent I/O bus conflicts in a device due to the delay of the address decoders, the card generates not only the I/O data bus and the I/O address bus, but also special strobe signals RD', WR' and $\overline{\text{LSS}}$'. $\overline{\text{LSS}}$ is combined with the other two strobe signals by a logic AND:

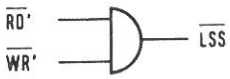


Figure 9.2.45-4 Generation of the $\overline{\text{LSS}}$ signal

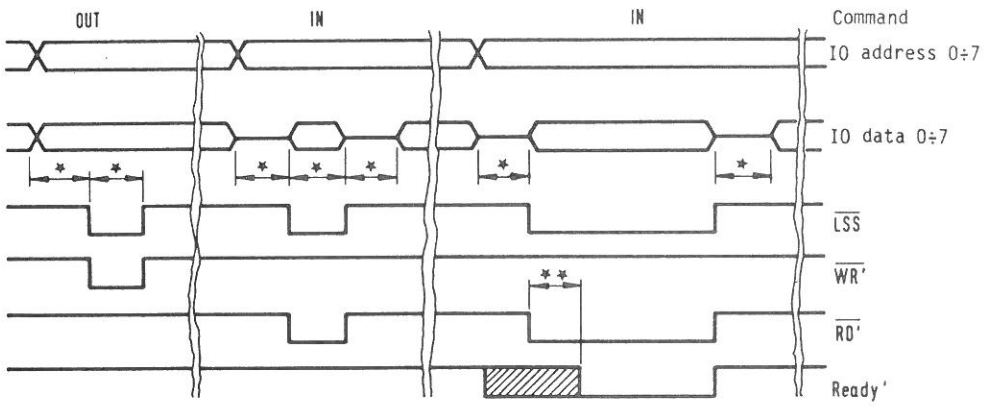
Each I/O operation consists of three time stages:

1. Addresses valid: Settling time for peripheral decoders
2. Strobe signal LOW: Data transfer ($\overline{\text{RD}}$ and $\overline{\text{WR}}$)
3. Waiting time: Resetting time for peripheral decoders

The three time stages can be varied (independently) via the three card inputs B 1-3. In positive logic, B 1-3 represents a 3-bit number:

$n = < B\ 3, B\ 2, B\ 1 >,\ 0 \leq n \leq 7$

This results in the following timing diagram for the I/O strobe signals and the I/O data- and address buses:



* $(n+1) \cdot 0.5\,\mu s + 0.25\,\mu s$ ** $\leqq n \cdot 0.5\,\mu s$

$0 \leqq n \leqq 7$

Figure 9.2.45-5 I/O timing

Stage 2 can be prolonged as desired by READY' = LOW.

Timing control sequence

The ALE signal resets the flip-flops IC 8/1, 8/2 and IC 9/2. Thus, as soon as an address for the I/O area is present on the data bus (IO/$\overline{M}$ = HIGH), the READY signal is switched to LOW via IC 10.8 and IC 11.4. Because the $\overline{Load}$ signal (IC 7.11) is LOW, counter IC 7 is already loaded with a value, e.g. ØAH (n = 5). READY also enables the clock for counter IC 7. As soon as the counter overflows, the next negative clock edge sets FF IC 8/2 (Q = H). IC 8/1 is connected downstream as a shift register cell, meaning that the counter receives a $\overline{Load}$ signal with the next-but-one clock edge.

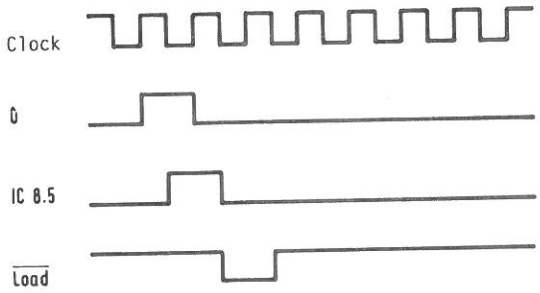
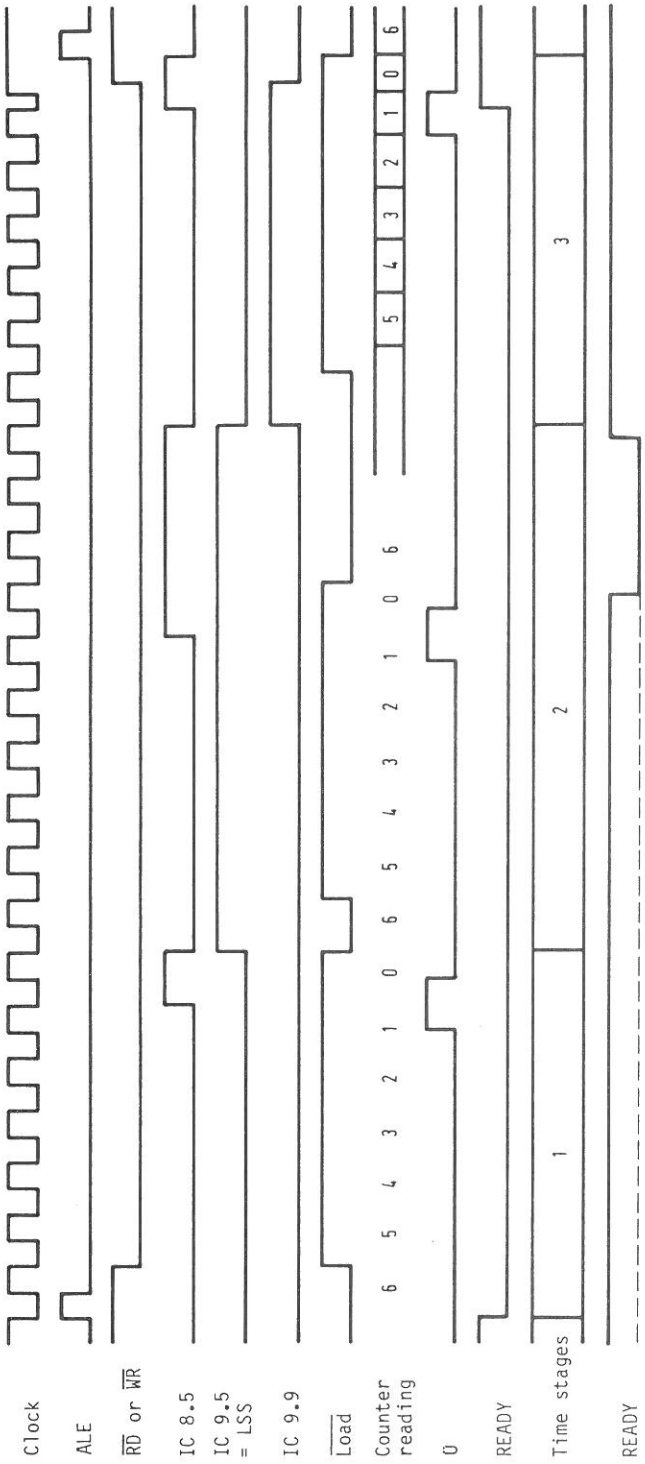


Figure 9.2.45-6 Signal sequence for counter overflow

This procedure is repeated for each time stage.

At the end of the first time stage, i.e. when the counter first overflows, flip-flop IC 9/1 (Q = IC 9.5 = LSS) is set. When the counter overflows a second time, it is reset and FF IC 9/2 is set instead.

The third and final overflow then sets the READY signal to HIGH via IC 10.8 and IC 11.4 (waiting status cancelled) and the clock is inhibited. The decelerated procedure is terminated. The control signal RWIO present at IC 9.15 resets IC 9/1 and also has a safeguarding function: LSS pulses can only be generated when the processor needs to perform READ or WRITE operations.



Time stage 2 can be prolonged as desired with READY'. Counter IC 7 is loaded with the data B1-B3 at the start of each time stage.

Figure 9.2.45-7 Timing control sequence

9.2.45.10 Test points

The card is provided with 2 x 8 test points:

Designation	Signal
$\overline{OE}$	Output enable for ROMs, same as RD strobe
$\overline{ROM0}$	ROM Ø chip select
$\overline{ROM1}$	ROM 1 chip select
$\overline{ROM2}$	ROM 2 chip select
$\overline{ROM3}$	ROM 3 chip select
$\overline{ROM4}$	ROM 4 chip select
$\overline{ROM5}$	ROM 5 chip select
$\overline{ROM6}$	ROM 6 chip select
$\overline{RAM3}$	RAM 3 chip select
$\overline{RAM2}$	RAM 2 chip select
$\overline{RAM1}$	RAM 1 chip select
$\overline{RAM0}$	RAM Ø chip select
TP 4	$\overline{LSS}$ (Low-Speed Strobe)
TP 3	$\overline{WR'}$ (Write strobe, I/O bus)
TP 2	SOD (Serial Output Data from processor)
TP 1	$\overline{RD'}$ (Read strobe, I/O bus)

Figure 9.2.45-8 Test points

9.2.46 DESCRIPTION OF THE PROCESSOR CARD CPU-2A (BN 2036)

Apart from bank-switching, the function of CPU-2A is identical with that of CPU-2 (described in Section 9.2.45).

9.2.46.1 Test points

The card is provided with 2 x 8 test points:

Designation	Signal
$\overline{OE}$	Output enable for ROMs, same as RD strobe
ROMØ	These signals are
ROM1	not used on
ROM2	CPU-2A
ROM3	
ROM4	For bank switching
ROM5	of ROMØØ ... ROMØ4
ROM6	
RAM3	RAM 3 chip select
RAM2	RAM 2 chip select
RAM1	RAM 1 chip select
RAMØ	RAM Ø chip select
TP 4	$\overline{LSS}$ (Low-Speed Strobe)
TP 3	$\overline{WR'}$ (Write strobe, I/O bus)
TP 2	SOD (Serial Output Data from processor)
TP 1	$\overline{RD'}$ (Read strobe, I/O bus)

Figure 9.2.46-1 Test points

9.2.46.2 Bank-switching

Bank-switching takes place via IC 50, IC 51 and IC 52. If output 6 of IC 50/3 is "HIGH", IC 51 is enabled and the selected EPROM is enabled.

9.3 SOFTWARE DESCRIPTION

The program are written in PASCAL and so are sufficient documented without further comments. A complete program listing however would take up too much space. Chapter 4.1 contains a description of the selftest that is run after switch on. This is adequate for serving the PCM-4.

9.4 DELAY-MEASUREMENT ASSIGNMENT

It is not always possible to give an exact delay list as many factors are involved. In the VAR.MODE it is also possible to vary the integration times (test times) and the delay before measurement. In fig. 9.4-1 the standard integration times of the PCM-4 are selected automatically. Any test time can be calculated using 9.4-3.

Analog-Signal ANA_SIGN_GEN		Integrationszeit AA	AD
Sin_10Hz		99,6	99,625
Sin_100Hz	f <4KHz	9,9	9,875
	f>=4KHz	99,6	99,625
Sin_subh		100	100
Noise_550Hz		256	256
Noise_550Hz_fast		128	128
Conv_tel			
Noise_ERL			
Noise_SRL			
Noise_SRLHI			
Group_delay		120	120
Group_del_83			
_4_Tone		199,5	199,5
OTHERWISE		512	512

Figure 9.4-1 Integration times PCM-4 (msec) basic settings

Digital-Signal PCM_SIGN_GEN	Integrationszeit DA	DD
sin_10Hz	99,6	99,625
sin_100Hz	9,9	9,875
sin_subh akt_2KHz	100	100
noise_550Hz	256	256
noise_550Hz_fast noise_3400Hz conv_tel noise_ERL Noise_SRL Noise_SRLHI	128	128
group_delay group_delay_83	120	120
_4_Tone	199,5	199,5
idle_alt_stoch	256	256
idle_alt_per	99,6	99,625
OTHERWISE	512	512

Integration time multiplication factor (var. mode 411)

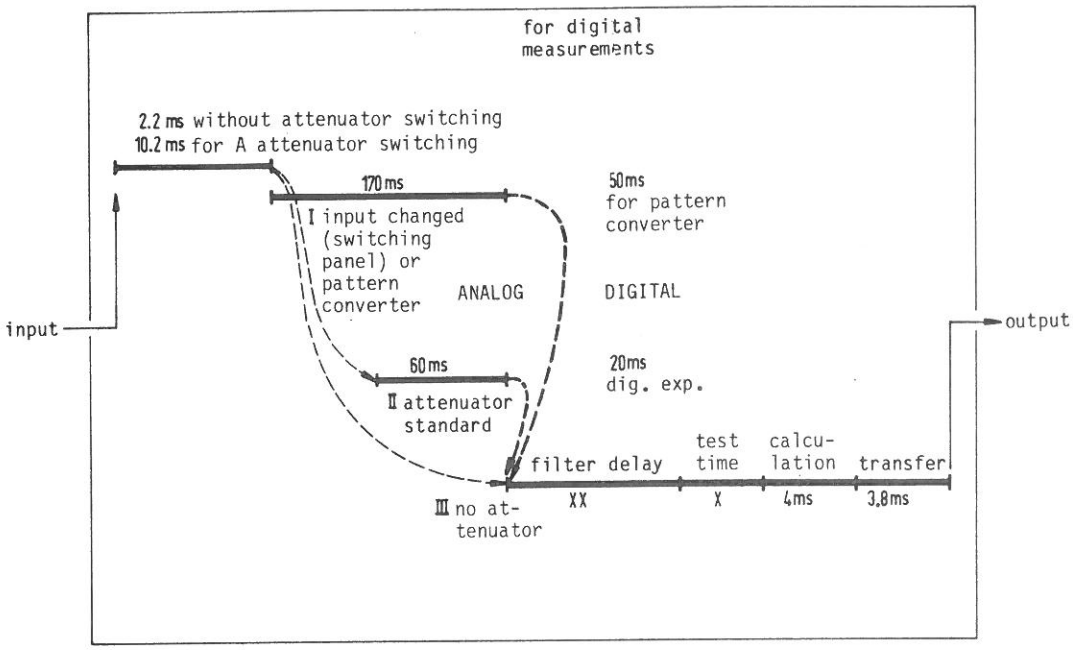
MODE		
	A13	* 4
	A51	* 2
	A52 - A57	* 5
	A91,A92	* 5
	A93,A94	* 2
	B51 - B54	* 4

Figure 9.4-1 Integration times (msec) for the PCM-4's basic settings (continued)

filter	RX filter	delay (ms)
Bypassed	Filter_aus	10
200..4k	_200_4k	20
20...4k	_20_4k	275
300..3k	_300_3k	15
20...72k	_20_72k	10
4,6k..128k	_4_128k	10
PSOPH	Psoph	10
C	C_mess	10
FLAT	_3kHz_flat	10
PSOPH + 2KHz Notch	Psoph_notch	15
C + 2KHz Notch	C_mess_notch	15
FLAT + 2KHz Notch	_300_3k_notch	15
S 350..550 Q 800..3350	_350_800	45
S 813 Q 813 Sperre+Kanalfilter	_800_wide	48
S 813 Q 813 Sperre+PSOPH	_800_psoph	48
S 1004 Q 1004 Sperre+Kanalfilter	_1000_wide	35
S 1004 Q 1004 Sperre+Kanalfilter	_1000_psoph	35
S 1004 Q 1004 Sperre+Kanalfilter	_1000_Cmess	35
Selektiv 301	Sel_300	95
Selektiv 813	Sel_813	55
Selektiv 1014	Sel_1014	55
Selektiv 3343	Sel_3343	65
350..550	_350_550	18
Phase 1000+/-300	_714_1314	10
4 TON B-A	_4Tone_BmA	90
4 TON B+A	_4Tone_BuA	90
4 TON 2B-A	_4Tone_2BA	90
KLIRR 1st.	Klirr_k2	50
KLIRR 2nd.	Klirr_k3	50

Figure 9.4-2 Filter delays (valid from series B)

MEASUREMENT



Analog measurements: 170 msec delay time when the switching panel is changed or the pattern converter is altered. (380 msec in test mode A13 or send frequency < 199 Hz)
60 msec delay is analog attenuator/amplifier are altered.

Digital measurement: 50 msec delay if pattern generator is altered
20 msec delay if the digital expansion factor is altered

Figure 9.4-3 PCM-4 test time

total measurement time

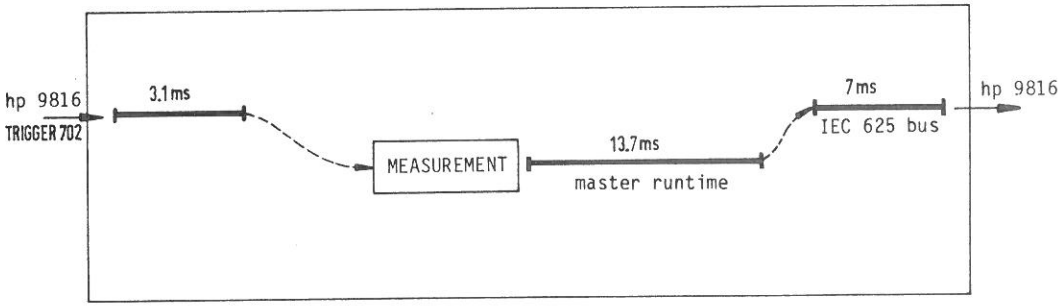


Figure 9.4-4 PCM-4 test time

10 TABLES, DIAGRAMS

This Section contains tables and drawings relating to GATE functions, etc.
The tables covering the driving of the analog generator and receiver attenuators may be particularly useful for repair work. As described in Section 2, the gates are addressed via the monitor function of the PCM-4.
(Note: Since the control gates are I/O gates, the OUT (IN) function of the monitor must be used!)

10.1 CIRCUIT BOARD ASSIGNMENTS

Version 984/02	984/01	984/03
T 1 Generator [984-AZ]	PCM-30 Generator [984-T] Series E... [984-T1] = Release 6	Same as 984/01 this version is labelled in German
T 1 Synchronization [984-BJ]	PCM-30 Rec. II [984-AS] Series E... [984-AS1] = Release 4	
T 1 Receiver [984-BD]	Rec. I [984-U] Series E... [984-U1] = Release 5	
T 1 Clock circuit [984-BF]	PCM-30 Clock circuit [984-V] Series E... [984-V1] = Release 10	
T 1 PCC [984-BE]	PCM-30 PCC [893-E]	
CRC circuit [984-AY]	CRC circuit (from E ...) [984-AY] A...D empty	
T 1 Input [984-AV]	PCM-30 Input [984-R]	
Diode board [984-Q]	Diode board [984-Q]	
T 1 Output [984-AW]	PCM-30 Output [984-S]	
Output stage 1 + 2 (1) [984-AA]	Output stage [984-AA]	
Preselector stage [984-AE]	Preselector stage [984-AE]	
Controller [984-BC]	Controller [984-BC]	
Switch panel [984-AF]	Switch panel [984-AF]	
Jack sockets	CF sockets	
Motherboard [984-A]	[984-A] (up to Release 7) (Series A ... D) without CRC; Motherboard (from Release 8) Series E... as US, with CRC	

Data retention	[959-AV]
Input	[984-E]
Aux. motherboard	[984-B]
Analog gen. 1	[984-X]
Analog gen. 2	[984-Y]
Output stage con.	[984-W]
Signal. dist.	[984-N]

	ADC-1	[984-K], [984-K1]	} alternative
	ADC-2	[984-AR], [984-AR1]	
	Analog filter	[984-J], [984-J1]	
	Digital filter	[984-F]	
	Clock filter	[984-L]	
	Evaluation circuit	[984-M]	
	PDG-64	[984-H]	
	Coupling card 1	[984-G]	
	Coupling card 2	[984-AD], [984-AD1]	
	Control	[984-C]	
	Coupling card 3	[984-AT]	
	Power supply C 15 A	Messrs. Gossen	
	Screen control card	[962-A]	
	CPU-2 card	[965-A]	
	Monitor card	[980-A/980-E]	
	CPU-2A card	[2036-A]	
Options:	958/21	IEC <625> Interface card	[958-A]
	...		
	984/00.01	Codirectional input 120 Ω	[984-Z]
	984/00.02	Codirectional output 120 Ω	[984-AJ]
	984/00.05	Serial 64 kbit/s TTL input	[984-AM]
	984/00.06	Serial 64 kbit/s TTL output	[984-AN]
	984/00.07	Parallel 64 kbit/s TTL input	[984-AO]
	984/00.08	Parallel 64 kbit/s TTL output	[984-AP]
	984/00.10	Return loss and signal balance ratio meas. bridge 600/900 Ω	[984-O]
	984/00.11	Return loss and signal balance ratio meas. bridge 600/850 Ω	[984-AG]
Accessories:	984/00.12	DC loop-holding circuit GH-1	[984-BA]
	984/00.13	DC decoupler PCMZ-4	[984-BN]

Fig. 10.1-1 Circuit boards

10.2 TABLES AND DRAWINGS ON THE CONTROL SEQUENCE

Interrupt and gate assignments of the 3 CPUs

	CPU 2A (master)	CPU 2A (disp. circ.)	CPU 2/3 (meas. circ.)
TRAP	Date retention Clear (IFC)	Reset out, Clear	Reset out, Clear
RST 7.5	IEC bus	Disp. transfer int.	Meas. transfer int.
RST 6.5	MESEND, UHR	SCC "finished"	FMAR, INIT/ALA, Overload, MRESINT
RST 5.5	TASINT, [SSOD] not used as interrupt	Flashing of SCC SCC = Screen control card	SIGN. EMP, SIGN. SEND, WKZ64K INT 1, WKZ64K INT 2
R00-R0F	00...08 IEC bus		
W00-W0F	00...06		
R10-R1F W10-W1F	} Coupling card 1	[10]... 13 ≅ CPU2 ROM [14]... 17 ≅ CPU2 ROM memory expansion	
R20-R2F W20-W2F	} Control		
R30-R3F W30-W3F	} Coupling card 2		
R40-R4F			Analog gen. RSEN
W40-W4F			Analog gen. WSEN
R50-R5F			Analog rec. REMP
W50-W5F			Analog rec. WEMP
R60-R6F		} SCC	ADU RADU
W60-W6F			ADU WADU
R70-R7F			DIG.FIL RDIF
W70-W7F			DIG.FIL WDIF
R80-R8F			Eval. circ. RAR
W80-W8F			Eval. circ. WAR
R90-R9F			PDG-64 RPDG64
W90-W9F			PDG-64 WPDG64
RA0-RAF			64 kbit I-face R64K
WA0-WAF			64 kbit I-face W64K
RB0-RBF			Signalling RKEZ
WB0-WBF			Signalling WKEZ
RC0-RDF			PCM I-face RPCMIF
WC0-WDF			PCM I-face WPCMIF
RE0-RFF			RESERVE
WE0-WFF			RESERVE

Fig. 10.2-1 Summary

Designation	Label/ Adress	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
Store MSB address and DMA on (SHOLD = H)	W 10	A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	(1)
PIEZO signal gen.	W 11	free	free	PIEZO		-	-	-	-	(2)
DMA off (SHOLD = L)	R 10	Strobe								(3)
Slave interrupt (SRST 7.5; MRST 7.5)	R 11	Strobe								(4)
Disp. circ. coupling	W 12	Strobe								(5)
Disp. circ. coupling	R 12	Strobe								(6)

Fig. 10.2-2 Coupling card 1

Designation	Label/ Adress	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
Interrupt status	$\overline{R\ 30}$	TASINT (RST5.5)	MESEND (RST6.5)	UHR (RST6.5)	SSOD=1 Slave=fin. RST5.5		MB Meas. br. fitted	MSOD Slave=fin.		(1)
							no interrupt capacity			
$\overline{CE}$ for UHR $\overline{CE}$ = L	$\overline{R\ 31}$	Strobe								(2)
$\overline{CE}$ = H	$\overline{R\ 32}$	Strobe								(3)
$\overline{RD}$ clock	$\overline{R\ 33}$	D 7							D Ø	(4)
Interrupt masks	$\overline{W\ 30}$	-	-	-	-	free	1 SSOD=free	1 MESEND	1 Clock	(5)
Reset MESEND-FF	$\overline{W\ 31}$	Strobe								(6)
Reset TASINT-FF	$\overline{W\ 32}$	Strobe								(7)
$\overline{WR}$ clock	$\overline{W\ 33}$	D 7							D Ø	(8)
ALE clock	$\overline{W\ 34}$ - $\overline{W\ 37}$	Strobe								(9)
From series E										
Status { Switch pan. / Meas. bridge	$\overline{R\ 34}$	-	-	free	free	-	ZMB Impedance meas. br.	$\overline{\text{Overload}}$ $\overline{E}$	$\overline{\text{Overload}}$ $\overline{S}$	(10)
Reset Overload S-FF	$\overline{R\ 35}$	Strobe								(11)
Reset Overload E-FF	$\overline{R\ 36}$	Strobe								(12)

Fig. 10.2-3 Coupling card 2

Designation	Label/ Adress	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
Reset INT										
INT FMAR	MW 28	Strobe								(1)
INT INT/ALA	MW 29	Strobe								(2)
INT MRES INT	MW 2A	Strobe								(3)
INT SIGN. EMP.	MW 2B	Strobe								(4)
INT SIGN. SEND	MW 2C	Strobe								(5)
INT WKZ64K INT 2	MW 2D	Strobe								(6)
Interrupt mask	MW 2E	WKZ64K INT 1	WKZ64K INT 2	SIGN. SEND.	SIGN. EMP.	MRES INT	Over-load	INT/ALA	FMAR	(7)
MESEND interrupt of meas. circ. CPU 2/3	MW 2F	Strobe								(8)
Interrupt status-poll	MR 28	WKZ64K INT 1	WKZ64K INT 2	SIGN. SEND	SIGN. EMP.	MRES INT	Over-load	INT/ALA	FMAR	(9)
Meas. sec. interface										
$\overline{WSEN}$	$\overline{W40}...\overline{W4F}$	Strobe								(10)
$\overline{WEMP}$	$\overline{W50}...\overline{W5F}$	Strobe								(11)
$\overline{WADU}$	$\overline{W60}...\overline{W6F}$	Strobe								(12)
$\overline{WDIF}$	$\overline{W70}...\overline{W7F}$	Strobe								(13)
$\overline{RSEN}$	$\overline{R40}...\overline{R4F}$	Strobe								(14)
$\overline{REMP}$	$\overline{R50}...\overline{R5F}$	Strobe								(15)
$\overline{RADU}$	$\overline{R60}...\overline{R6F}$	Strobe								(16)
$\overline{RDIF}$	$\overline{R70}...\overline{R7F}$	Strobe								(17)
$\overline{WAR}$	$\overline{W80}...\overline{W8F}$	Strobe								(18)
$\overline{WPDG\ 64}$	$\overline{W90}...\overline{W9F}$	Strobe								(19)
$\overline{W64K}$	$\overline{WA0}...\overline{WAF}$	Strobe								(20)
$\overline{WKEZ}$	$\overline{WB0}...\overline{WBF}$	Strobe								(21)
$\overline{RAR}$	$\overline{R80}...\overline{R8F}$	Strobe								(22)
$\overline{RPDG64}$	$\overline{R90}...\overline{R9F}$	Strobe								(23)
$\overline{R64K}$	$\overline{RA0}...\overline{RAF}$	Strobe								(24)
$\overline{RKEZ}$	$\overline{RB0}...\overline{RBF}$	Strobe								(25)
$\overline{WPCMIF}$	$\overline{WG0}...\overline{WDF}$	Strobe								(26)
$\overline{WRES}$	$\overline{WE0}...\overline{WFF}$	Strobe								(27)
$\overline{RPCMIF}$	$\overline{RC0}...\overline{RDF}$	Strobe								(28)
$\overline{RRES}$	$\overline{RE0}...\overline{RFF}$	Strobe								(29)

Fig. 10.2-4 Coupling card 3

Explanations to the gate assignment table

Coupling card 1

(1), (6): W 12, R 12 select the circuit coupling required. The slave interrupt (RST 7.5) is made active by R 11 at the circuit selected by W 12, R 12. The same operations take place in DMA mode (W 10 = on and R 10 = off).

Coupling card 2

(1) : The signals MB and MSOD have no interrupt capacity.
MB = Measuring bridge fitted
MSOD = Measuring circuit finished

(2), (3) : R 31, R 32 - Strobes stored by the RS FF.

(5) : Interrupts can be disabled or enabled via this gate.
SSOD is permanently inhibited by the software (i.e. the interrupt capacity of SSOD is not used; interrogation is achieved by polling).

(9) : ALE clock = Address Latch Enable of the clock, i.e. multiplex mode of data and address input.

(10), (11), (12): This modification is installed from Series E onwards.
ZMB = Impedance measuring bridge

Coupling card 3

(1) - (6): Reset interrupt hold FF.

(7) : All interrupts arriving on the coupling card can be disabled or enabled via this data gate. A HIGH signal at the Q outputs of the data latch enables the interrupts.

(8) : MESEND = End-of-measurement interrupt of the measuring circuit to the master computer.

(10)-(29): Generation of strobe signals used as decoder enable signals for the various cards.

W_SEN	Write Enable	Analog generator
W_EMP	Write Enable	Analog generator
W_ADU	Write Enable	ADC
W_DIF	Write Enable	Digital filter
W_AR	Write Enable	Evaluation circuit
W_PDG64	Write Enable	PDG-64
W_64K	Write Enable	64 kbit input/output
W_KEZ	Write Enable	Signalling distortion
W_PCMIF	Write Enable	PCM-30
W_RES	Write Enable	Reserve
R_SEN	Read Enable	Analog generator
R_EMP	Read Enable	Analog receiver
R_ADU	Read Enable	ADC
R_DIF	Read Enable	Digital filter
R_AR	Read Enable	Evaluation circuit
R_PDG64K	Read Enable	PDG-64
R_64K	Read Enable	64 kbit input/output
R_KEZ	Read Enable	Signalling distortion
R_PCMIF	Read Enable	PCM-30
R_RES	Read Enable	Reserve

Designation	Label/ Adress	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
Keyboard columns	$\overline{W20}$ or $\overline{W21}$	TS 7	TS 6	TS 5	TS 4	TS 3	TS 2	TS 1	TS Ø	(1)
LEDs	$\overline{W24}$					Ri compl.	Ri 900	Ri 850	Ri 600	(2)
LEDs	$\overline{W25}$				Re >30 KΩ	Re compl.	Re 900	Re 850	Re 600	(3)
LEDs	$\overline{W26}$				Stop = on = 1		Numer. on	Graphic on	Start on	(4)
LEDs	$\overline{W27}$				Local on	Remote on		TX/RX on	4-wire on	(5)
Keyboard rows	$\overline{R20}$	TZ 7	TZ 6	TZ 5	TZ 4	TZ 3	TZ 2	TZ 1	TZ Ø	(6)

Fig. 10.2-5 Control

Analog generator

(1): The data of offset switch S1 are adopted in this way at the start of each calibration cycle, i.e. strobe pulse R40 is output once during each calibration cycle.

(2): The addresses W40 - W47 address the gate-array circuit.

(5): Attenuation settings of the analog generator
The following diagram illustrates the switching states of divider control signals T1...T4.
The ordinate scale Ps/dB represents the output level of the generator at socket 25.
It is assumed that the FINE ATTENUATOR is set to "0dB". Consequently, the ranges displayed may deviate by up to 3 dB in relation to the absolute scale.
Example:
Output level at socket 25: 25 dB
TØ = 1
T1 = 0
T2 = 0
T3 = 1
T4 = 0

Designation	Address			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
Attenuator*	W4B	Atten. [dB]	Hex	TØ	T1	T2	T3	T4	(5)
		0	00	0	0	0	0	0	
		6	10	1	0	0	0	0	
		12	08	0	1	0	0	0	
		18	18	1	1	0	0	0	
		24	04	0	0	1	0	0	
		30	02	0	0	0	1	0	
		36	12	1	0	0	1	0	
		42	01	0	0	0	0	1	
		48	11	1	0	0	0	1	
		54	09	0	1	0	0	1	
		60	19	1	1	0	0	1	
		66	05	0	0	1	0	1	
		72	03	0	0	0	1	1	
		78	13	1	0	0	1	1	
		84	ØB	0	1	0	1	1	
		90	1B	1	1	0	1	1	
		96	07	0	0	1	1	1	
		Generator OFF	1F	1	1	1	1	1	
Ri values	W4C	- -	-	-	Compl.	900 Ω	850 Ω	600 Ω	(6)
Level attenuator Aux. output	W4D	- -	H5	H4	H3	H2	H1	HØ	(7)
Test points for signature analysis	W4E	- -	-	-	-	SA3	SA2	SA1	(8)

* In order to transfer the setting into setting latch IC 25, "0:46.00" must be executed subsequently!

Fig. 10.2-6 Analog generator

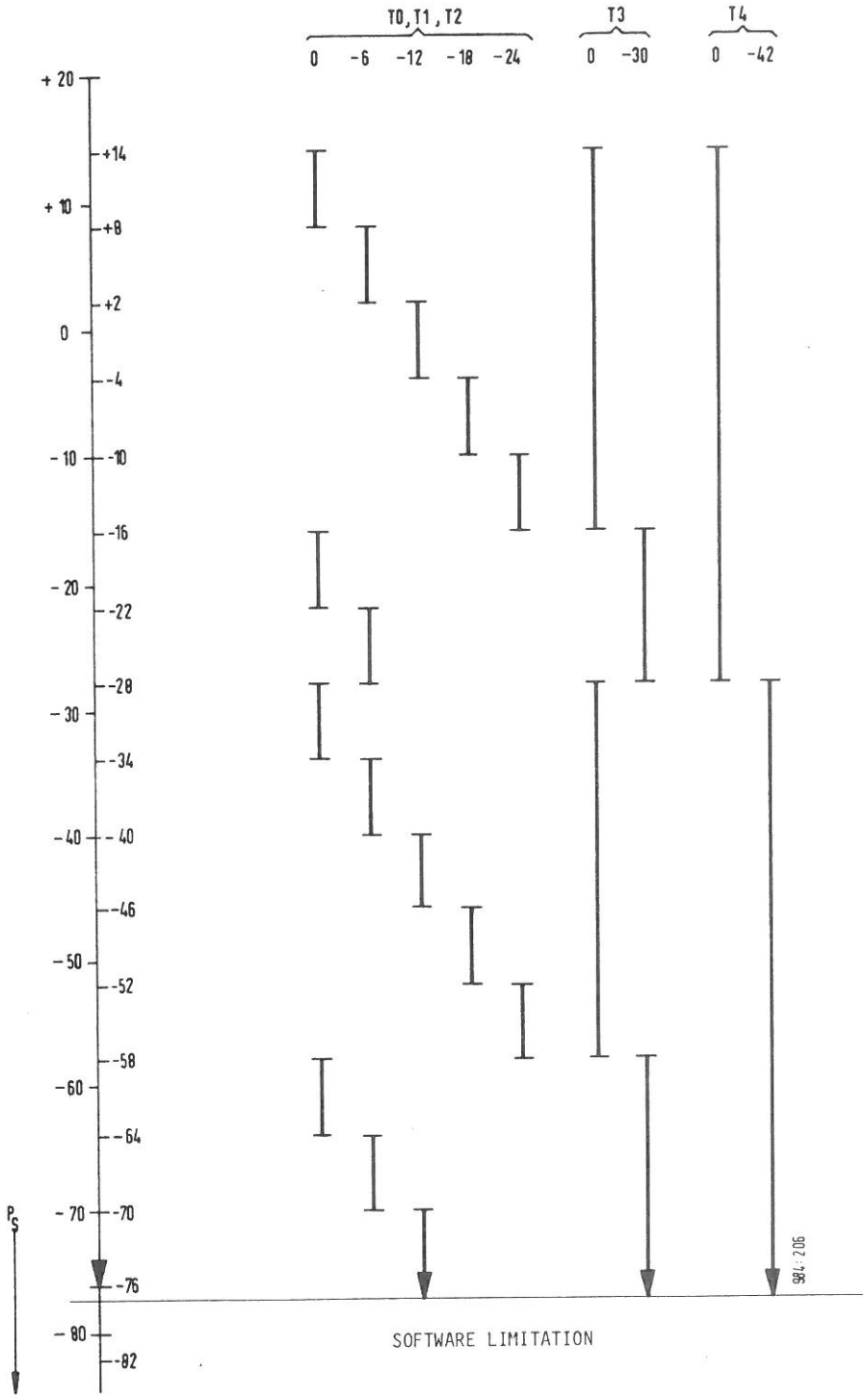


Fig. 10.2-7 PCM-4 generator section

Designation	Label/ Adress	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
Reset Gate Array	W4Ø	-	-	-	-	-	-	-	Reset	
Control	W41	-	Clock Test Single		Clock1 0 Clock2 0 Clock3 1 Clock RST 1	0 1 0 1	Control2	Control1	Sweep	
Increment LSB	W42	I7	I6	I5	I4	I3	I2	I1	IØ	
Increment MSB	W43	-	-	-	I12	I11	I10	I9	I8	(2)
Field length LSB	W44	L7	L6	L5	L4	L3	L2	L1	LØ	
Field length MSB	W45	-	-	L13	L12	L11	L10	L9	L8	
Synchronization	W46	No data required								
Range division	W47	-	-	-	A13	A12	A11	A1Ø	A9	
Reference DAC LSB	W48	R7	R6	R5	R4	R3	R2	R1	RØ	
MSB	W49					R11	R1Ø	R9	R8	(3)
Filter, control Aux. output	W4A	Switched-through signal		Hex				F1	FØ	
		Noise TP 1,7 kHz		00				0	0	
		In-band TP 4,5 Hz		01				0	1	(4)
		Out-of-band only TP 75 kHz		02				1	0	
		Analog ground		03				1	1	
Input gates Offset of reference converter RSEN	R4Ø	-	-	05	04	03	02	01	00	(1)

Fig. 10.2-8 Analog generator gates

Analog receiver

(1): Rec. attenuator: 0:50.55 switches a bypass around the reference attenuator.

The following tables of attenuator states can be used to check the switching states at IC 6, IC 8, IC 10.
A distinction must be made between three general settings:

Mode MA 8x = attenuator selection Out-of-band
Mode MA 6x = attenuator selection Sensitive
Mode MA 7x = attenuator selection Sensitive
Other modes = attenuator selection Normal

Key to abbreviations: ZT = Intermediate attenuator
ZV = Intermediate amplifier
ET = Input attenuator
EV = Input amplifier
RT = Reference attenuator
AV = Output amplifier
BYP = Bypass

Example of using the attenuator diagram:
MA 11 E
VAR. MODE 511 E
LEVEL 0dB E

Attenuator selection "NORMAL"

			D7 . . . . . DØ
ET/EV	= -18 dB	IC 10	. . . . . 0 0
ZT_1	= -6 dB	IC 8	. . . . . 0 0 1
ZV_1	= 0 dB	IC 10	. . . . 0 0 . .
AV	= +27 dB	IC 10	. . 1 . . . . .
ZV_2	= 0 dB	IC 12	. . . 0 0 . . .
ZT_2	= 0 dB	IC 6	. . . . . 0 0 0

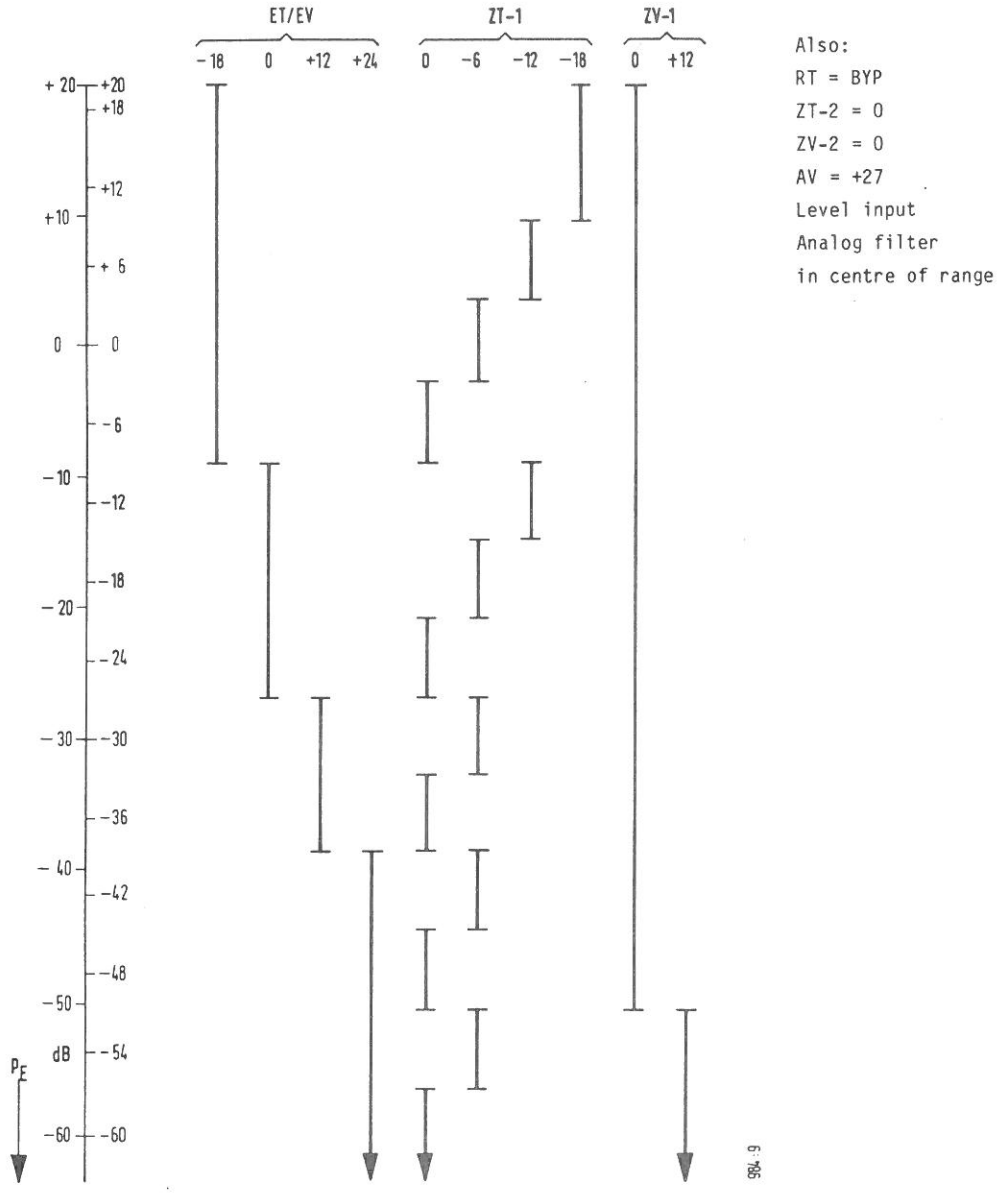


Fig. 10.2-9 PCM-4 receiver section (attenuator selection "Normal")

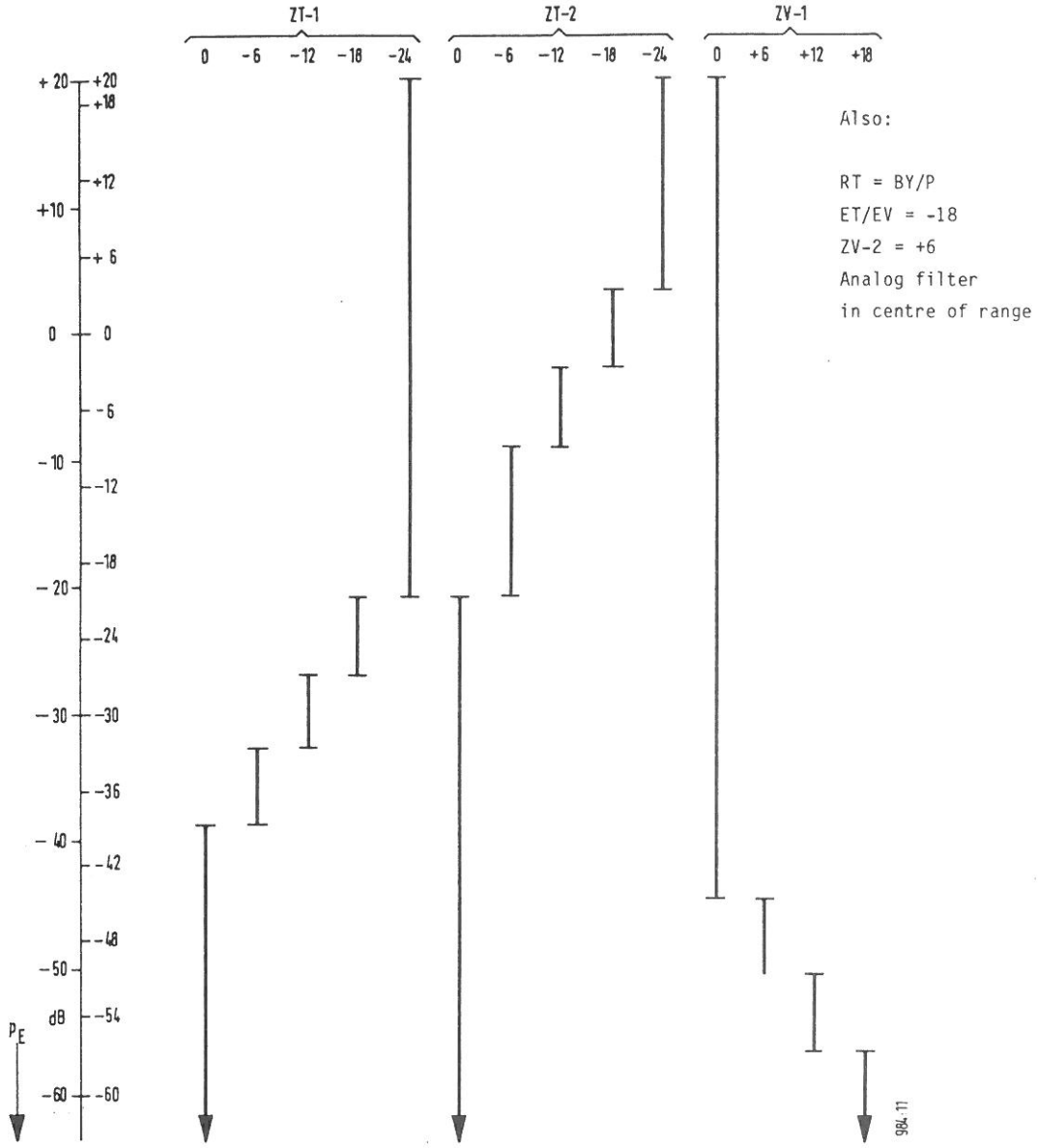


Fig. 10.2-10 Attenuator selection "Out-of-band"

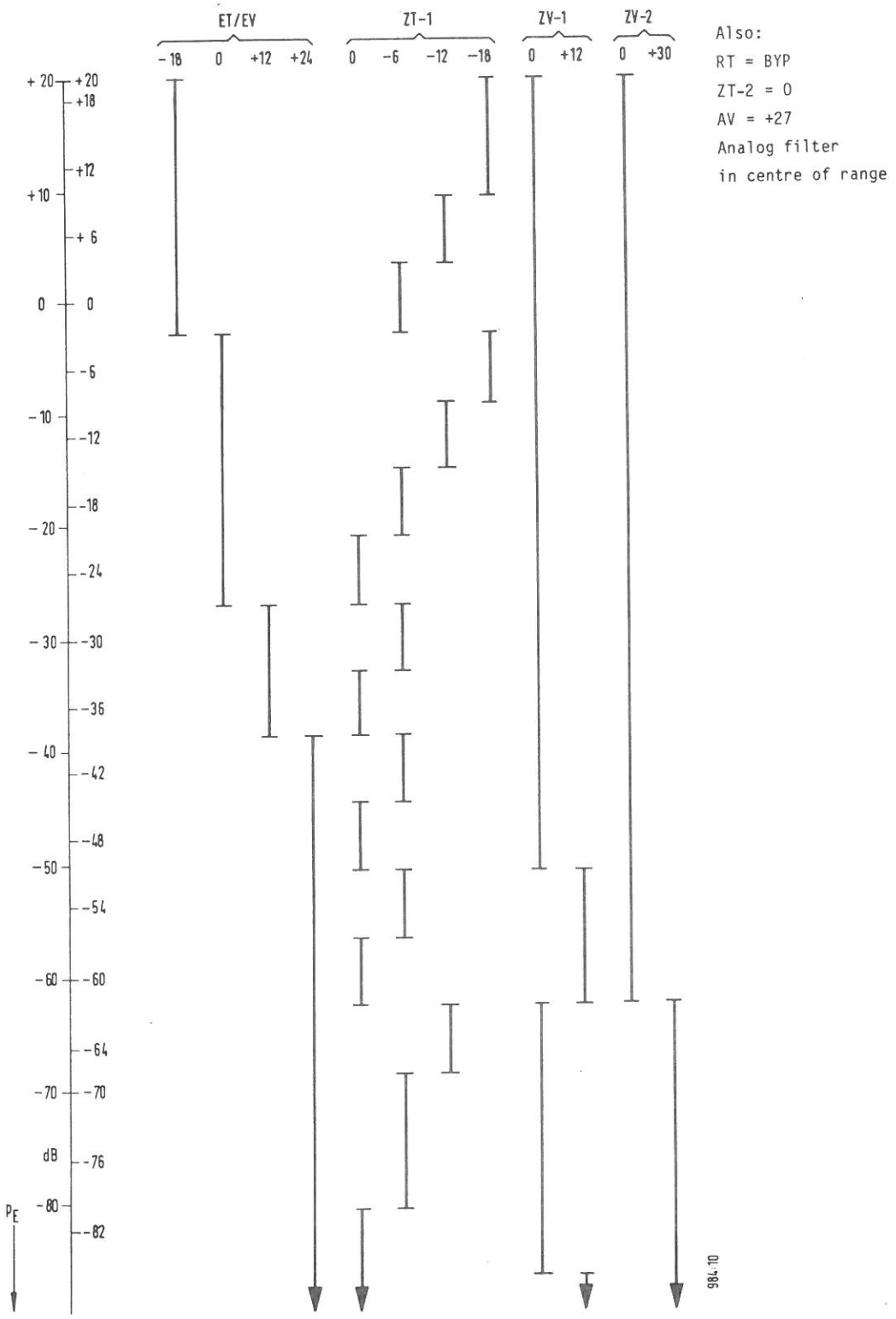


Fig. 10.2-11 Attenuator selection "Sensitive"

Designation	Label/ Adress	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Remarks
Rec. attenuator	W50		Reference atten. RT				Interm. atten. ZT-1			
			0	0	0		0	0	0	
			0	0	1		0	0	1	
			0	1	0		0	1	0	
			0	1	1		0	1	1	(1)
			1	0	0		1	0	0	
			1	0	1		1	0	1	
			1	1	0		1	1	0	
			1	1	1		1	1	1	
Rec. attenuator Rec. impedance	W51	Re-corr.	Imped. 1=cplx	Rec. 0000 = 30 K 1=900Ω	1=850Ω	1=600Ω	Interm. atten. ZT-2			
							0	0	0	
							0	0	1	
							0	1	0	
							0	1	1	(2)
							1	0	0	
							1	0	1	
							1	1	0	
							1	1	1	
Rec. amplifier	W52	free	AV	Interm. ampl.ZV2		Interm. ampl.ZV1		EV/ET		
			0≙0dB	0dB 0	0	0dB 0	0	-18dB 0	0	
			1≙+27dB	+6dB 0	1	+6dB 0	1	0dB 0	1	(3)
				+30dB 1	0	+12dB 1	0	+12dB 1	0	
						+18dB 1	1	+24dB 1	1	
Meas. bridges	W53	BI ar/AS	BI impedance ar			as	BII out	BII Z/4	BII imped.	
		0≙ar	1=kplx	1=600Ω	1=850Ω	0≙600Ω	0≙Uab	0≙OFF	0≙600Ω	(4)
	W53	1≙as				1≙850Ω	1≙Ump	1≙ON	1≙850Ω	
Meas. bridges	W54						CAL as 0	00=OFF 0		
	W54						CAL BI 1	1		(5)
	W54						Nat. bal. BI/BII 0	1		
Switch panel	W55	Rel9	Rel8	Rel7	Rel6	Rel5	Rel3	Rel2	Rel1	(6)
T1	W56	0	0	0	0	0	0	0	0	(7)
T2	W57	0	0	0	0	0	0	0	0	
Reset overloaded	W58	0	0	0	0	0	0	0	0	(8)
2-wire connection	W59				MB4 1 Rel 10 2-wire termination (complex)					(9)

Fig. 10.2-12 "Input 1" card

Designation	Label/ Adress	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Remarks
Output WADU	WRITE									
DAU LSB	W60	D7	D6	D5	D4	D3	D2	D1	DØ	(1)
DAU MSB	W61	X	X	X	X	X	X	D9	D8	
ADC latch	W62	X	X	X	X	X	X	X	X	(2)
ANA FILT	W63	X	X	Analog output	$\overline{\text{AHP4,6}}$	$\overline{\text{TP4,6}}$	$\overline{\text{EHP4,6}}$	ABAND	BBAND	(3)
	W64			0	1	0	1	0	0	
	W65			1	1	0	1	1	1	
	W66									
	W67									
Input RADU	READ									
STATUS GATE	R60	0	0	0	too big ZGR	too small ZKL	(Ø) ADC	over-driven UST	Filter FIL	(4)
CLEAR pw latch	R61	X	X	X	X	X	X	X	X	
	R62									
	R63									
STATUS GATE	R64	0	0	0	ZGR	ZKL	ADC	UST	FIL	(5)
CLEAR pw latch	R65	X	X	X	X	X	X	X	X	
	R66									
	R67									

Fig. 10.2-13 ADC-1, output 2

ADU

(4.) (5.) The adresses R60, R64 and R61, R65 address the same gates.

Designation	Label/ Adress	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Remarks
Filter digital	W70	Rounding Specification RND1	RNDØ	FILS (res.)	FIL4	FIL3	FIL2	FIL1	FILØ	
	W71	Reserve			CWFIL $\overline{\text{ON}}$/ High Z	Random sampling $\overline{\text{ON}}$/OFF	$\overline{\text{Filter}}$ 1:1-Path	f_A= $\overline{\text{8 kHz/ 10 kHz}}$	Single filter Double filter	
Clock filter	W72			Reserve		DD3	DD2	DD1	DDØ	
	W73			Reserve		$\overline{\text{octet}}$ on/ High Z	Random sampling $\overline{\text{off}}$/on on	— - A/μ-law	f_A= $\overline{\text{8 kHz/ 10 kHz}}$	
Reserve	W74									
	W75									
	W76									
	W77									
Clock	R70... 77				Reserve			Digital $\overline{\text{filter fitted}}$	Clock $\overline{\text{filter fitted}}$	

Fig. 10.2-14 Digital filter/clock filter

Designation	Label/ Adress	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
	W80		Evaluation circuit mode							
	W81		Input data byte Ø							
	W82		Input data byte 1							
	W83		Input data byte 2							
	R80		Evaluation circuit status							
	R81		Output data byte Ø							
	R82		Output data byte 1							
	R83		Output data byte 2							

Fig. 10.2-15 Evaluation circuit

Designation	Label/ Adress	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
Output gate reset	$\overline{W90}$								H	
Output gate Control	$\overline{W91}$				H for Clock3	L for Clock3	H with Control2	H with Control1	H with Sweep	
Pre-latch increment	$\overline{W92}$	Step width								
Pre-latch increment	$\overline{W93}$						Step width			
Latch Field length -1	$\overline{W94}$	Possibly DX	32-1 D6	797-1 D5	2047-1 D4	79-1 D3	Possibly others D2	D1	DØ	
Latch Field length -1	$\overline{W95}$	-	-	-	Higher values of W84 D4	D3	D2	D1	DØ	
Synchronization FF	$\overline{W96}$	Direct access to PR input of sync. FF								
Range division	$\overline{W97}$	-	-	-	-	A13	A12	A11	A10	
Mode selection	$\overline{W98}$	Res.	A12	A11	H with PRS	H with Byp. on or with oct.8085	L with octet of 8085	H with PDG-84 OFF	H with quasi-sine	
Mode selection	$\overline{W99}$	Res.	Res.	A12	A11	H with offset	H with μ-law	H with offset	H with subfr. & offset	
Level setting	$\overline{W9A}$	D7	D6	D5	D4	D3	D2	D1	LSB DØ	
Level setting	$\overline{W9B}$	-	-	-	MSB D4	D3	D2	D1	DØ	
Octet of 8085	$\overline{W9A}$	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	
Sub. frequencies	$\overline{W9A}$	A8	A7	A6	A5	X	X	X	X	
Offset	$\overline{W9A}$	A8	A7	A6	A5	A4	A3	A2	A1	
	$\overline{W9C}$	as $\overline{W98}$								
	$\overline{W9D}$	as $\overline{W93}$								
	$\overline{W9E}$	as $\overline{W9A}$								
	$\overline{W9F}$	as $\overline{W9B}$								

Fig. 10.2-16 PDG-64

Designation	Label/ Adress	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
PCM-30 Clock circuit	WCØ	-	Frequency detector ON/OFF	LOOP 2Mbit/s ALL TS	H=PLL L=INT. OSC.	PLL c/o switch B	A	Clock source circ. B	A	00
Timeslot (frame IC)	WC1	—		32	TIMESLOT 16	8	4	2	1	01
Frame (frame IC)	WC2	00 G.732/TS16 INT 01 G.732/TS16 EXT 10 1 ... 21 11 0 ... 31		Frame structure		TIMESLOT 1 (17) ... 15 (31) 8	4	2	1	01
FAS	WC3	1	Ø	Ø	1	1	Ø	1	1	
NOT FAS	WC4	1	1	Ø	1	1	1	1	1	
TS 16 FRM Ø	WC5	MFAS sync. word Ø	Ø	Ø	Ø	MFAS alarm word 1	Ø	1	1	
Signalling TST/ Free TS	WC6	Signalling TST a 1	b 1	c 1	d 1	Signalling Free TS a 1	b 1	c 1	d 1	
Frame test Dial. sign. dist. Ext. dialling sig.	WC7	-	-	MFAS ERR OFF/ON	CRC ERR OFF/ON	FAS/MFRM Error ratio B	A	MFRM ERROR ≅ H	FAS ERROR ≅ H	
FAS ERROR CRC ERROR	WC8	x	x	x	x	x	x	x	x	
FAS ERROR CRC ERROR	WC9	x	x	x	x	x	x	x	x	
PDG-64 64 kbit/s input OCTET 8085	WCA	OCTET 8085 in FREE TS	in TST	Only in FREE B	64 kbit/s input in FREE B	in TS16 CCITT	in TST	PDG-64 in FREE TS	in TST	
OCTET 8085	WCB	1	1	Ø	1	Ø	1	Ø	1	
LOOP AIS CODE	WCC	— 120/75Ω	Insertion OFF ≅ H	Tandem opera-tion	LOOP 2M/ALL TS	LOOP SEL.TS ≅ H	AIS ≅ H	CODE		
Signalling	WCD	-	-	-	-	Signal dist. bit selection		Sig.dis. ≅ H	Ext. sig ≅ H	
Reserve	WCE									
CRC circuit	WCF	x	x	CRC MFAS ERR 3 IN 4	S1-T	S2-T	CRC ERR ON	CRC-4 CRC-6	NORMAL EXTEND.	

Fig. 10.2-17 PCM-30 generator

Designation	Label/ Adress	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
PCM-30 Clock circuit	WCØ	-	Frequency detector ON/OFF	LOOP 2Mbit/s	H ≙ PLL L ≙ INT OSC	PLL c/o switch B	A	Clk source c/o switch B	A	
CLOCK INT 2048 kHz	WCØ	-	Ø	Ø	Ø	X	X	Ø	Ø	
CLOCK EXT 2048 kHz	WCØ	-	1	Ø	Ø	X	X	Ø	1	
CLOCK EXT 8 kHz	WCØ	-	1	Ø	1	1	Ø	Ø	Ø	
CLOCK FROM RECEIVER	WCØ	-	Ø	?	Ø	X	X	1	Ø	
MUX TELEPH CHANNEL CODIR	WCØ	-	Ø	Ø	1	Ø	Ø	Ø	Ø	
MUX TIME SLOT 16 CODIR	WCØ	-	Ø	Ø	1	Ø	1	Ø	Ø	
G.732/TS 16 EXT. CODIR	WCØ	-	Ø	Ø	1	Ø	1	Ø	Ø	
LOOP 2 Mbit/s ALL TS	WCO	-	Ø	1	Ø	X	X	1	Ø	

Fig. 10.2-18 PCM-30 generator (GATE WCØ)

Designation	Label/ Adresse	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
Timeslot setting (frame IC) TST	WC1	-	-	Binary timeslot number 2^5	2^4	2^3	2^2	2^1	2^0	
Timeslot Ø	WC1	-	-	Ø	Ø	Ø	Ø	Ø	Ø	
to										
timeslot 31	WC1	-	-	Ø	1	1	1	1	1	
Frame structure + timeslot (frame IC)	WC2	Frame struc. sett. on hardware PCM-30 generator		Frame structure setting in frame IC		Timeslot number 1 (17) ... 15 (31) 2^3	2^2	2^1	2^0	
G.732/TS 16 INT	WC2	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	
Timeslot (1+17) to										
G.732/TS 16 EXT	WC2	Ø	1	Ø	Ø	1	1	1	1	
Timeslot (15+31)										
G.732/TS 16 TELEPH	WC2	1	Ø	Ø	1					
ALL 32 TS TELEPH	WC2	1	1	1	1					

Fig. 10.2-19 PCM-30 generator (GATES WC1 + WC2)

Designation	Label/ Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
	WC7	-	-	MFAS ERR OFF/ON	CRC ERR OFF/ON	FAS/MFRM error ratio B	A	MFRM ERROR=H	FAS ERROR=H	
FAS ERROR	WC7	-	-	0	0	X	X	0	ON≙1 OFF≙0	
FAS ERROR 10^{-4}	WC7	-	-	0	0	0	0	0	1	
FAS ERROR 10^{-3}	WC7	-	-	0	0	0	1	0	1	
FAS ERROR 2 IN 4	WC7	-	-	0	0	1	0	0	1	
FAS ERROR 3 IN 4	WC7	-	-	0	0	1	1	0	1	
MFRM ERROR	WC7	-	-	0	0	X	X	ON≙1 OFF≙0	0	
MFRM ERROR 1 IN 2	WC7	-	-	0	0	0	0	1	0	
MFRM ERROR 1 IN 1	WC7	-	-	0	0	0	1	1	0	
CRC-ERROR	WC7	-	-	0	ON≙1 OFF≙0	X	X	0	0	
MFAS ERROR CRC	WC7	-	-	ON≙1 OFF≙0	0	X	X	0	0	

Fig. 10.2-20 PCM-30 generator (GATE WC7)

Designation	Label/ Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
Value	WC8	2^7 (128)	2^6 (64)	2^5 (32)	2^4 (16)	2^3 (8)	2^2 (4)	2^1 (2)	2^0 (1)	
Value	WC9	2^{15} (32768)	2^{14} (16384)	2^{13} (8192)	2^{12} (4096)	2^{11} (2048)	2^{10} (1024)	2^9 (512)	2^8 (256)	
FAS ERROR 10^{-4}	WC8	1	0	0	1	0	1	0	0	
FAS ERROR 10^{-4}	WC9	0	0	0	0	0	1	0	1	
FAS ERROR 10^{-3}	WC8	1	0	0	0	1	1	1	0	
FAS ERROR 10^{-3}	WC9	0	0	0	0	0	0	0	0	
FAS ERROR 2 IN 4	WC8	0	0	0	0	0	0	0	1	
FAS ERROR 2 IN 4	WC9	0	0	0	0	0	0	0	0	
FAS ERROR 3 IN 4	WC8	0	0	0	0	0	0	1	1	
FAS ERROR 3 IN 4	WC9	0	0	0	0	0	0	0	0	
CRC ERR X 908/1000	WC8	0	0	1	0	1	1	0	0	
CRC ERR X 908/1000	WC9	0	0	0	0	1	1	1	0	
CRC ERR X 914/1000	WC8	0	1	0	0	0	1	0	0	
CRC ERR X 914/1000	WC9	0	0	0	0	1	1	1	0	
CRC ERR X 920/1000	WC8	0	1	0	1	1	1	0	0	
CRC ERR X 920/1000	WC9	0	0	0	0	1	1	1	0	

Fig. 10.2-21 PCM-30 generator (GATES WC8 + WC9)

Designation	Label/ Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
	WCA	OCTET 8085 In FREE TS	In TST	64 kbit/s input Only in FREE TS	In FREE TS	In TS 16 CCITT	In TST	PDG-64 In FREE TS	In TST	
PDG-64 in all TST (in SELECTED CHANNEL)	WCA	0	0	0	0	0	0	0	1	
PDG-64 in all TS (in ALL TS)	WCA	0	0	0	0	0	0	1	1	
PDG-64 in FREE TS (in ALL CH. EXCL. SELECTED)	WCA	0	0	0	0	0	0	1	0	
64 kbit/s input in TST (in SELECTED CHANNEL)	WCA	0	0	0	0	0	1	0	0	
64 kbit/s input in TS 16	WCA	0	0	0	0	1	0	0	0	
64 kbit/s input in all TS (in ALL TS)	WCA	0	0	0	1	0	1	0	0	
64 kbit/s input in FREE TS (in ALL CH. EXCL. SELECTED)	WCA	0	0	1	1	0	1	0	0	
OCTET 8085 in TST	WCA	0	1	0	0	0	0	0	0	
OCTET 8085 in FREE TS	WCA	1	0	0	0	0	0	0	0	

Fig. 10.2-22 PCM-30 generator (GATE WCA)

Designation	Label/ Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
	WCC	120/$\overline{75\Omega}$	Insertion OFF ≙ H	Tandem operat.	LOOP 2M ≙ H	LOOP Sel.TS≙H	AIS ≙ H	CODE 2	1	
NRZ	WCC	0	0	0	0	0	0	1	1	
AMI	WCC	0	0	0	0	0	0	0	1	
HDB-3	WCC	0	0	0	0	0	0	0	0	
AIS	WCC	0	0	0	0	0	ON≙1 OFF≙0	0	0	
LOOP 2M SEL. TS	WCC	0	0	0	0	ON≙1 OFF≙0	0	0	0	
LOOP 2M ALL TS	WCC	0	0	0	ON≙1 OFF≙0	0	0	0	0	
Tandem operation	WCC	0	1	ON≙1 OFF≙0	0	0	0	0	0	
Tandem operation Insertion "ON"	WCC	0	0	1	0	0	0	0	0	
Output imp. 75 Ω coaxial	WCC	0								
Output imp. 120 Ω balanced	WCC	1								

Fig. 10.2-23 PCM-30 generator (GATE WCC)

Designation	Label/ Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
	WCD	-	-	-	-	Signal dist. a,b,c,d	selec.	Signal dist.	External sig. ≙ H	
External signal from quartet socket	WCD	-	-	-	-	X	X	X	ON≡1 OFF≙0	
Signal distortion	WCD	-	-	-	-	X	X	ON≡1 OFF≙0	X	
Signal distortion on bit a	WCD	-	-	-	-	0	0	1	X	
Signal distortion on bit b	WCD	-	-	-	-	0	1	1	X	
Signal distortion on bit c	WCD	-	-	-	-	1	0	1	X	
Signal distortion on bit d	WCD	-	-	-	-	1	1	1	X	

Fig. 10.2-24 PCM-30 generator (GATE WCD)

Designation	Label/ Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Re-marks
Timeslot setting	WDØ	-	-	-	>TS16≡H <TS16≡L	-	-	-	-	
OCTET display Sig. bit output	WD3	-	Sig.bit SELECT		DISPLAY SELECT C	B	A	DISP sig. ON/$\overline{OFF}$	LED DISPL ON/$\overline{OFF}$	
Outp. -> PDA-64 Outp. -> 64 kbit/s output	WD4	-	-	-	-	⊖→ PDA-64 TSR/TSØ	ON/$\overline{OFF}$	⊖→64 kbit/s outp. TSR/TS16 CCITT	ON/$\overline{OFF}$	
Card poll Signal poll	RDØ	NO EXT. FRM 8KHz≡H	8 KHz ≙ H	2048KHz ≙ H	NO EXT. CLOCK≡H	Ground	Ground	T1 fitted ≙ L	PCM-30 fitted ≙ L	
Alarm poll current status	RD1	NO SIGNAL	AIS	NO FRAME	NO EXT. FRM.	NO MFRM	- Ground	- Ground	- Ground	
Interrupt poll	RD2	NO SIGNAL	AIS	NO FRAME	NO EXTEND. FRAME	NO MFRM	- Ground	- Ground	- Ground	
FAS	RD3	Bit 1 .1	2 0	3 0	4 1	5 1	6 0	7 1	Bit 8 1	
NOT FAS	RD4	1	1	0	1	1	1	1	1	
SEL. CHANNEL	RD5									
MAS/NOT MAS	RD6	0	0	0	0	1	0	1	1	
Signalling TS 16 signalling	RD7	-	-	-	-	Bit a (1/5)	Bit b (2/6)	Bit c (3/7)	Bit d (4/8)	
	RD8									
	RD9									
	RDA									
	RDB									
	RDC									
	RDD									
	RDE									
CRC circuit*	RDF	CRC $\overline{\text{card fitted}}$	1	1	1	1	1	S_1-R	S_2-R	

Fig. 10.2-25 PCM-30 receiver 2

* From Series E...

Designation	Label/ Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Remarks
Timeslot TSR (frame IC addr. Ø)	$\overline{WDØ}$	-	-	32 2^5	16 2^4	Timeslot 2^3	2^2	2 2^1	1 2^0	
Timeslot Ø to timeslot 31	$\overline{WDØ}$	-	-	0	0	0	0	0	0	
	$\overline{WDØ}$	-	-	0	1	1	1	1	1	
Frame structure + timeslot	$\overline{WD1}$	Frame structure PCM-30	EMPF.	Frame structure Frame IC		Timeslot 1(17) ... 15(31) 2^3	2^2	2^1	2^0	
G.732/TS 16 INT. timeslot (1/17) to G.732/TS 16 EXT. timeslot (15/31)	$\overline{WD1}$	0	0	0	0	0	0	0	1	
	$\overline{WD1}$	0	1	0	0	1	1	1	1	
G.732/TS 16 TELEPH.	$\overline{WD1}$	1	0	0	1					
ALL 32 TS TELEPH.	$\overline{WD1}$	1	1	1	1					
	$\overline{WD2}$	TEST	-	-	Output MFRM.ERR ON/$\overline{OFF}$	LOOP ALL TS	$\overline{AMI}$/ $\overline{HDB}$	Input > 3KΩ	Input NRZ	
LOOP 2M ALL TS PARAM. 121	$\overline{WD2}$	0	-	-	X	1	X	X	X	
LOOP OPEN PARAM. 123	$\overline{WD2}$	0	-	-	X	0	X	X	X	
RX LINE IMPEDANCE PARAM. 421 120/75Ω	$\overline{WD2}$	0	-	-	X	X	X	0	X	
RX LINE IMPEDANCE PARAM. 422 > 3KΩ	$\overline{WD2}$	0	-	-	X	X	X	1	X	
RX LINE CODE PARAM. 411 HDB-3	$\overline{WD2}$	0	-	-	X	X	0	X	0	
RX LINE CODE PARAM. 412 AMI	$\overline{WD2}$	0	-	-	X	X	1	X	0	
RX LINE CODE PARAM. 413 NRZ	$\overline{WD2}$	0	-	-	X	X	1	X	1	
MFRM ERR output ON/OFF	$\overline{WD2}$	0	-	-	ON=1 OFF=0	X	X	X	X	
TEST, generator -> Receiver ON/$\overline{OFF}$	$\overline{WD2}$	ON=1 OFF=0	-	-	X	X	X	X	X	

Fig. 10.2-26 PCM-30 receiver 1

Designation	Label/ Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Remarks
Timeslot setting TSR < 16	$\overline{WD0}$	-	-	0	0	X	X	X	X	
Timeslot setting TSR > 16	$\overline{WD0}$	-	-	0	1	X	X	X	X	
TS ASSIGNMENT	$\overline{WD3}$	-	Sig.bit select		DISPLAY SELECT C	B	A	DISP sig ON/$\overline{OFF}$	LED DISP ON/$\overline{OFF}$	
TS ASSIGNMENT <1> TELEPH. CHANNEL	$\overline{WD3}$	-	X	X	0	0	0	0	1	
TS ASSIGNMENT <2> FAS	$\overline{WD3}$	-	X	X	0	0	1	0	1	
TS ASSIGNMENT <3> NOT FAS	$\overline{WD3}$	-	X	X	0	1	0	0	1	
TS ASSIGNMENT <4> MAS/NOT MAS	$\overline{WD3}$	-	X	X	0	1	1	0	1	
TS ASSIGNMENT <6> Signalling chan.	$\overline{WD3}$	-	X	X	0	0	0	1	1	
TS ASSIGNMENT <7> DISPL. OFF	$\overline{WD3}$	-	X	X	X	X	X	X	0	
VAR MODE 831 Signalling on bit a	$\overline{WD3}$	-	0	0	X	X	X	X	X	
VAR MODE 832 Signalling on bit b	$\overline{WD3}$	-	0	1	X	X	X	X	X	
VAR MODE 833 Signalling on bit c	$\overline{WD3}$	-	1	0	X	X	X	X	X	
VAR MODE 834 Signalling on bit d	$\overline{WD3}$	-	1	1	X	X	X	X	X	
	$\overline{WD4}$	-	-	-	-	⊖→ PDA-64 $\overline{TSR}$/TSØ	ON/$\overline{OFF}$	⊖→ 64 kbit/s outp. $\overline{TSR}$/TS16	ON/$\overline{OFF}$	
8kHz, 64kHz, 64kbit/s to 64 kbit/s output OFF (high imped.)	$\overline{WD4}$	-	-	-	-	X	X	X	0	
TSR to 64 kbit/s output	$\overline{WD4}$	-	-	-	-	X	X	0	1	
TS 16 CCITT to 64 kbit/s output	$\overline{WD4}$	-	-	-	-	X	X	1	1	
8kHz, 64kHz, 64kbit/s to PDA-64 OFF (high imped.)	$\overline{WD4}$	-	-	-	-	X	0	X	X	
TSR to PDA-64	$\overline{WD4}$	-	-	-	-	0	1	X	X	
TSØ to PDA-64	$\overline{WD4}$	-	-	-	-	1	1	X	X	

Fig. 10.2-27 PCM-30 receiver 2

SCC card (screen control card)

Graphic I/O assignments

Address	I/O	Gate	Mirror word	Assignment
60	O	CMD	DCMD	See Data Sheet EF9365
60	I	STATUS	DCMD	See Data Sheet EF9365
61	I/O	CTRL1	DCTRL1	See Data Sheet EF9365
62	I/O	CTRL2	DCTRL2	See Data Sheet EF9365
63	I/O	CSIZ	DCSIZ	See Data Sheet EF9365
65	I/O	DELTAX	DDELTX	See Data Sheet EF9365
67	I/O	DELTAY	DDELTY	See Data Sheet EF9365
68	I/O	XMSB	DXMSB	See Data Sheet EF9365
69	I/O	XLSB	DXLSB	See Data Sheet EF9365
6A	I/O	YMSB	DYMSB	See Data Sheet EF9365
6B	I/O	YLSB	DYLSB	See Data Sheet EF9365
6C	I	XLP		See Data Sheet EF9365
6D	I	YLP		See Data Sheet EF9365
70	O	CTRLO	DCTRLO	/W3/W1/W2/nD3/nD1/nD2/nExp/clr/ n = not (inverted) W = write D = display Exp = Level 2 expanded clr = SCC interrupt inhibited

Fig. 10.2-28 Graphic I/O assignments

10.3 EVALUATION CIRCUIT TABLES

10.3.1 TABLE OF EVALUATION CIRCUIT MODES

(Mode = Mode & Submode; e.g.: Mode = 2H, Submode = 1H - Mode = 21H) from Series E ...

MODE		SUBMODE		PARAMETERS
0	RESULT OUTPUT	0 to F	Output of result No. "SUBMODE" into the four output registers (status register and output data registers 0-2). This is the only mode where their is no status message.	No parameters
1	PARAMETER INPUT	0 to F	Transfer of parameter No. "SUBMODE" to evaluation circuit. The parameter is max. 3 bytes long.	W_81: LSByte of parameter W_82: 2nd byte of parameter W_83: MSByte of parameter
2	LEVEL MEASUREMENT	0 1 2 4 6 7	Analog in band Digital in band Analog out-of-band (4-128 kHz) Analog random sub-sampling (20 Hz - 72 kHz) As 20, but with delayed start of measurement As 21, but with delayed start of measurement	W_81, W_82: Sample No. (W_81 = LSByte) W_83: Analog: -- Digital: 000LDDDD (= Bit 7...Bit 0) with L=0: A-law, L=1: µ-law DDDD: Dig. expansion factor PARAMETER No. 0: ..... For BA 22: Offset (I2) For BA 26,27: Wait time in ms (16bit w/o del.)
3	S/Q MEASUREMENT	0 1 2 3	Analog without intrinsic noise correction Digital without intrinsic noise correction Analog with intrinsic noise correction Digital with intrinsic noise correction	W_81, W_82: Sample No. (W_81 = LSByte) W_83: Analog: -- Digital: 000LDDD (= Bit 7...Bit 0) with L=0: A-law, L=1: µ-Law DDDD: Dig. expansion factor PARAMETER No. 0: ..... For BA 32, 33: Intrinsic noise, (I2), in mB Range: -65.0 0dB...-90.0 0dB
4	ERROR MEASUREMENT	0 1 2 3	For 64 kbit/s and pseudo-random seq. 2^9-1 For 64 kbit/s and pseudo-random seq. 2^{11}-1 For 64 kbit/s and variable octet of the frame signals (FAS, MFRM, CRC)	W_81, W_82, W_83: Measuring time as number of seconds (W_81 = LSByte) PARAMETER No. 0: ..... For BA 42: Transm. octet (byte, PCM code)
5	GROUP DELAY MEASUREMENT	0 1 2 3 4 5 6 7	Analog, conf. A-A, split frequency 41.6 Hz Digital, conf. A-D, split frequency 41.6 Hz Analog, conf. D-A, split frequency 41.6 Hz Digital, conf. D-D, split frequency 41.6 Hz As 50, but split frequency 83.3 Hz As 51, but split frequency 83.3 Hz As 52, but split frequency 83.3 Hz As 53, but split frequency 83.3 Hz	W_81, W_82: Sample No. (W_81 = LSByte) W_83: Analog: -- Digital: 000LDDDD (Bit 7...Bit 0) with L=0: A-law, L=1: µ-Law DDDD: Dig. expansion factor PARAMETER No. 0: ..... Meas. freq. in Hz (= carrier freq.), (I2)

Fig. 10.3.1-1 Table of evaluation circuit modes

MODE		SUBMODE		PARAMETERS
6	CODER MEASUREMENTS	0 1 2 3	Load limit measurement Peak-load measurement (CWmin, CWmax) Coder offset for A-law Coder offset for μ-law	W_81, W_82: Sample No. (W_81 = LSByte)
7	SIGNALLING DISTORTION MEAS.	0 1	Analog Digital	W_81, W_82: Meas. time as number of periods of sig. signal W_83: Debouncing time in ms
8 to C	Not used			
D	MONITOR	0 1 2 3 4	WRITE (value_16-) address_16) OUT (value_8-) address_8) READ (address_16 -) result_16) IN (address_8 -) result_8) START (Start address: address_16)	Value_16: Parameter No. 0 Value_8: W_81 Address_16: W_81, W_82 (LSB, MSB) Address_8: W_81 Result_16: R_81, R_82 (LSB, MSB) Result_8: R_81
E	TEST	0 1 2 3 4 5 6 7 8 9 A B C	Output of software status I/O interface test (W_80-W_83, R_80-R_83) ROM test RAM test 1 (non-destructive) RAM test 2 (destructive) Re-initialization (with RAM, ROM test) Output of 00H into R_80 - R_83 Output of FFH into R_80 - R_83 Output of AAH into R_80 - R_83 Output of 55H into R_80 - R_83 Read and output signal inputs I/O address decoder stimulus program Set control registers	No parameters After start: W_80-W_83: test pattern No parameters No parameters No parameters No parameters No parameters No parameters No parameters No parameters No parameters No parameters W_81: Byte to be output
F	SOFT_RESET INTERRUPTION	0 F	Interrupts the current measurement and starts re-initialization. Interrupts the current measurement; the eval. circ. then awaits a new input.	No parameters No parameters

Fig. 10.3.1-1 Table of evaluation circuit modes (contd.)

10.3.2 TABLE OF MODE-DEPENDENT RESULTS OF THE EVALUATION CIRCUIT

(UI: 8 bits without sign U2: 16 bits without sign P1: 8 bits PCM coding)
(I1: 8 bits 2 s complement (ZWK) I2: 16 bits ZWK I4: 32 bits ZWK)
(F4: LS value: mantissa 1000...9999, MSW word: exponent)

from series E...

MODE		RESULTS				
No.		No.		Type	Resolution, range	Possible STATUS
20H 24H 26H	LEVEL MEAS., analog ditto, stoch. subsampl. ditto, w. delayed start	0 1 2 3 4	Level of filter 1 Level of filter 2 Transgression frequency Filter 1 offset Filter 2 offset	I4 I4 I2 I2 I2	0.1 mB 0.1 mB 0.01 %, 0...10000 1 LSB, -32767...32767 1 LSB, -32767...32767	32, finished 41, meas. range exceeded 42, signal error
21H 27H	LEVEL MEAS., digital ditto, w. delayed start	0 1 2 3 4	Level of filter 1 Level of filter 2 Byte 0: CWmin Byte 1: CWmax Byte 2: ICWImax Filter 1 offset Filter 2 offset	I4 I4 P1 P1 I1 I2 I2	0.1 mB 0.1 mB -127...-0, +0...127 -127...-0, +0...127 0...127 1 LSB, -32767...32767 1 LSB, -32767...32767	32, finished 41, meas. range exceeded 42, signal error
22H	LEVEL MEAS., out-of band	0 1 2 3 4	Level As result No. 0 - AMOUNT (U_rms_gl-U_offset) As result No. 3	I4 I4 I2 I2	0.1 mB As No. 0 0...32767 As No. 3	32, finished 41, meas. range exceeded
30H 32H	S/Q MEAS., analog ditto, w. noise corr.	0 1 2 3 4 5	Level of filter 1 (S) Level of filter 2 (Q) Transgression frequency Filter 1 offset Filter 2 offset S/Q ratio	I4 I4 I2 I2 I2 I4	0.1 mB 0.1 mB 0.01 %, 0...10000 1 LSB, -32767...32767 1 LSB, -32767...32767 0.1 mB	33, finished 41, meas. range exceeded 42, signal error
32H 33H	S/Q MEAS., digital ditto, w. noise corr.	0 1 2 3 4 5	Level of filter 1 (S) Level of filter 2 (Q) Byte 0: CWmin Byte 1: CWmax Byte 2: ICWImax Filter 1 offset Filter 2 offset S/Q ratio	I4 I4 P1 P1 I1 I2 I2 I4	0.1 mB 0.1 mB -127...-0, +0...127 -127...-0, +0...127 0...127 1 LSB, -32767...32767 1 LSB, -32767...32767 0.1 mB	33, finished 41, meas. range exceeded 42, signal error
40H 41H 42H	ERROR MEAS., PRS 2^9-1 ditto, PRS 2^{11}-1 ditto, variable octet	0 1 2 3 4	Bit error Octet error Bit error ratio Octet error ratio Error-free seconds	I4 I4 F4 F4 I4	0...2^{31}-1 0...2^{31}-1 1.000E-10...1.000E0 1.000E-10...1.000E0 0.01 %, 0...10000	34, finished 44, NoSync at start 47, NoSync during meas.

Fig. 10.3.2-1 Table of mode-dependent results of the evaluation circuit

MODE		RESULTS				
No.		No.		Type	Resolution, range	Poss. STATUS
43H	ERROR MEAS., frame sig.	0	FAS bit error	I4	$0...2^{31}-1$	34, finished
		1	FAS word error	I4	$0...2^{31}-1$	44, NoSync
		2	MFRM error	I4	$0...2^{31}-1$	
		3	CRC error	I4	$0...2^{31}-1$	
		4	FAS bit error ratio	F4	1.000E-10...1.000E0	
		5	FAS word error ratio	F4	1.000E-10...1.000E0	
50H 52H 54H 56H	GROUP DELAY MEAS, A-A ditto, D-A	0	Signal level	I4	0.1 mB	35, finished
		1	As result No. 0	I4	As No. 0	41, meas. range exceeded
		2	Transgression frequency	I2	0.01 %, 0...10000	
		3	Signal offset	I2	1 LSB, -32767...32767	42, signal error
		4	As result No. 3	I2	As No. 3	
		5	--			
		6	Group delay	I4	0.1 µs, 0...240000	
51H 53H 55H 57H	GROUP DELAY MEAS. A-D ditto, D-D	0	Signal level	I4	0.1 mB	35, finished
		1	As result No. 0			41, meas. range exceeded
		2	Byte 0: CWmin	P1	-127...-0, +0...127	
			Byte 1: CWmax	P1	-127...-0, +0...127	42, signal error
			Byte 2: ICWImax	I1	0...127	
		3	Signal offset	I2	1 LSB, -32767...32767	
		4	As result No. 3			
		5	--			
		6	Group delay	I4	0.1 µs, 0...240000	
60H	LOAD LIMIT MEASUREMENT	0	Rel. load limit with CW=127	I4	0.1 mB	36, finished
		1	Rel. load limit with CW=127	I4	0.1 mB	40, input error
		2	LSWord: No. of CW -127	I2		45, Send level too low
			MSWord: No. of CW +127	I2		46, Send level too high
61H	PEAK LOAD MEASUREMENT	0	Byte 0: CWmin	P1	-127...-0, +0...127	36, finished
			Byte 1: CWmax	P1	-127...-0, +0...127	
			Byte 2: ICWImax	I1	0...127	
62H 63H	CODER OFFSET, A-law ditto, µ-Law	0	Coder offset	I1	-127...+127	36, finished
		1	Coder offset w. NC digit	I2	-1270...+1270	
		2	Linear offset	I2	-32767...+32767	
70H 71H	SIG. DIST. MEAS., analog ditto, digital	0	Mean duty cycle	I2	0.01 %, 0...10000	37, finished 42, signal error
D0H D1H D4H	Monitor, WRITE Monitor, OUT Monitor, START	-	No result	-	-	3D, finished
D2	Monitor, READ	-	Res. available immediately	R_81	R_82 (LSB, MSB): value read	3D, finished
D3	Monitor, IN	-	Res. available immediately	R_81	8-bit value read	3D, finished

Fig. 10.3.2-1 Table of mode-dependent results of the evaluation circuit (contd.)

MODE		RESULTS				
No.		No.		Type	Resolution, range	Poss. STATUS
E0H	Software version	-	Result (4 byte) available immediately, no status	R_80 R_81	Version No. R_83: Software No. (984-0190)	--
E1H	I/O test	-	Content of W_80 - W_83 transferred dynamically to R_80 - R_83 until OFFH written into W_80			
E2H	ROM test	-	--	-	STATUS: R_80=3EH, finished w. test R_81=0: EPROMs o.k. 1: LSB EPROM faulty 2: MSB EPROM faulty 3: Both EPROMs faulty	
E3H E4H	RAM test, non-destr. RAM test, destructive	0	LSW: Error count LSB-RAM MSW: Error count MSB-RAM	-	STATUS: R_80=3EH, finished w. test R_81=0: RAMs o.k. 1: LSB RAM faulty 2: MSB RAM faulty 3: Both RAMs faulty	
E6H to E9H	Test of computer interface (output direction)	-	No status!	-	R_80 to R_83: 00000000H (for E6H) FFFFFFFFH (for E7H) AAAAAAAAH (for E8H) 55555555H (for E9H)	
EAH	Signal input test	-	No status!	R_80:LSB of filter output signal (CWFIL) R_81:MSB of filter-output signal (CWFIL) R_82:PCM octet signal (OCTET) R_83:Signal gate: (Bit0: SL 6c ; Bit1: SL 5c Bit2: SL 14b; Bit3: SL 8c)		
EBH ECH	I/O address decoder test Set control registers	-	No results	-	-	-
E5H F0H RES	Re-initialization Interruption with re-init. and after hardware RESET	-	--	-	R_80=F0H: Initialized, RAM/ROM o.k. =F1H: Initialized, RAM/ROM faulty R_81,Bit0: LSB ROM faulty Bit1: MSB ROM faulty Bit2: LSB RAM faulty Bit3: MSB RAM faulty	
FFH	Interruption	-	-	-	STATUS: = 5XH, interruption in Mode X	

Fig. 10.3.2-1 Table of mode-dependent results of the evaluation circuit (contd.)

The following applies for all modes (except E4, E5, F0):

1. Result No. 14: Eval. circ. status b e f o r e start of measurement
2. Result No. 15: Eval. circ. status a f t e r start of measurement

The following applies for all modes:

Status "2XH" (= busy with MODE No. X) is output during the measurement

Example:

Select CPU 2/3,

```
O: 80.E5 ENTER -> ! Re-initialization takes place
I: 80.ENTER -> F0! RAM/ROM test is tested: F0 = o.k.

O: 80.E8 ENTER -> ! Write AAH into 80H to 83H (O: 81.AA ...)
I: 80.ENTER -> AA! ENTER ->   }
I: 81.AA ! ENTER ->           }  Read AAH into 80H to 83H
I: 82.AA ! ENTER ->           }
I: 83.AA !                    }
```

10.3.3 TABLE OF STATUS INFORMATION OF THE EVALUATION CIRCUIT, VØØ

(Status information = Status & Substatus; e.g.: Status = 2H, Substatus = 1H-
Status inf. = 21H)

STATUS	SUBSTATUS	DESCRIPTION
0	0 ... F	Not used
1	X = 0 ... F	Parameter No. "X" entered in parameter buffer
2	X = 0 ... F	Busy with Mode No. "X"
3	X = 0 ... F	Finished with Mode No. "X"
4	X = 0 ... F	Error No. "X"
5	X = 0 ... F	Interruption in Mode No. "X"
6	X = 0 ... F	Interm. result No. "X" present in R_81 ... R_83
7 to E	0 ... F	Not used
F	0	Initialization completed, RAM and ROM test o.k.
F	1	Initialization completed, RAM and/or ROM test not o.k.

Fig. 10.3.3-1 Table of the status information of the evaluation circuit

10.3.4 TABLE OF THE ERROR MESSAGES OF THE EVALUATION CIRCUIT, VØØ

STATUS	DESCRIPTION
40	INPUT ERROR: 1. Entry of a non-existent mode 2. Parameter error
41	MEASURING RANGE EXCEEDED: (measurement not interrupted, results nevertheless available) 1. Analog level, S/Q meas.: Filter signal value ±32767 has occurred; the "transgression frequency" states how often (in % of No. of samples) 2. Digital level, S/Q meas.: Transgression of the PCM octet range specified by the "Dig. expansion" parameter in either direction
42	MEAS. SIGNAL ERROR: 1. Level, S/Q measurement: DC voltage, no AC component in Filter1 or Filter2 signal 2. Group delay measurement: Ratio of side-to-carrier line deviates by more than ± 2 dB 3. Signalling distortion meas.: No signal change or signal not in frequency range
44	NO SYNCHRONIZATION AT START OF MEASUREMENT: 1. Frame error measurement: No synchronization with FAS signal 2. 64 kbit/s error meas.: No synchronization with pseudo-random sequence 3. Group delay measurement: Error in sampling clock
45	1. Load limit measurement: Send level too high
46	1. Load limit measurement: Send level too low
47	NO SYNCHRONIZATION DURING MEASUREMENT: 1. 64 kbit/s error meas.: Loss of synchronization with pseudo-random sequence
4F	INTERNAL ERROR

Fig. 10.3.4-1 Table of the error messages of the evaluation circuit

10.3.5 MEASURING MODULES

	COMMUNICATION:
ERGEB_AUS	Result output to 8085
PARAM_EIN	Parameter input from 8085
	LEVEL MEASUREMENT:
PMESS_ANA	Analog
PMESS_DIG	Digital
PEG_ABAND	Out-of-band measurement
PMESS_ANA	Pseudo-random subsampling
PM_WART_A	Analog, with delayed start of measurement
PM_WART_D	Digital, with delayed start of measurement
	S/Q MEASUREMENT:
SQMESS_ANA	Analog
SQMESS_DIG	Digital
SQ_ANA_ND	Analog with noise reduction
SQ_DIG_ND	Digital with noise reduction
	ERROR MEASUREMENT:
FM_64K_9	Error measurement with 64 kbit/s and PRS 2 9-1
FM_64K_11	Error measurement with 64 kbit/s and PRS 2 11-1
FM_64K_EO	Error measurement with 64 kbit/s and var. octet
FM_FRAME	FAS bit/word error, MFRM, parity error
	DELAY MEASUREMENT:
GRLZM_ANA	Group delay measurement, analog-analog
GRLZM_DIG	Ditto, analog-digital
GRLZM_ANA	Ditto, digital-analog
GRLZM_DIG	Ditto, digital-digital
	PEAK CODE MEASUREMENTS:
AUST_GR	Load limit determination
PEAK_LOAD	Peak load measurement (CWmin, CWmax, ICWImax)
CODER_OFF	Coder offset determination (A-law)
CODER_OFF	Coder offset determination (μ-law)
	SIGNALLING DISTORTION:
WKV_MESS	Analog
WKV_MESS	Digital

	MONITOR FUNCTIONS:
MONIT_W	"W", write
MONIT_O	"O", out
MONIT_R	"R", read
MONIT_I	"I", in
MONIT_S	"S", start
	TEST PROGRAMS:
SW_STAND	Software status poll
IO_TEST	I/O interface test
ROM_TEST	ROM test (checksum test)
RAM_TEST1	RAM test (non-destructive)
RAM_TEST2	RAM test (destructive)
INIT_AWR	Re-initialization, RAM, ROM tests
OUT_00H	Output of 00H to status and output register
OUT_FFH	Output of FFH to status and output register
OUT_AAH	Output of AAH to status and output register
OUT_55H	Output of 55H to status and output register
SIGIN_TST	Read and output signal inputs
IODEC_TST	I/O address decoder stimulus program
SET_STREG	Set control registers
	INTERRUPTS:
INIT_AWR	Interrupt with re-initialization
NMI_BREAK	Normal interrupt

CRC-4 error ratio (from Series E...)

Send side (PCM-30 generator):

N = (number of CRC errors x 4) - 4

908 errors: N = 908 x 4 - 4 = 3628 $\cong$ ØE2C_{HEX}

GATE C8 = 2C

GATE C9 = ØE

914 errors: N = 914 x 4 - 4 = 3652 $\cong$ ØE44_{HEX}

GATE C8 = 44

GATE C9 = ØE

920 errors: N = 920 x 4 - 4 = 3676 $\cong$ ØE5C_{HEX}

GATE C8 = 5C

GATE C9 = ØE

Receive side:

Re-synchronization threshold $\cong$ N + 1

i.e. with N = 913, resynchronization takes place after 914 errors

Error threshold = 914 -> N = 913 $\cong$ Ø391_{HEX}

S1 = 91

S2 = Ø3

S1, S2 = DIL switches on card [984-AY]
(CRC circuit)

CRC-4 MFAS ERR (from Series E ...)

1 IN 4; C7: 20, C8: 1F, CF: 19
2 IN 4; C7: 20, C8: 0F, CF: 19
3 IN 4; C7: 20, C8: 07, CF: 39
4 IN 4; C7: 20, C8: 07, CF: 19

Attenuation factor N = C8 + 1

1 IN 4; N = 32, 32 x 250 µs = 8 ms -> Every 4th CRC MFAS is wrong
2 IN 4; N = 16, 16 x 250 µs = 4 ms -> Every 2nd wrong
3 IN 4; N = 8, 8 x 250 µs = 2 ms
together with attenuator on CRC card, 3 of 4 CRC MFAS are wrong
4 IN 4; every CRC MFAS is wrong

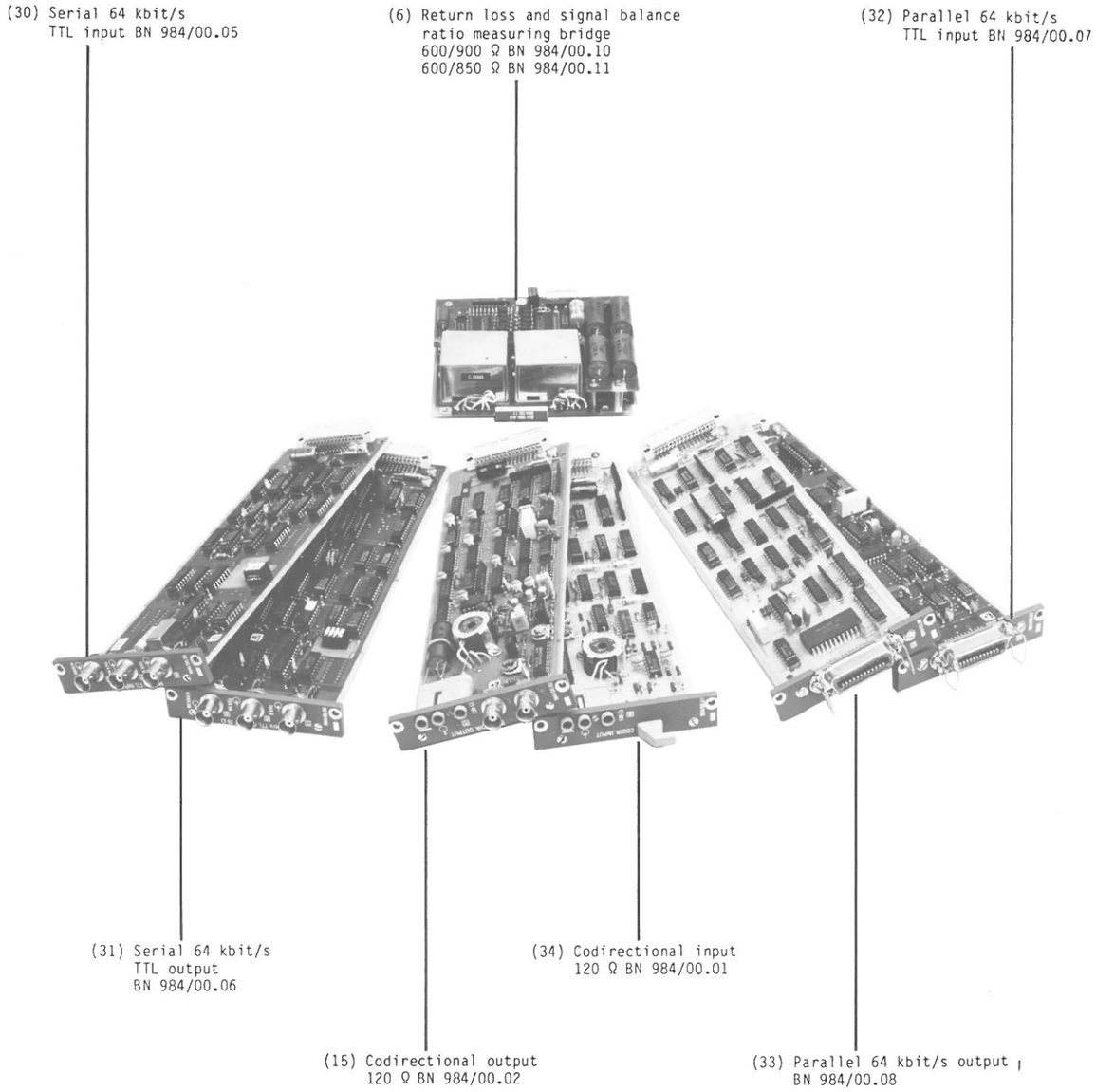
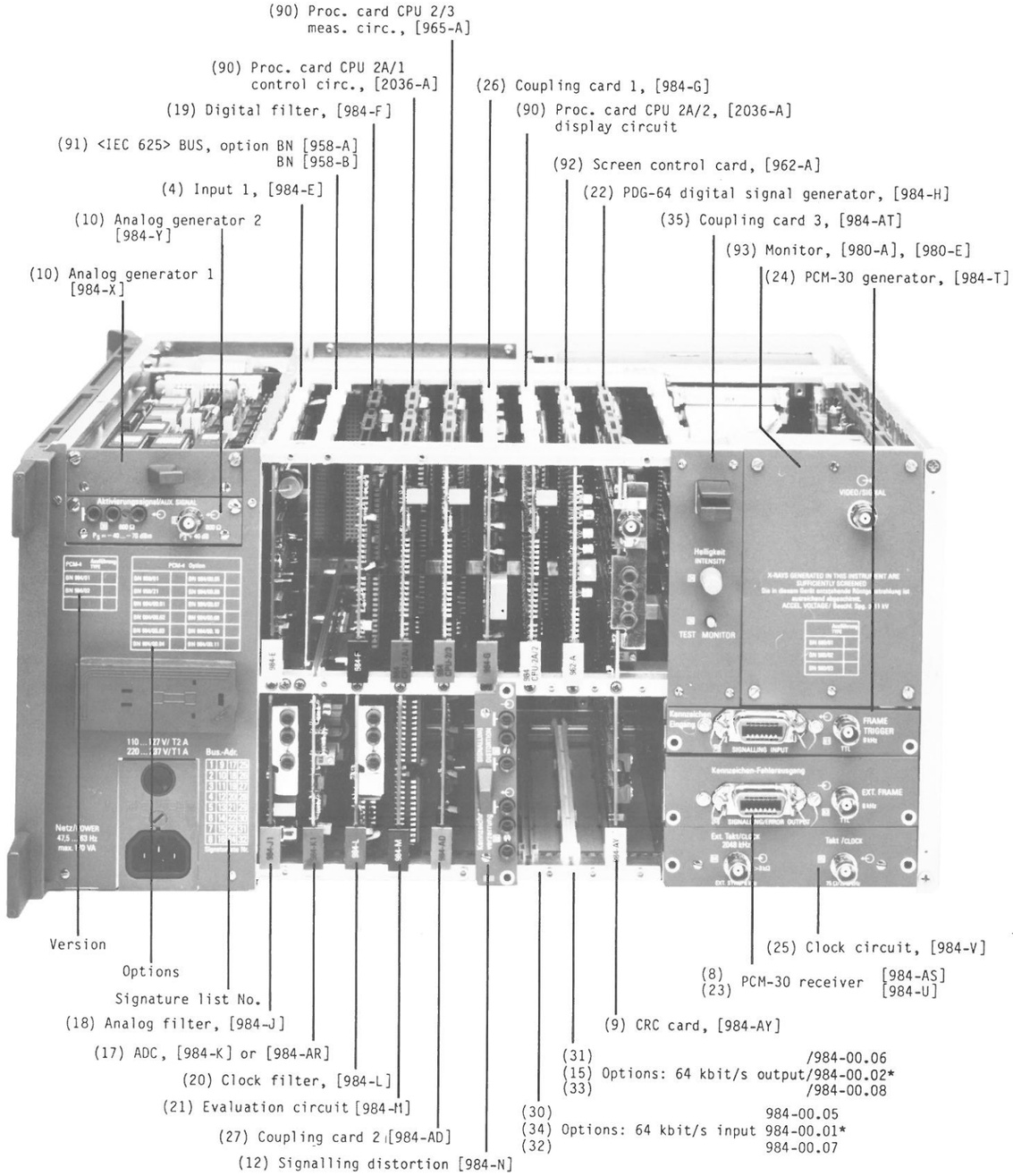


Fig. 10.4-1 PCM-4 options



* Also see Fig. 10.1-2

Fig. 10.4-2 Location of assemblies

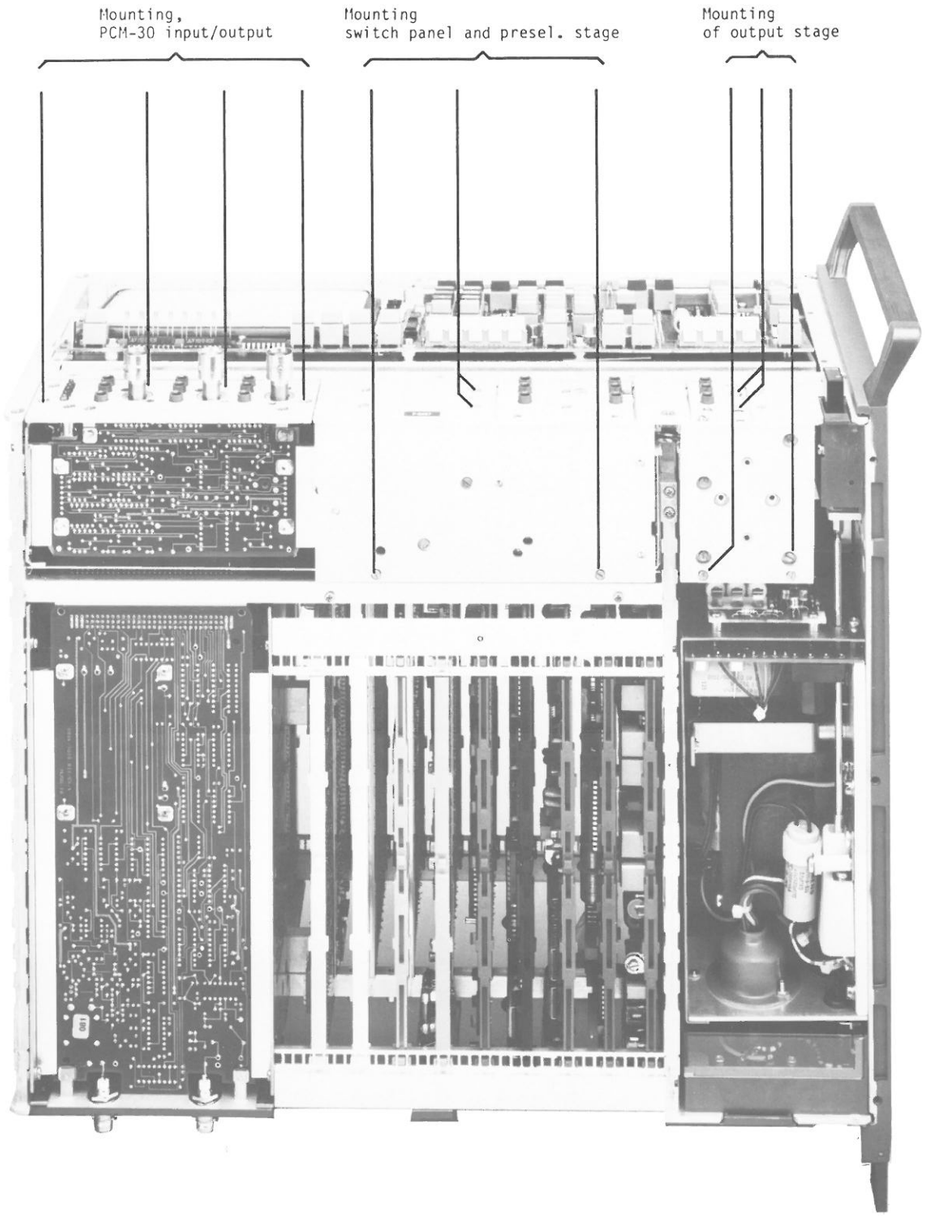
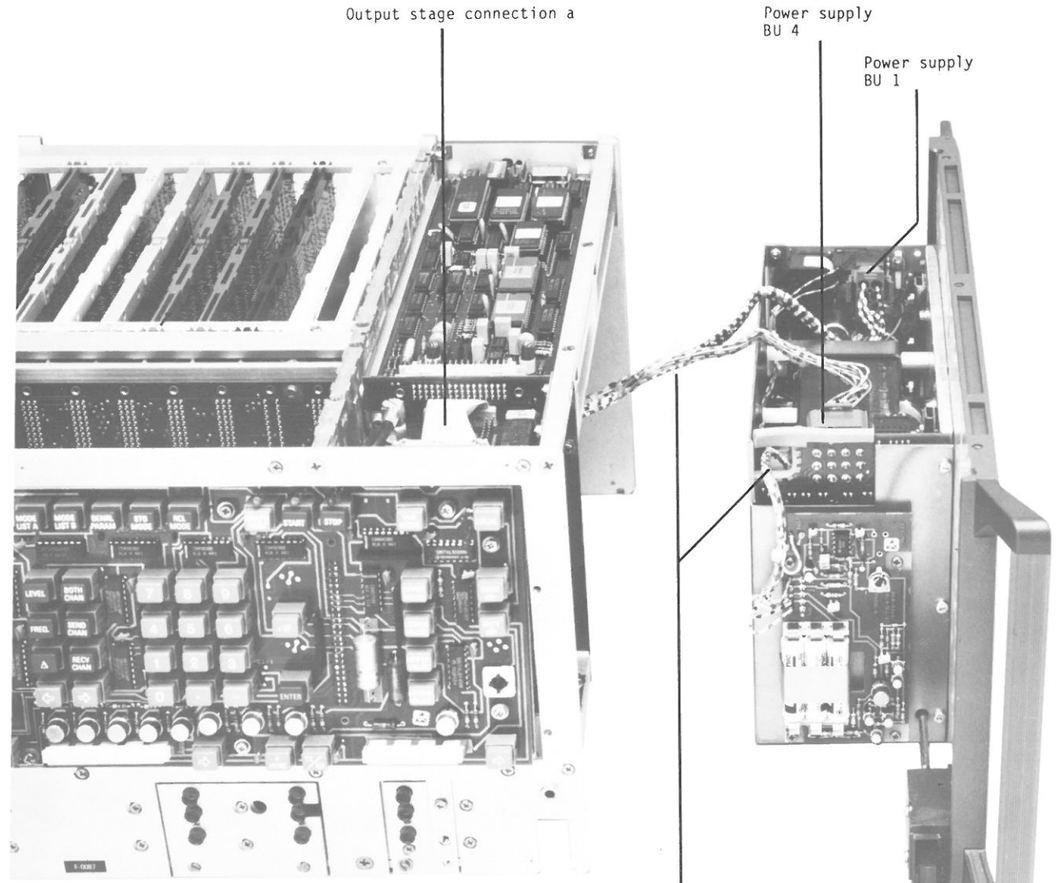


Fig. 10.4-3 Installation of assemblies



NOTE:
When installing the power supply unit, remove analog generator 1 and 2 modules and slide the cable harness under the guard strip without fail. Then re-install analog generator 1 and 2.

Fig. 10.4-4 Installation of assemblies

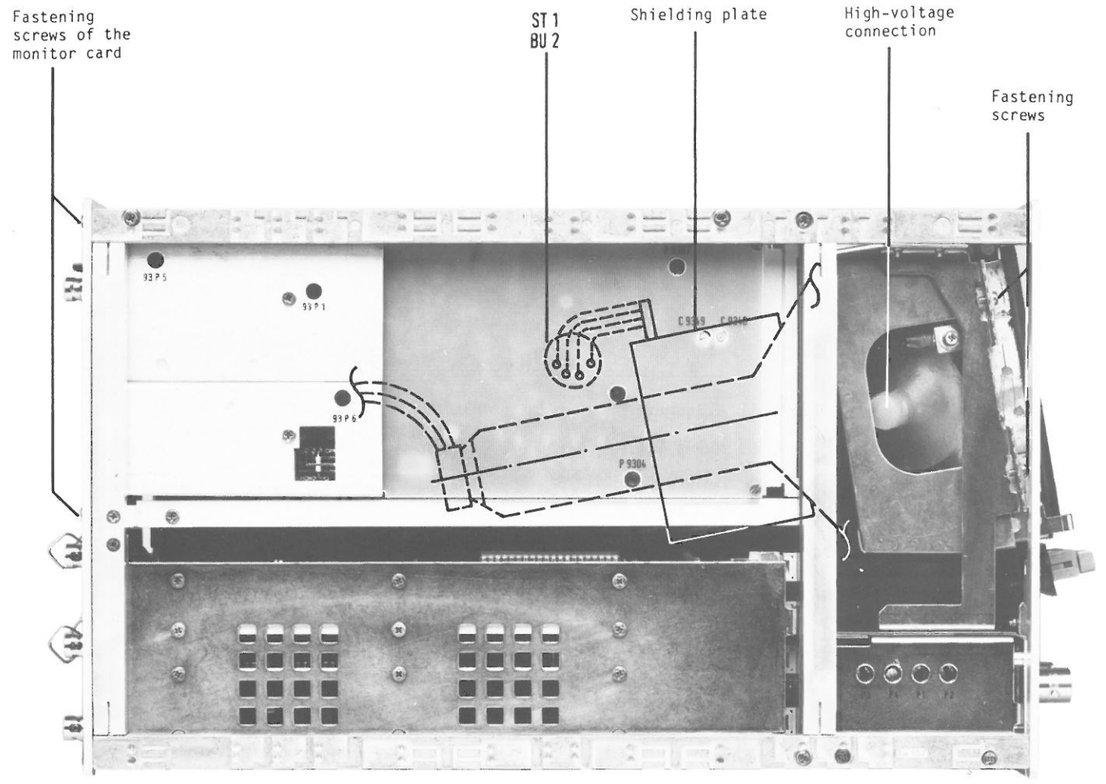


Fig. 10.4-5 Installation of the monitor

[CLR RSLT] and MAINS ON simultaneously

yes — 1 x short BEEP — no

yes

no error OK	all LEDs on

no

TEST coupling board 2 error in ...

clock generator on coupling board faulty:	clock data bus, CE flip-flop on coupling board 2 faulty	coupling board 2 not fitted
LEDs in undefiniert status	after 6 s cont. BEEP LEDs in undefined status	continous BEEP LEDs in undefined status

no further action

CPU-I, error in ...

ROM	RAM	I/O	AMD	IEC
BEEP HIGH LOW LOW 5 s pause BEEP HIGH LOW LOW	BEEP LOW LOW LOW 5 s pause BEEP LOW LOW LOW	BEEP LOW LOW HIGH 5 s pause LOW LOW HIGH	BEEP HIGH LOW HIGH 5 s pause HIGH HIGH HIGH	BEEP HIGH HIGH HIGH 5 s pause LOW LOW HIGH

no further action

no error OK

TEST coupling board 1 * transmission
CPU-I ⟷ CPU-II
CPU-I ⟷ CPU-III

CPU-II does not drive its SSOD line	CPU-III does not drive its SSOD line	no transmission CPU-I/CPU-II	no transmission CPU-I/CPU-III
4 x BEEP "long"	4 x BEEP "short"	2 x BEEP "long"	2 x BEEP "short"

no further action — no further action

* the audible error signals may occur singly or combined!

No fault OK

a) RAM/ROM test of CPU-II
b) RAM/ROM test of coupling card 1
c) Test of SCC

Fault at a)

8085		
2 x beep "short" 2 x beep "long"		
ROM Ø	ROM 1,2,3,4 RAM 1,2,3 Arith.proc.	RAM Ø
4 x beep "long" All LEDs ON	LED "LOCAL" flashes	2 x beep "long" All LEDs ON

Fault at b)

RAM ROM 1,3	ROM 2
4 x beep "long" All LEDs ON	LED "REMOTE" flashes

Fault at c)

LEDs "LOCAL" and "REMOTE" flash

No further reaction

d) RAM/ROM test, CPU-III (meas. run)
e) RAM/ROM test, evaluation processor

no error OK

CPU-2/1 (MASTER) RAM-ROM O.K.
CPU-2/2 (DISPLAY) RAM-ROM O.K.
CPU-2/3 (MEAS.FLOW.) RAM-ROM O.K.
EVAL.-CIRCUIT RAM-ROM O.K.

error in d)

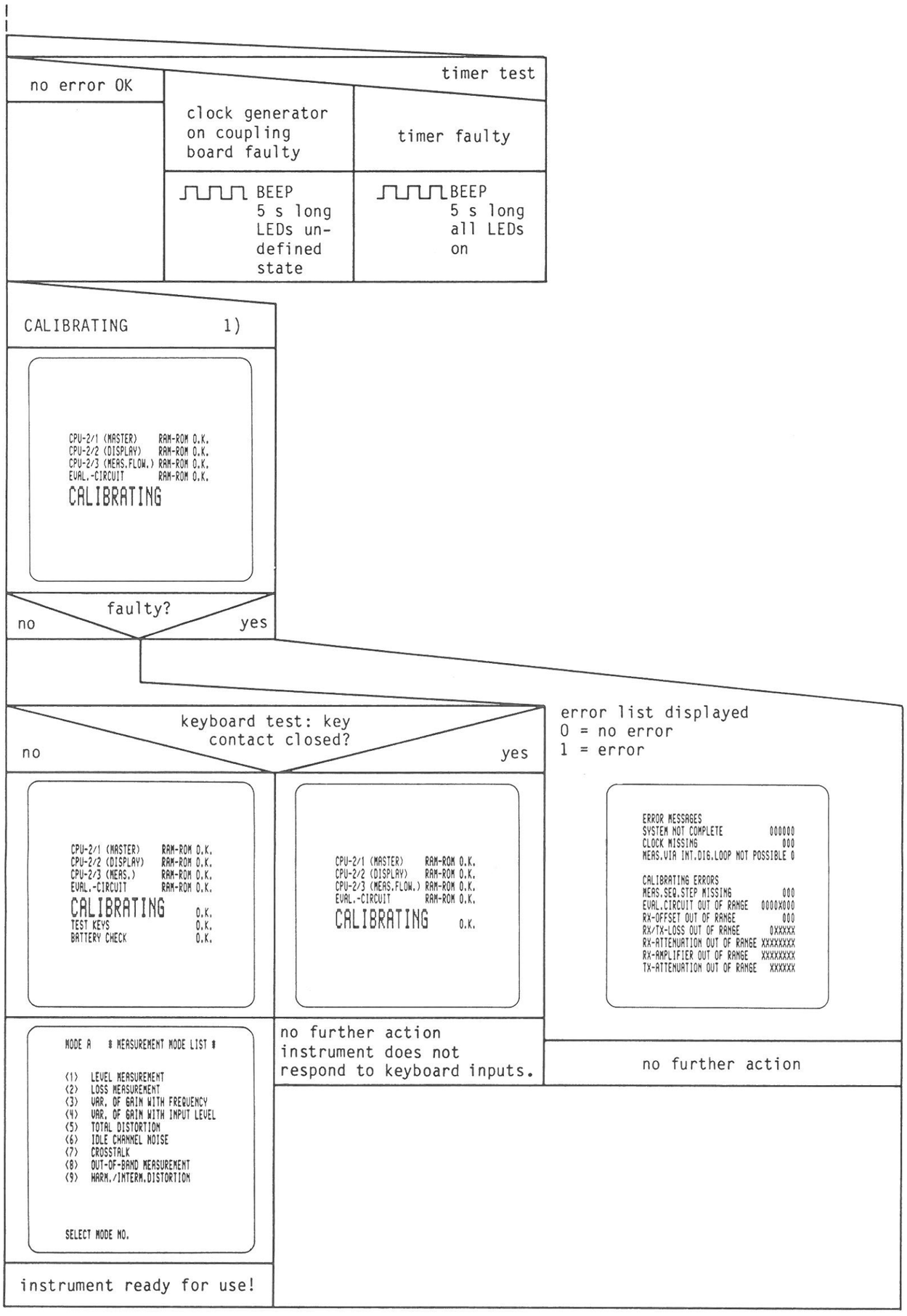
CPU-2/1 (MASTER) RAM-ROM O.K.
CPU-2/2 (DISPLAY) RAM-ROM O.K.

error in e)

CPU-2/1 (MASTER) RAM-ROM O.K.
CPU-2/2 (DISPLAY) RAM-ROM O.K.
CPU-2/3 (MEAS.FLOW.) RAM-ROM O.K.

no further action

((continued overleaf))



1) It is possible to operate the instrument under limited conditions by omitting the calibration sequence. This is done by pressing /9/ when switching the instrument on, the effect being that:
   - the instrument does not self-calibrate,
   - the error list is not displayed,
   - standard values are entered in place of the values which would normally result from calibration, and
   - the results may differ from the nominal values.

Fig. 10.5-1 Structural diagram of troubleshooting

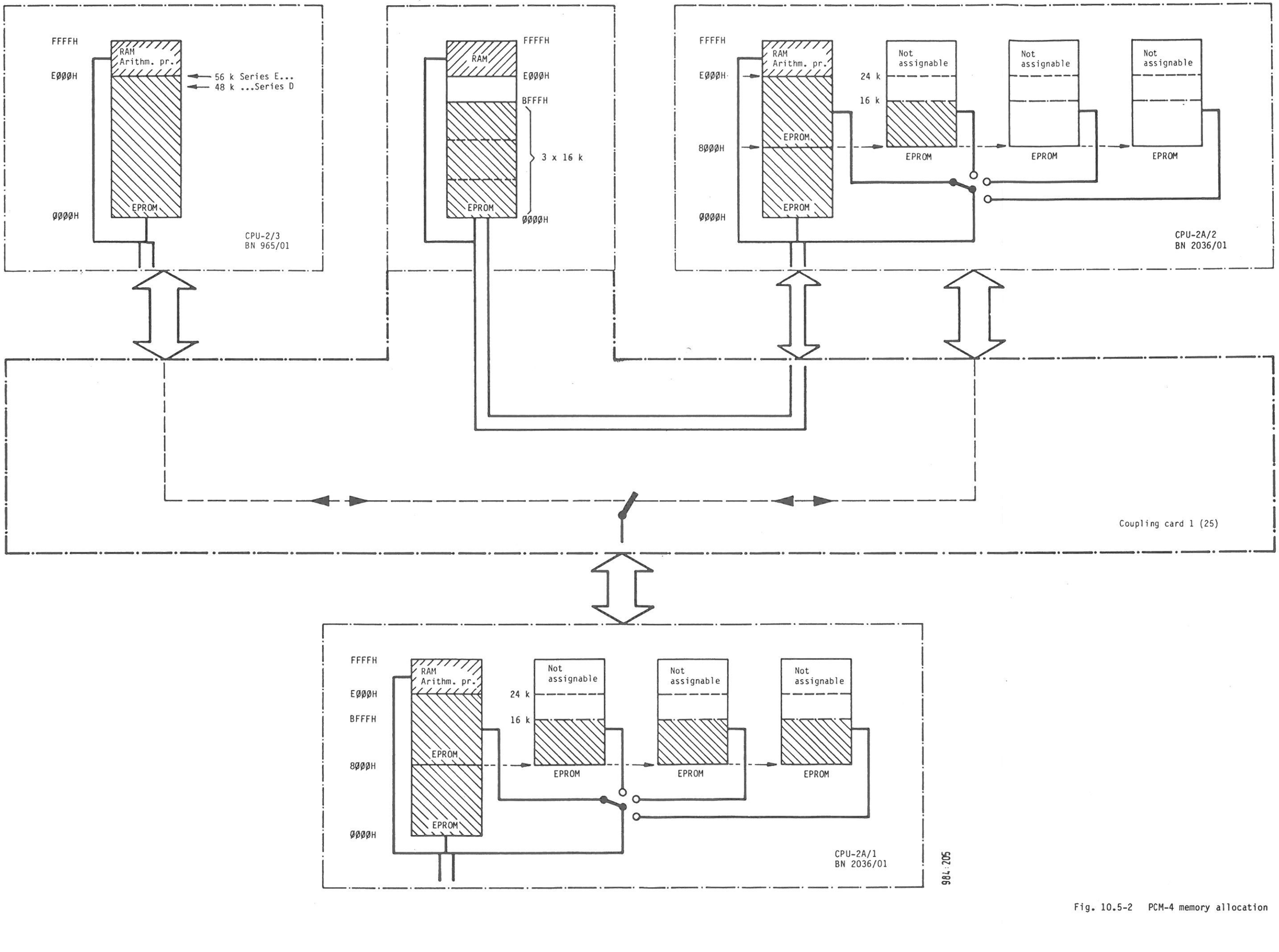


Fig. 10.5-2 PCM-4 memory allocation

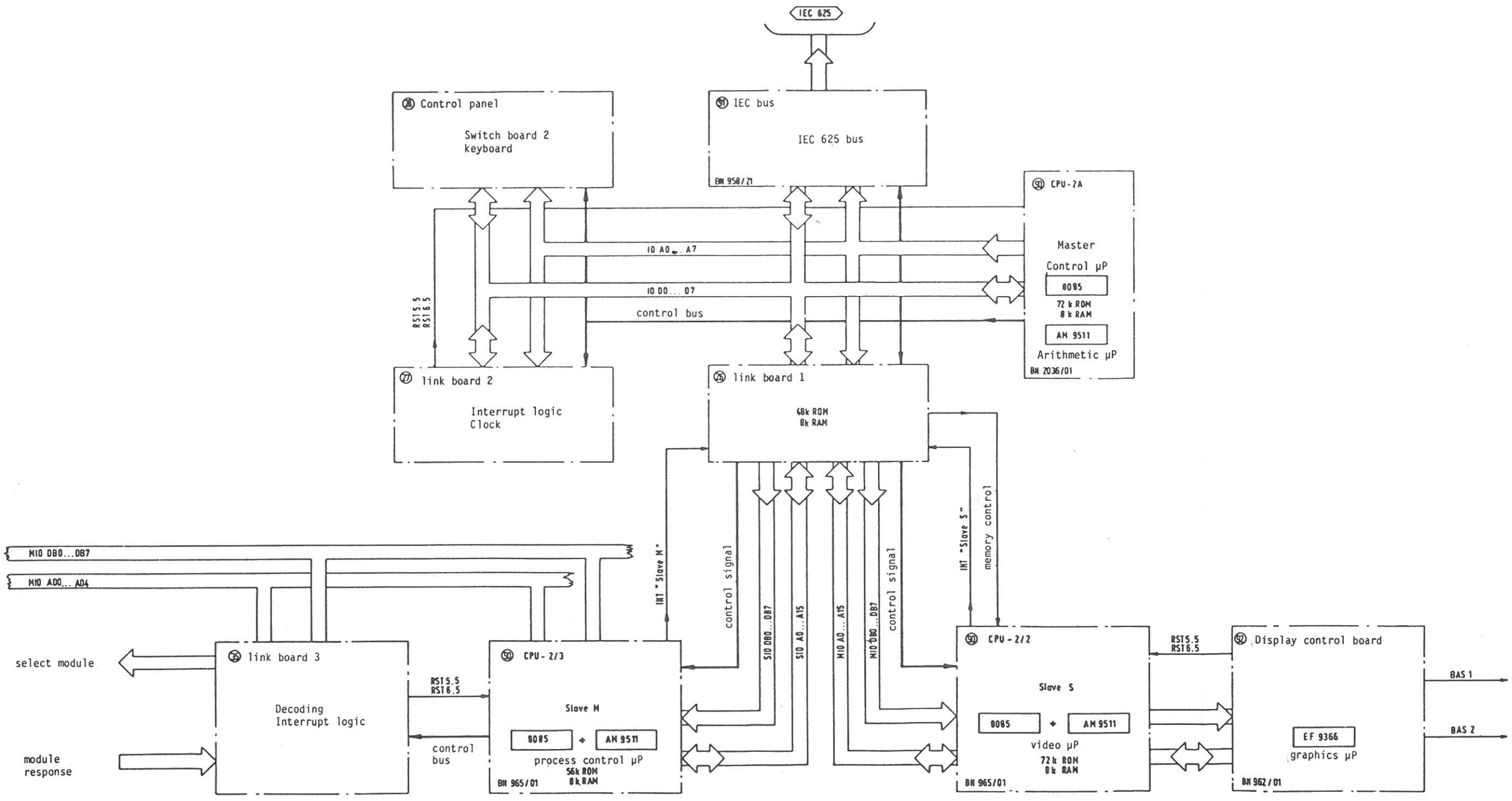


Fig. 10.6-1 Block circuit diagram of CPUs

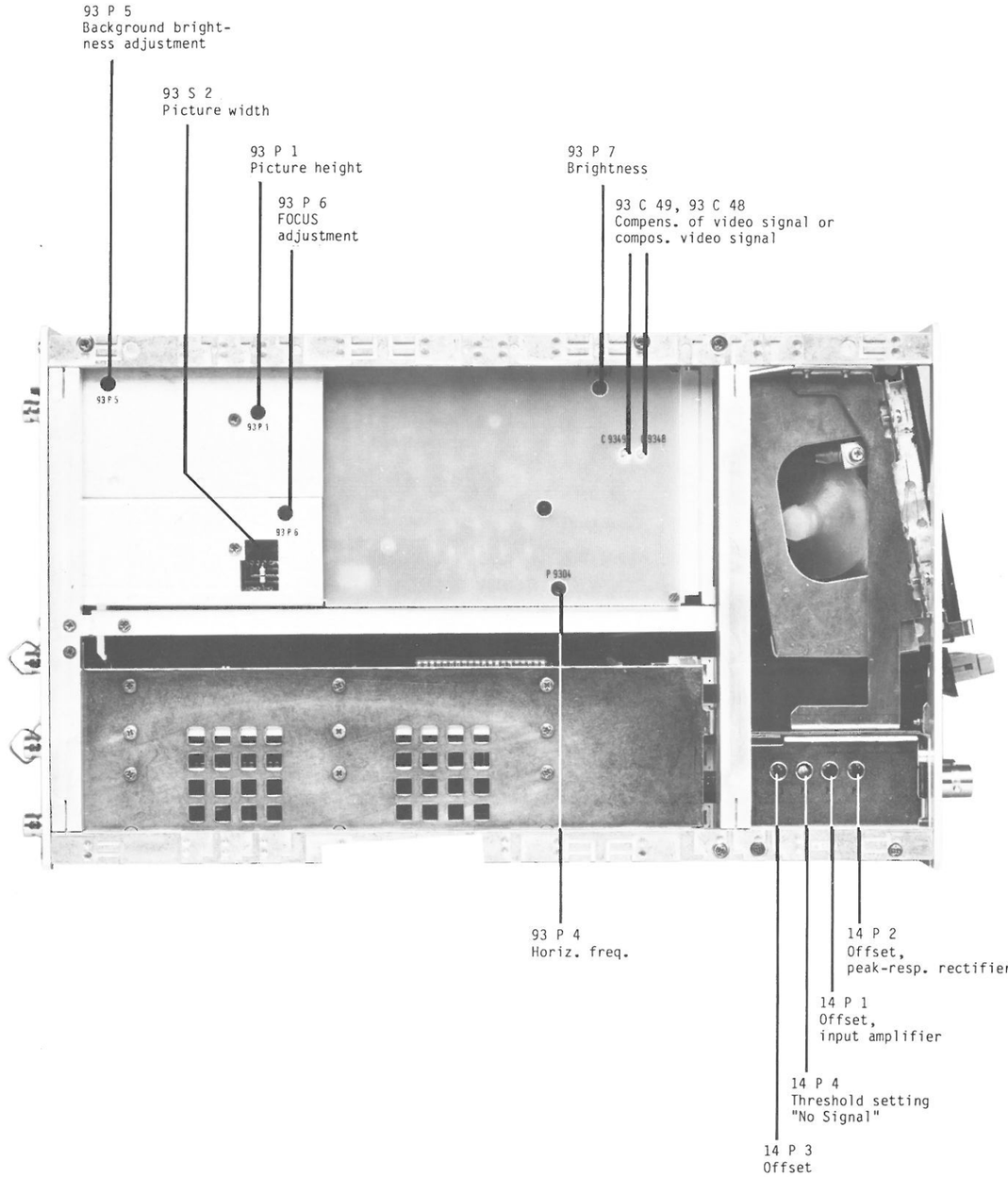


Fig. 10.7-1 Location of alignment elements

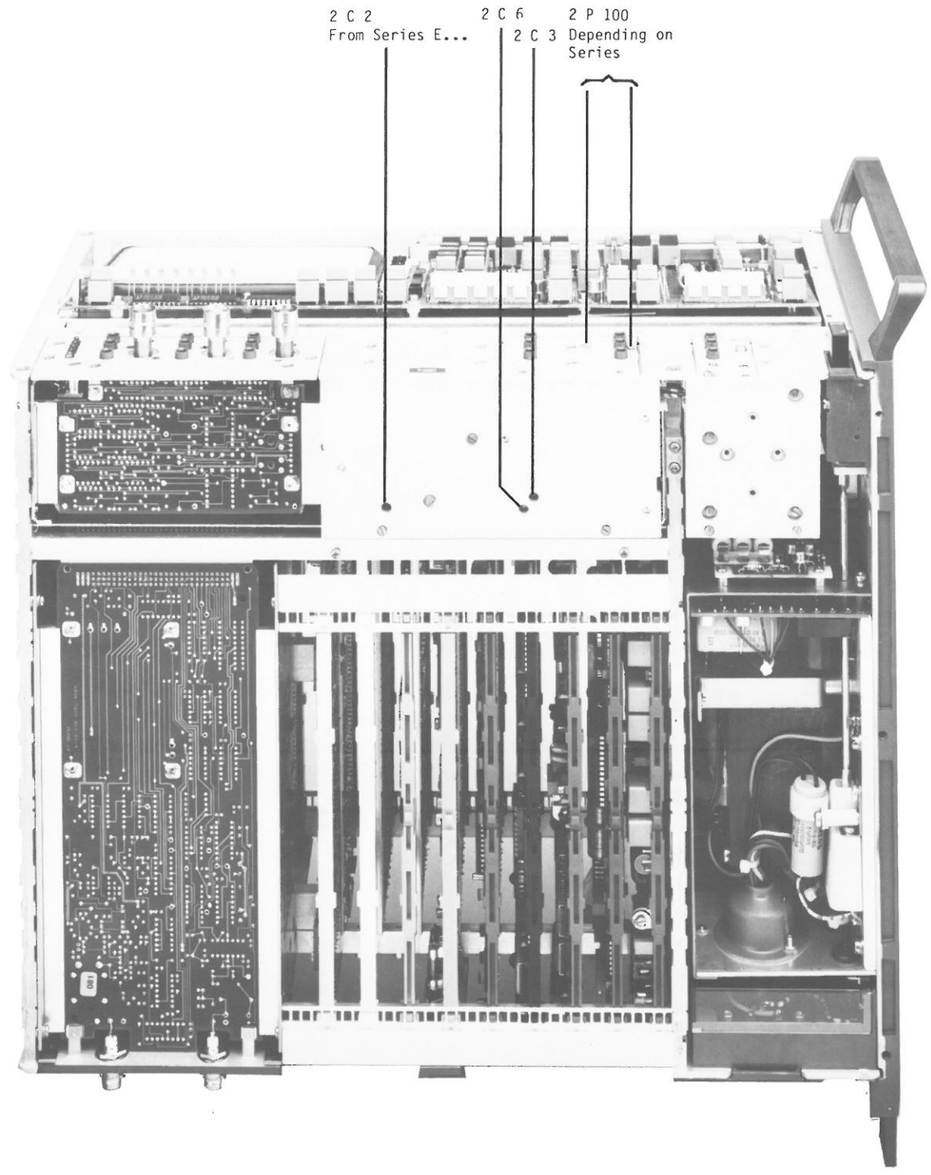


Fig. 10.7-2 Location of alignment elements

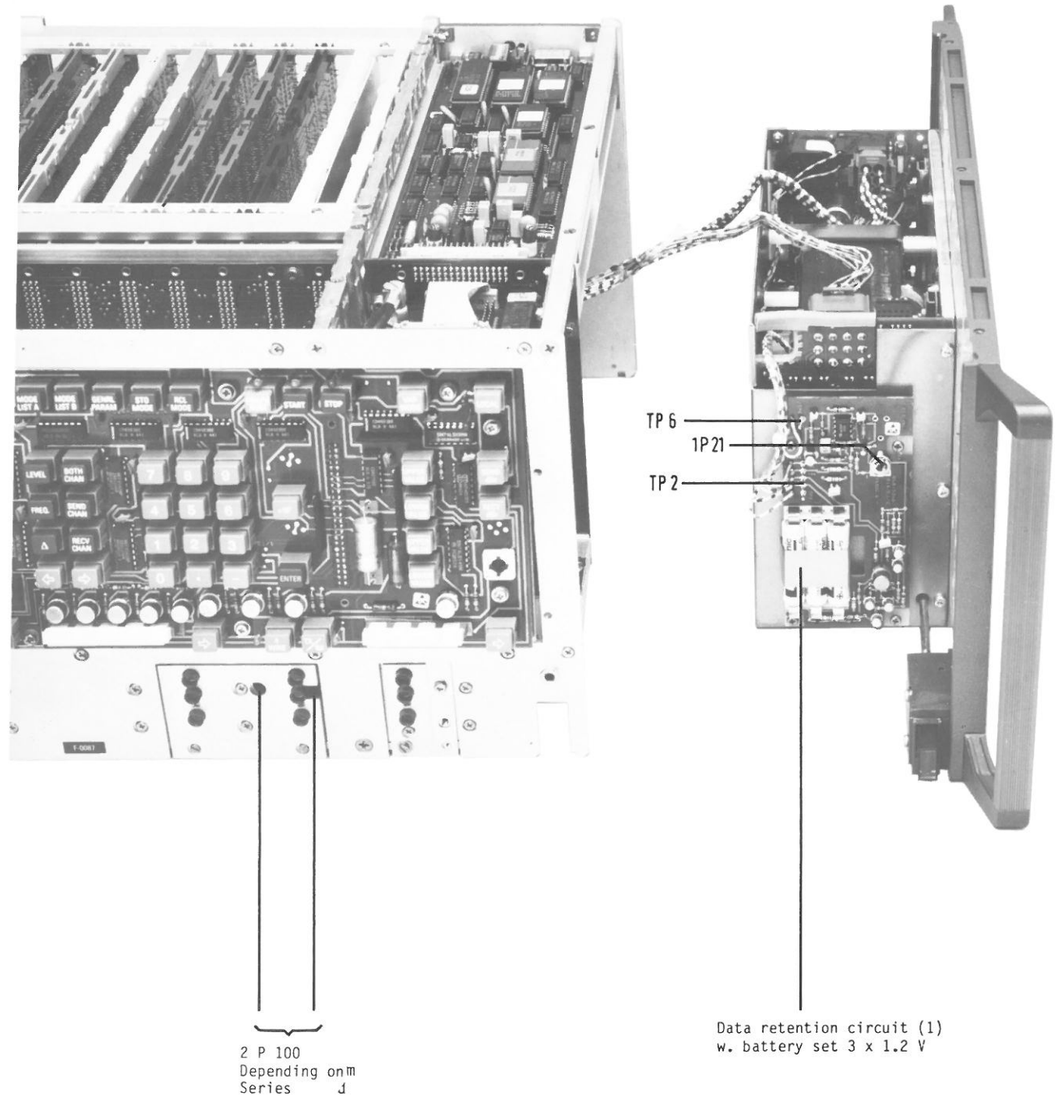


Fig. 10.7-3 Location of aligment elements and back-up batteries