
Service Guide

Hewlett-Packard
16550A

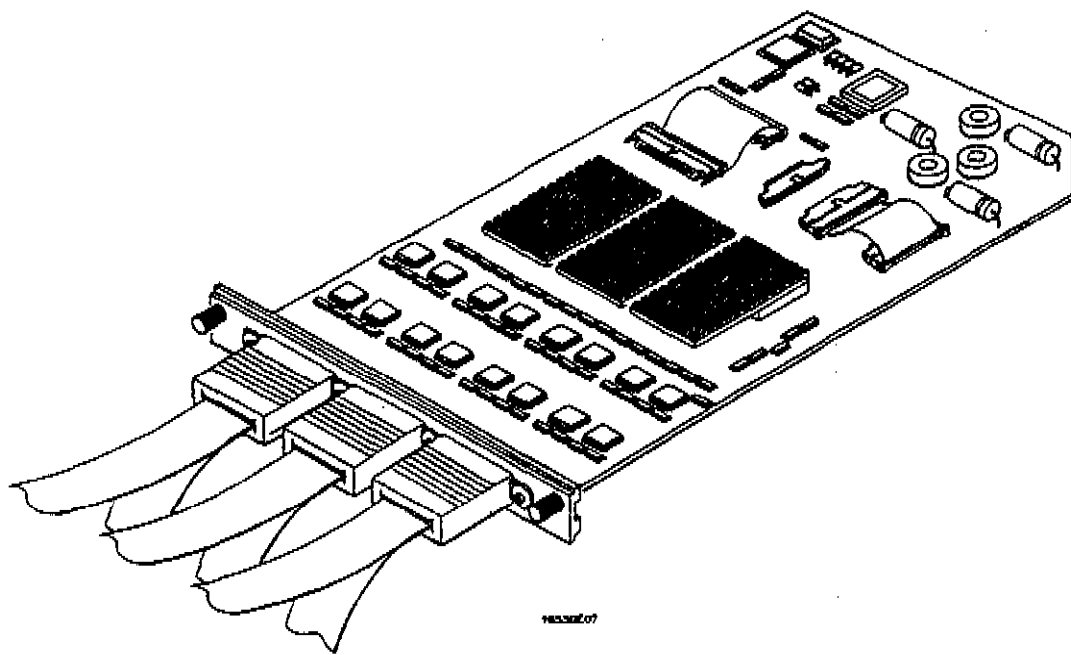
Publication number 16550-90901
First edition, April 1992



**HP 16550A
100-MHz State/500-MHz Timing
Logic Analyzer**

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The HP 16550A 100-MHz State/500-MHz Timing Logic Analyzer

Specifications

The specifications are the performance standards against which the product is tested.

Maximum State Speed	100 MHz
Minimum State Clock Pulse Width*	3.5 ns
Minimum Master to Master Clock Time*	10.0 ns
Minimum Glitch Width	3.5 ns
Threshold Accuracy	$\pm (100 \text{ mV} + 3\% \text{ of threshold setting})$
Setup/Hold Time:*	
Single Clock, Single Edge	0.0/3.5 ns through 3.5/0.0 ns, adjustable in 500-ps increments
Single Clock, Multiple Edges	0.0/4.0 ns through 4.0/0.0 ns, adjustable in 500-ps increments
Multiple Clocks, Multiple Edges	0.0/4.5 ns through 4.5/0.0 ns, adjustable in 500-ps increments

* Specified for an input signal $V_H = -0.9 \text{ V}$, $V_L = -1.7 \text{ V}$, slew rate = 1 V/ns , and threshold = -1.3 V .