Service Guide

Hewlett-Packard
16550A

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HP 16550A
100-MHz State/500-MHz Timing Logic Analyzer

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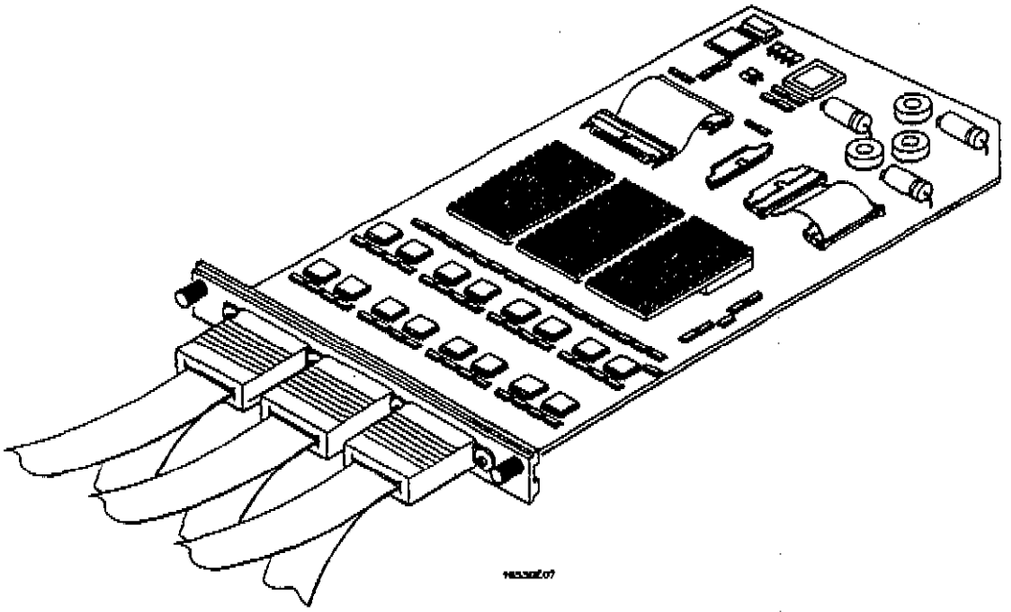

The HP 16550A 100-MHz State/500-MHz Timing Logic Analyzer

Specifications

The specifications are the performance standards against which the product is tested.

Maximum State Speed	100 MHz
Minimum State Clock Pulse Width*	3.5 ns
Minimum Master to Master Clock Time*	10.0 ns
Minimum Glitch Width	3.5 ns
Threshold Accuracy	± (100 mV + 3% of threshold setting)
Setup/Hold Time:*	
Single Clock, Single Edge	0.0/3.5 ns through 3.5/0.0 ns, adjustable in 500-ps increments
Single Clock, Multiple Edges	0.0/4.0 ns through 4.0/0.0 ns, adjustable in 500-ps increments
Multiple Clocks, Multiple Edges	0.0/4.5 ns through 4.5/0.0 ns, adjustable in 500-ps increments

* Specified for an input signal VH = −0.9 V, VL = −1.7 V, slew rate = 1 V/ns, and threshold = −1.3 V.