Using Agilent SPECS

Agilent E3185B PDQ-WLR™ Software
Agilent PDQ-WLR™ revision 2.01

Agilent Technologies

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Edition 2

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In This Manual

This manual provides information on how to use the Agilent SPECS software to execute a PDQ-WLR test. The SPECS program performs the test using the Agilent PDQ-WLR as an algorithm library.

This manual consists of the following chapters.

Chapter 1 will quickly familiarize you with the SPECS software and show you how to perform a PDQ-WLR test. Chapter 2 through 5 provide more detailed information.

1. Getting Started

   Explains how to execute a PDQ-WLR test using the SPECS software, the plug framework, and test plan provided with the PDQ-WLR software.

2. Creating Your Test Environment

   Provides the information required to create and modify your framework and test plan for the SPECS.

3. Executing a PDQ-WLR Test

   Provides information on how to execute a PDQ-WLR test using the SPECS.

4. PDQWLR_PLG Plug Framework

   A description of the plug framework furnished with the PDQ-WLR software.

5. PDQWLR_TPT Sample Test Plan

   A description of the sample test plan furnished with the PDQ-WLR software.

NOTE

About the PDQ-WLR Algorithms and Test Result Analysis

This manual does not provide detailed information on the PDQ-WLR algorithms or on the installation procedure for the PDQ-WLR software. For this information, refer to the *“Agilent PDQ-WLR User’s Guide”*. For information on analyzing the test result data, refer to the *“Agilent PDQ-AT User’s Guide”*.

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1 Getting Started

This chapter explains how to execute a PDQ-WLR test using the Agilent SPECS software, the plug framework and the sample test plan provided with Agilent PDQ-WLR software. This chapter covers the following topics:

- "PDQ-WLR Test Using SPECS"
- "To Create Your Framework"
- "To Create Your Test Plan"
- "To Execute PDQ-WLR Test"

This guide will quickly familiarize you with the SPECS software and show you how to run a PDQ-WLR test.

NOTE

Before Starting PDQ-WLR Test

Before starting the test, you need to install the PDQ-WLR software. Refer to the *"Agilent PDQ-WLR User's Guide"* for information on installing the software.

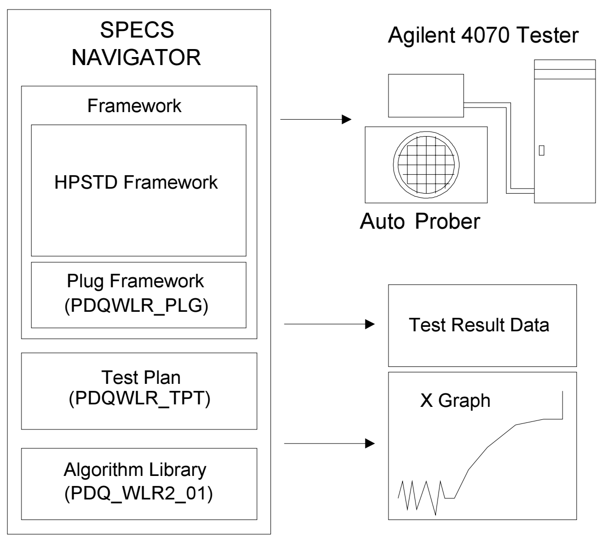
PDQ-WLR Test Using SPECS

The PDQ-WLR software provides a SPECS algorithm library (PDQ_WLR2_01), a plug framework (PDQWLR_PLG), and a sample test plan (PDQWLR_TPT). They are used to perform a PDQ-WLR test using the SPECS.

You can perform the test as shown below:

1. Create your framework by combining the PDQWLR_PLG plug framework and the HPSTD framework.
2. Modify the PDQWLR_TPT test plan as you desire.
3. Execute the test from the SPECS NAVIGATOR window.

After the test, you will obtain the test result data and/or an X-graph.



PDQ_WLR2_01 Algorithm Library

The algorithm library consists of HP BASIC subroutines. It is required to control the tester and to execute the PDQ-WLR test.

For a description of the algorithms included with the PDQ-WLR software, see the *"Agilent PDQ-WLR User's Guide"*.

PDQWLR_PLG Plug Framework

The PDQWLR_PLG plug framework is used to create your framework. You can easily create your framework using the SPECS plug-in function. The plug framework provides operation panels for the following tests (algorithms). The plug framework can be used with other algorithms, however operation panels are not provided.

- ISO_4_EMR algorithm
- TCR_3_EMR algorithm
- JRAMP_3_CAP algorithm
- JTDDB_3_CAP algorithm
- VRAMP_3_CAP algorithm
- VTDDB_3_CAP algorithm
- MBLION_SHS algorithm
- HCI_3_MOS algorithm

For information on creating your framework, see “To Create Your Framework” on page 1-5.

PDQWLR_TPT Sample Test Plan

The PDQWLR_TPT sample test plan is a template. You can create your test plan by modifying the PDQWLR_TPT test plan. The test plan provides test definitions for the algorithms (listed above) covered by the PDQWLR_PLG plug framework and the algorithms listed below:

- KELRES_3_EMR algorithm
- BEM_3_EMR algorithm
- HFCV_3_CAP algorithm

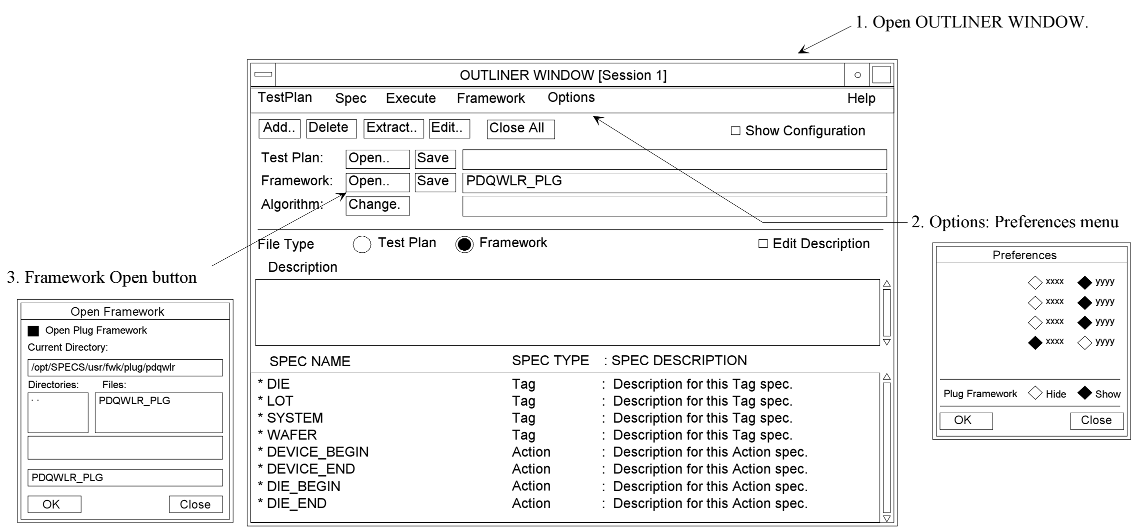
For these three algorithms, the PDQWLR_PLG plug framework does not provide an operation panel for test condition setup. However, without the operation panel, you can execute the algorithm using your framework.

For information on creating your test plan, see “To Create Your Test Plan” on page 1-7.

To Create Your Framework

You can create your framework using the following procedure.

1. Open the SPECS OUTLINER window.
2. Set the OUTLINER so it can open the plug framework. See below:
    a. Select the **Option: Preferences** menu to open the Preferences dialog box.
    b. Set the Plug Framework Hide/Show button to **Show**.
    c. Click **OK**.
3. Open the PDQWLR_PLG plug framework. See below:
    a. Open the Open Framework dialog box by clicking Framework **Open**.
    b. Click **Open Plug Framework** to show the list of plug frameworks in the Files area.
    c. Change the Current Directory to /opt/SPECS/usr/fwk/plug/pdqwlr.
    d. Select PDQWLR_PLG in the Files area.
    e. Click **OK**.



4. Combine the plug framework with the HPSTD framework. See below:

    a. Select the **Framework: Plugin** menu to display the Plugin Framework dialog box.

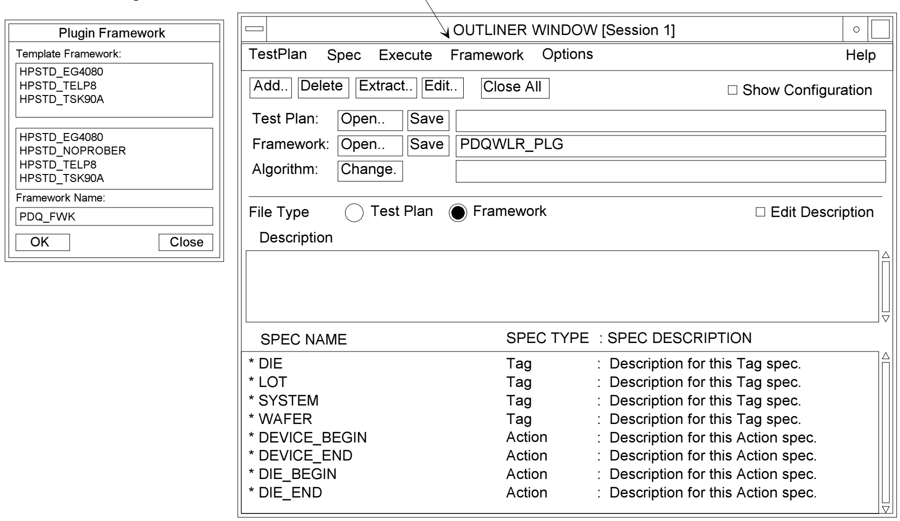
    b. Select an HPSTD framework (HPSTD_EG4080, HPSTD_TELP8, or HPSTD_TSK90A) from the Template Framework area.

    c. Enter the new framework name in the Framework Name field, for example, PDQ_FWK.

    d. Click **OK**.

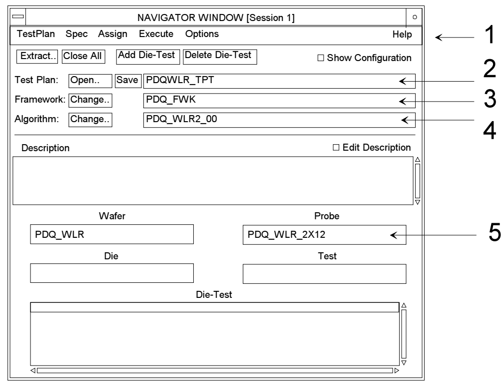
5. Wait until your framework appears in the /opt/SPECS/usr/fwk directory.

4. Framework: Plugin menu



To Create Your Test Plan

You can create your test plan by modifying the PDQWLR_TPT sample test plan as shown below:



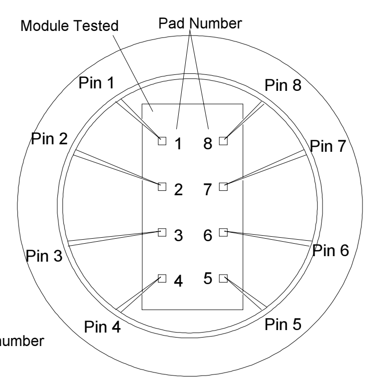
1. Open the SPECS NAVIGATOR window.
2. Click Test Plan **Open**, and select PDQWLR_TPT.
3. Click Framework **Change**, and select your framework, for example, PDQ_FWK.
4. Click Algorithm **Change**, and select PDQ_WLR2_01.
5. Edit the probe specification to define the relationship between the pad number of your test die or module and the matrix pin number of your tester.

   To open the Spec Editor, move the mouse pointer to the Probe field of NAVIGATOR, click the right mouse button, then select **Edit**.

Example of Probe Specification

Spec Editor

Pad Number	Pin Number
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8



Pin N: Matrix Pin number

6. Use the Spec Editor Attribute menu to edit the wafer specification to define the attribute information on the wafer, such as, wafer size, die size, and so on. Use the Spec Editor Body menu to define the dice to be tested, for example, MY_DIE.

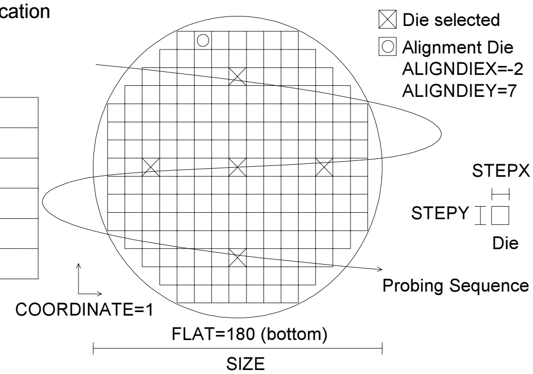
   To open the Spec Editor, move the mouse pointer to the Wafer field of NAVIGATOR, click the right mouse button, then select **Edit**.

   To select the Body or Attribute menu, click **Body** or **Attribute** on the Spec Editor.

Example of Wafer Specification

Spec Editor (Body)

Die Name	X	Y
MY_DIE	0	5
MY_DIE	5	0
MY_DIE	0	0
MY_DIE	-5	0
MY_DIE	0	-5



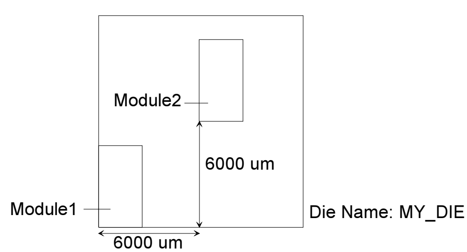
7. Enter the die name in the Die entry field of NAVIGATOR, and press return to open the Spec Editor. Define the new specification.

   The *Die* name is important. Enter the same *Die Name*, for example, MY_DIE, you defined earlier in the wafer specification. For predefined die names, see Table 1-1 on page 1-11.

Example of Die Specification

Spec Editor

Module Name	X[um]	Y[um]
Module1	0	0
Module2	6000	6000



8. Select a test specification, for example, EM_TCR, in Test entry field of NAVIGATOR, and edit the specification as you desire.

   To select the test specification and open the Spec Editor, move the mouse pointer to the Test field of NAVIGATOR, click the right mouse button, then choose **Select**. Choose one of the test specifications in the Select Spec (Test) dialog box.

   For available test specification names, see Table 1-2 on page 1-11.

   For definitions in the test specification that are not used, put a number sign (#) at the beginning of the line as shown in line Module2 of the next example. To add a number sign (#), select the line and click **Comment**. To remove the number sign (#), click **Uncomment**.

   Example of Test Specification: (EM_TCR)

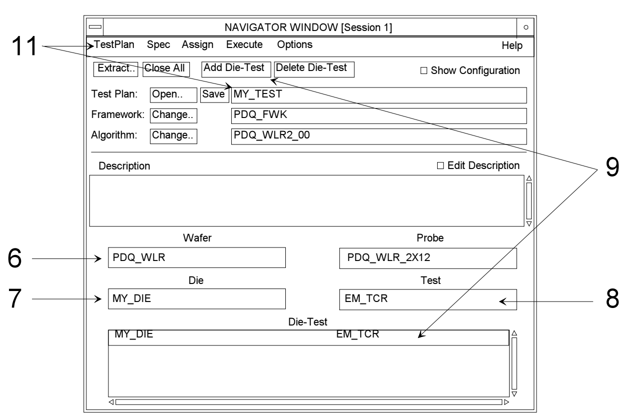
	Molule Name	Device Name	Algorithm	Input	Pad Number	Out	L	C
	Module1		TCR_3_EMR_XL	Soak=	F1=1,F2=2,S1=			
#	Module2		TCR_3_EMR_XL	Soak=	F1=1,F2=2,S1=			

   The *Module Name* is important. Enter the same*Module Name*, for example, Module1 and/or Module2, defined in the die specification.

   Use the Assist dialog box to enter the Input parameters. To open the Assist dialog box, move the mouse pointer to the Input field, click the right mouse button, then select **Assist**.

   In the Assist dialog box, set the actual values but keep the variables. The variables allow you to enter Input values from the operation panel from the run-time framework.

   For the EM_BEM, GOI_HFCV, and EM_KELRES test specifications, enter the actual values. No operation panel is available for these tests.



9. Click **Add Die-Test**. This registers the die and test specifications pair on which a test executes.
10. Repeat steps 7 to 9 for all the test items (algorithms) you want to execute.

    Do not pair a die or test specification which has already been paired in your test plan. To add another pair, you must define a new die specification in step 7, and then select another test specification in step 8.
11. Save the test plan with new name, for example, MY_TEST.

NOTE

To delete unnecessary pairs of Die and Test specifications

When opening the PDQWLR_TPT sample test plan, some pairs are defined in the Die-Test list area. To delete unused pairs, select the pair you want to delete and click **Delete Die-Test**.

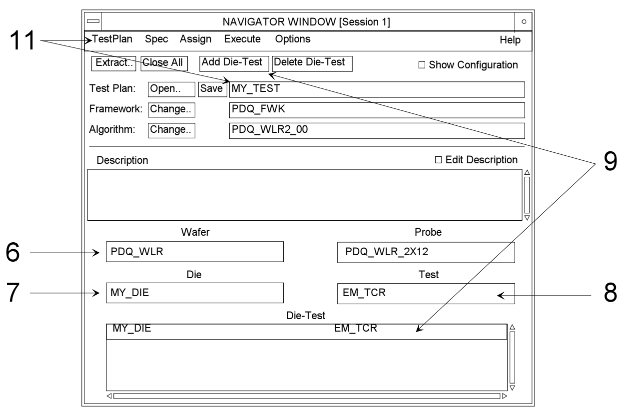


Table 1-1 **Die Names defined in Wafer Specification**

Die Name defined in Wafer Specification	Die Specification (pre-defined)	Test Specification (pre-defined)
EM_TCR	EM_TCR	EM_TCR
EM_ISO	EM_ISO	EM_ISO
EM_KELRES	EM_KELRES	EM_KELRES
GOI_JRAMP	GOI_JRAMP	GOI_JRAMP
GOI_JTDDB	GOI_JTDDB	GOI_JTDDB
GOI_MBLION_SHS	GOI_MBLION_SHS	GOI_MBLION_SHS
GOI_VRAMP	GOI_VRAMP	GOI_VRAMP
GOI_VTDDB	GOI_VTDDB	GOI_VTDDB
MOS_HCI	MOS_HCI	MOS_HCI
	EM_BEM	EM_BEM
	GOI_HFCV	GOI_HFCV

Table 1-2 **Test Specifications and Algorithms**

Test Specification	Algorithm defined in Test Specification	PDQ-WLR Algorithm (original name)
EM_TCR	TCR_3_EMR_XL	TCR_3_EMR
EM_ISO	ISO_4_EMR_XL	ISO_4_EMR
EM_KELRES	KELRES_3_EMR_XL	KELRES_3_EMR
GOI_JRAMP	JRAMP_3_CAP_XL	JRAMP_3_CAP
GOI_JTDDB	JTDDB_3_CAP_XL	JTDDB_3_CAP
GOI_MBLION_SHS	MBLION_SHS_XL	MBLION_SHS
GOI_VRAMP	VRAMP_3_CAP_XL	VRAMP_3_CAP
GOI_VTDDB	VTDDB_3_CAP_XL	VTDDB_3_CAP
MOS_HCI	HCI_3_MOS_XL	HCI_3_MOS
EM_BEM	BEM_3_EMR_X	BEM_3_EMR
GOI_HFCV	HFCV_3_CAP_XL	HFCV_3_CAP

To Execute PDQ-WLR Test

You can run your framework, and execute the PDQ-WLR test as shown below:

1. Launch your framework using the following procedure.

   a. Open the SPECS NAVIGATOR window.

   b. Click Framework **Change**, and select your framework, for example, PDQ_FWK.

   c. Click Test Plan **Open**, and select your test plan, for example, MY_TEST.

   d. Click Algorithm **Change**, and select PDQ_WLR2_01.

   e. Select **Execute:Execute**. The RUN PANEL and OPERATION PANEL are displayed on the screen. See Figure 1-1.

   f. Click **Start** on RUN PANEL to launch the framework. Wait until the Initialize Hardware panel is displayed as shown in Figure 1-1.

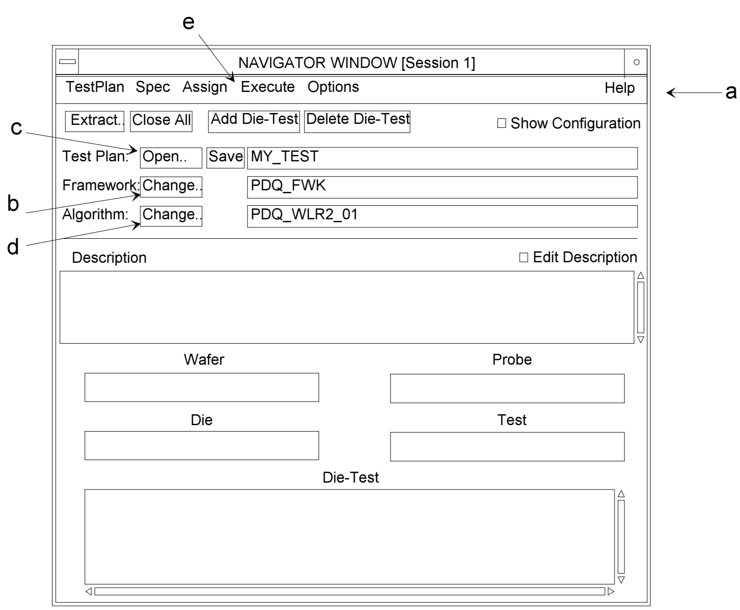
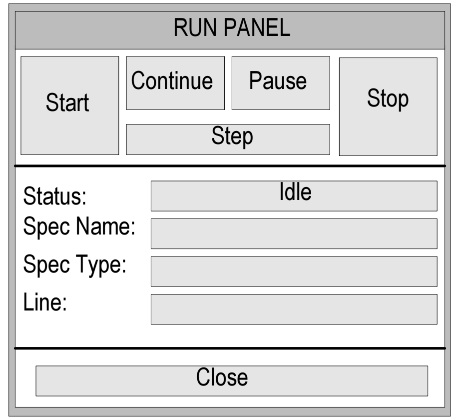
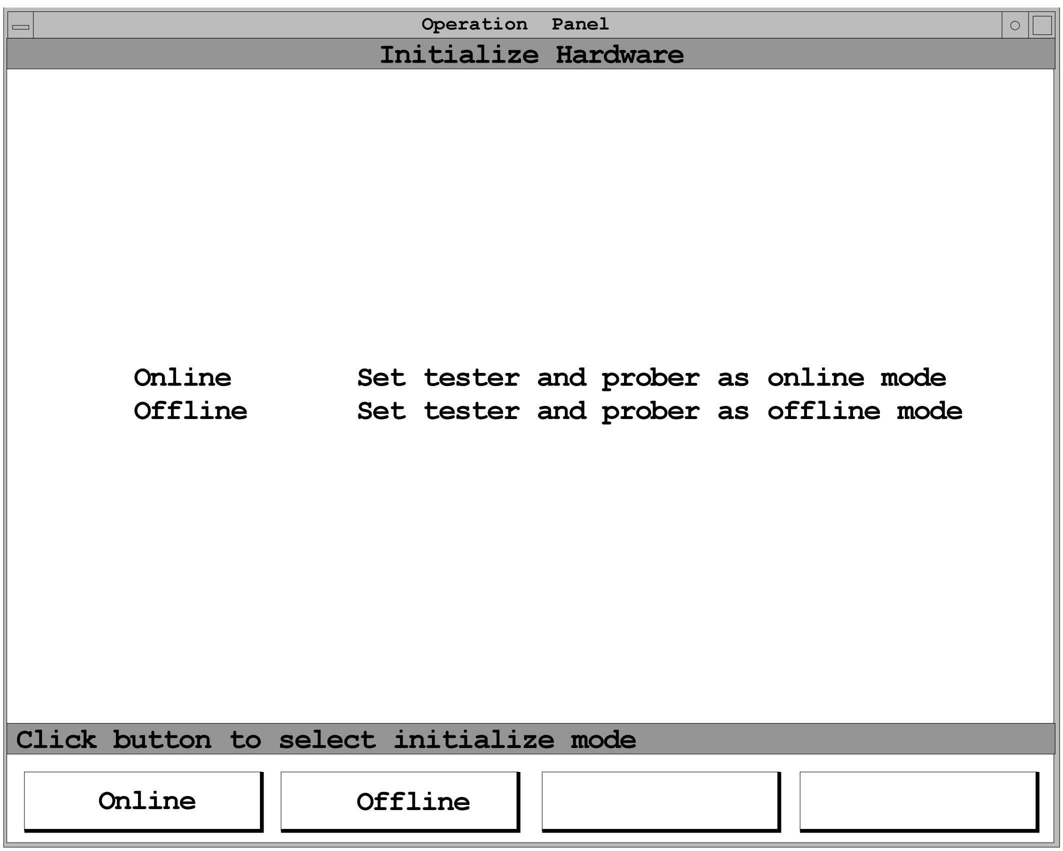


Figure 1-1 Launching the Framework





2. **Initialize Hardware panel**

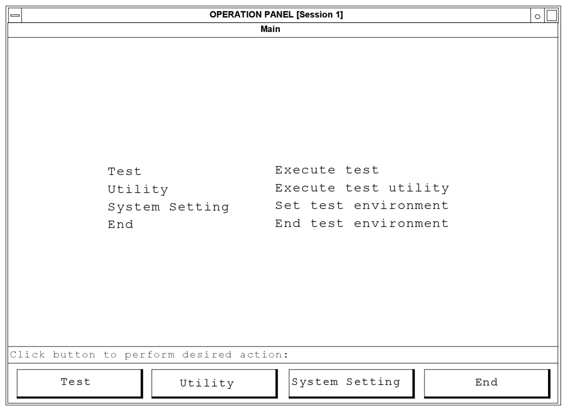
   Click **Online** to select the online execution mode. This executes the hardware initialization.

3. **Hardware Configuration panel**

   Click **Next** after the initialization is completed.

4. **Main panel**

   Click **Test** to continue the test setup.



5. **Register Operator panel**

   Enter your operator name in the Operator Name entry field, then click **Next**.

6. **Set Test Condition panel**

   Enter the lot ID, cassette ID, and process name in the entry fields (optional).

   Ignore the Limit File. It is not available for the PDQ-WLR test.

   Click **Next** to continue the test setup.

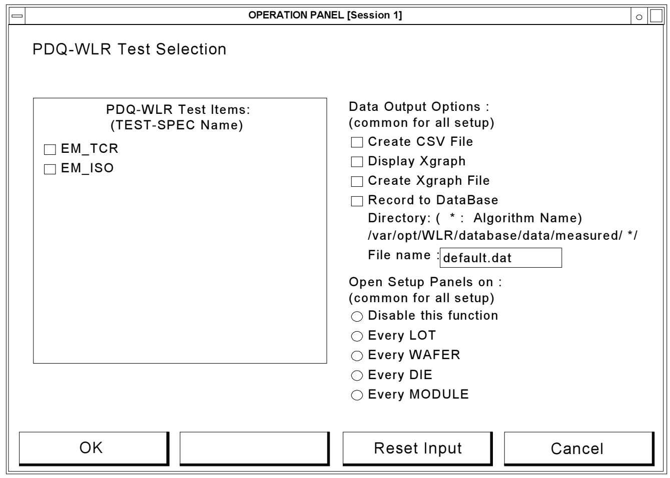
   To return to the Main panel, click **Main Menu**.

7. **Select Wafer panel**

   Select wafer ID, and click **Start Test**.

   To return to the Set Test Condition panel, click **Abort Test**.

8. **PDQ-WLR Test Selection panel (1)**



Set the following as you desire, and then click **OK**.

a. PDQ-WLR Test Items:

Select the test to execute. This area lists all the test specification/die specifications pairs in your test plan. If your test plan, for example, MY_TEST, pairs the EM_TCR and EM_ISO test specifications, the panel will be as shown above.

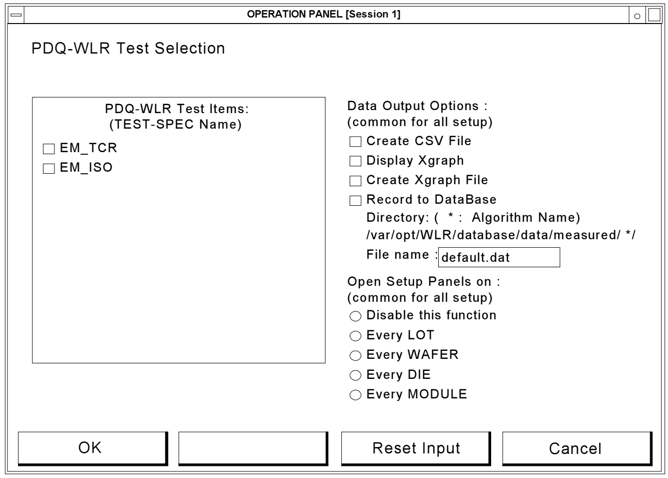
b. Data Output Options and Open Setup Panels on:

Select the options you desire. For selection, see step 9.

To apply the default values to the panel, click **Reset Input**.

To apply the default values to the panel and open the next panel, click **Cancel**.

9. **PDQ-WLR Test Selection panel (2)**



Use this panel to change the PDQ-WLR options explained below:

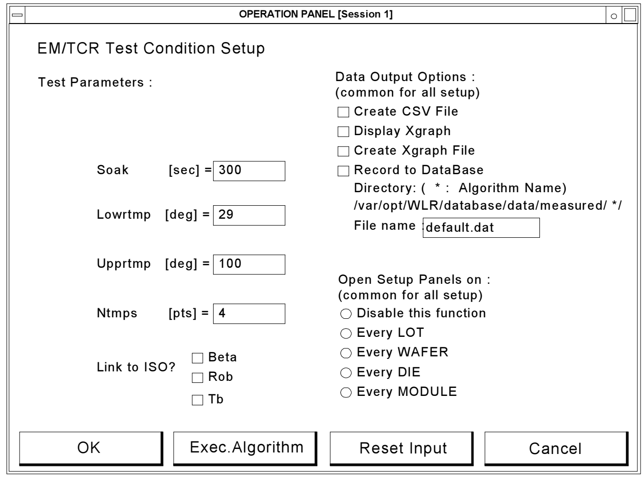
Data Output Options Selects the output data listed below. Multiple selection is available. Initially, Display Xgraph and Record to DataBase are selected. For Database, you can set the name of the test result data file.

- Create CSV File (CSV file is created after test)
- Display Xgraph (Xgraph is displayed after test)
- Create Xgraph File (Xgraph file is created after test)
- Record to Database (.dat file is stored in database)

Open Setup Panels on Selects the panel display option that specifies when the Test Condition Setup panel is displayed.The default is Every LOT.

- Disable this function (the panel is never displayed)
- Every LOT (the panel is opened every lot test)
- Every WAFER (the panel is opened for each wafer test)
- Every DIE (the panel is opened for each die test)
- Every MODULE (the panel is opened for each module test)

10. **(Optional) Test Condition Setup panels**



This panel is displayed if you selected “Every LOT” in the “Open Setup Panels on” in step 9. The panel displays the test you selected in step 8. The figure above shows an operation panel for the EM_TCR test. On the panel, do following:

a. Set the test parameter values to the Test Paramters area.

   For a description of the parameters, see Panel Specifications in Chapter 4.

b. Change the setup of the “Data Output Options” and “Open Setup Panels on”, if desired.

Click **OK** to accept the new test setup and open the next panel.

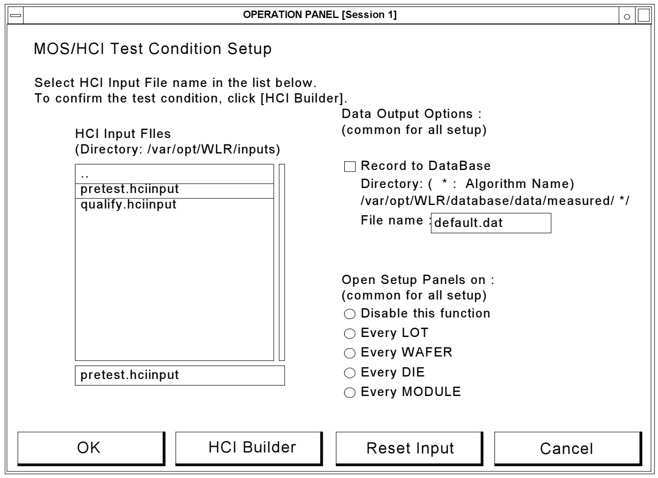
To execute the algorithm now, click **Exec. Algorithm**.

To apply the default values to the panel, click **Reset Input**.

To apply the default values to the panel and open the next panel, click **Cancel**.

If You Execute MOS_HCI Test

If your test plan contains a MOS_HCI test specification, and you selected MOS_HCI on the PDQ-WLR Test Selection panel in step 8, you will see this panel.



On the panel, do the following:

a. Select an HCI input file from the HCI Input Files list.

b. Change the setup of the “Data Output Options” and “Open Setup Panels on”, if desired.

Click **OK** to accept the setup and open the next panel.

To run the HCI builder, click **HCI Builder**.

To apply the default values to the panel, click **Reset Input**.

To apply the default values to the panel and open the next panel, click **Cancel**.

If you want to see, modify, or create the HCI input file, click the HCI Builder button. The HCI builder provides a graphical user interface to create the file. For information on the HCI builder, see the *“Agilent PDQ-WLR User’s Guide”*.

11. **Select Die/Module panel**

    Select the dice and modules to be tested, then click **Next** to start the test.

    To apply the default settings to the panel, click **Undo**.

12. **Execute Test panel**

    This panel is displayed during test execution.

    To immediately stop the test, click **Pause**.

13. **(Optional) PDQ-WLR Test Condition Setup panels**

    During test execution, the panel can be displayed for each wafer test, die test, or module test. The timing of the display depends on the setting in the “Open Setup Panels on” in step 9 and step 10.

14. **Test Result panel**

    This panel is displayed after the test, and shows the test result list.

    To return to the Set Test Condition panel, click **Complete Test**.

    To run the test again, select a wafer from the list, and select **Start Retest**.

2 Creating Your Test Environment

This chapter provides the information required to create or modify the PDQ-WLR test environment using the SPECS, and consists of the following sections:

- “Required Environment”
- “Operation Summary”
- “Plug Framework”
- “Modification Overview”
- “To Create Your Framework”
- “To Create a Test Plan”
- “To Add Operation Panels”

Required Environment

The following environment is required to run PDQ-WLR test using the SPECS.

Platform	HP 9000 Series 700 Model 745 workstation
Operating System	HP-UX 10.20 and HP BASIC/UX 8.02 or later
SPECS	Agilent E3180B revision B.02.41 or later
PDQ-WLR	Agilent E3185B revision A.02.01 or later
PDQ-AT	Agilent E3186A revision A.01.01 or later (for data analysis)
Test System	Agilent 4071A Semiconductor Parametric Tester, Agilent 4072A Advanced Parametric Tester, or Agilent 4062UX Semiconductor Process Control System

NOTE The PDQ-WLR software is required to run the test.

PDQ-WLR Software

The PDQ-WLR software contains the following files for the test using the SPECS:

- **PDQ_WLR2_01 Algorithm Library with Algorithm Core**

  The SPECS algorithm library for PDQ-WLR test and PDQ-WLR algorithm core.

- **PDQWLR_PLG Plug Framework**

  The SPECS plug framework for PDQ-WLR test. This file is used to create your framework. See “To Create Your Framework” on page 2-8. Also see Chapter 4 for details on the file.

- **PDQWLR_TPT Sample Test Plan**

  The SPECS sample test plan for PDQ-WLR test. Use this file to create your test plan. See Chapter 5 for more information on the file.

NOTE For information on installing the PDQ-WLR software, see the *“Agilent PDQ-WLR User’s Guide*”.

Operation Summary

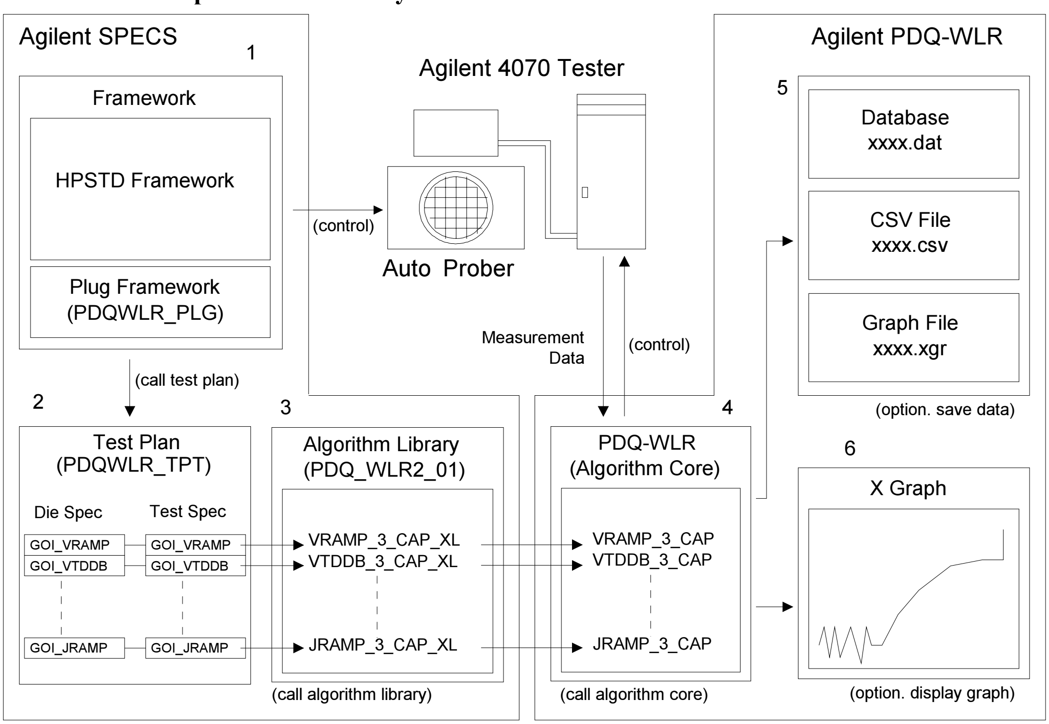
The SPECS performs the PDQ-WLR test as shown in the flowchart below:

1. Framework displays the operation panels and controls the test. Framework also controls the auto prober.
2. The test plan specifies the die tested, selects the algorithm, and defines the test.
3. The Algorithm Library calls the PDQ-WLR algorithm core.
4. The PDQ-WLR algorithm core controls the tester, and executes the measurements.
5. (optional) The algorithms create and save the data files, CSV files, and graph files.
6. (optional) The algorithms display the test result graphs.

NOTE

Steps 5 and 6 depend on the settings of the algorithm input parameter Plot$. For the Plot$ parameters, see the *"Agilent PDQ-WLR User's Guide"*.

Figure 2-1 **Operation Summary**



Output Data

The algorithms can create the following data files for each test. Select the files using the Plot$ parameter.

***.dat file** Test result data file. Use the PDQ-AT software to open the file. The default file name is *default.dat*. The default data directory is /var/opt/WLR/database/data/measured/*alg* where *alg* is the algorithm name.

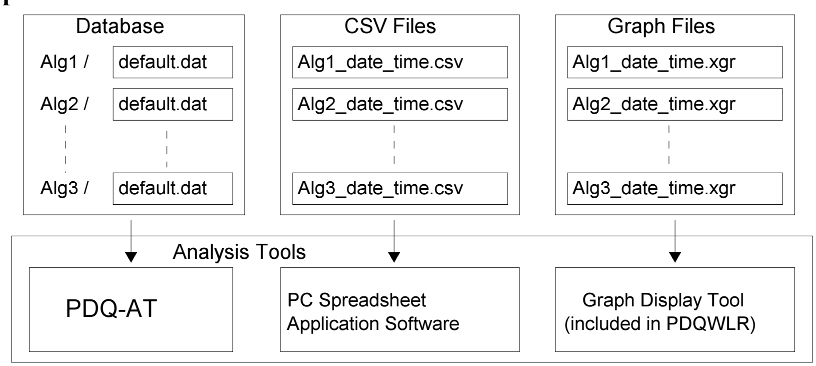
***.csv file** Comma-Separated Value file. Use a PC spreadsheet program to open the file. The file name is *alg_date_time*.csv. The files are stored in the /var/opt/WLR/database/data/csv_files directory.

***.xgr file** HP-UX executable graph file. The file name is *alg_date_time*.xgr. The files are stored in the /var/opt/WLR/database/data/graphs directory.

For *alg_date_time*, *alg* is algorithm name, *date* is yyyy.mm.dd, and *time* is hh.mm.ss. Where, yyyy is the year, mm is the month, dd is the date, hh is the hour, mm is the minute, and ss is the second.

For details on the output data, see the *"Agilent PDQ-WLR User's Guide"*. For data analysis, see the *"Agilent PDQ-AT User's Guide"*.

Figure 2-2 **Output Data Files**



NOTE

SPECS Data File

If the ADTLOGGING parameter of /opt/SPECS/sys/config/sysconf file is TRUE, the SPECS creates a data file (*.adt, *.ad2, or *.ad3 file) after each lot test. If you use the test result data files created by PDQ-WLR algorithms and not the SPECS data file, set ADTLOGGING=FALSE before starting SPECS or delete the unnecessary data file after the PDQ-WLR test.

Plug Framework

The PDQWLR_PLG plug framework is used to create your framework. For information on creating your framework see “To Create Your Framework” on page 2-8. The framework provides two execution environments, PDQ-WLR GUI Enable and GUI Disable.

The default environment is GUI Enable. You can change the environment using the operation panel. See Chapter 3.

See Chapter 4 for a definition of the PDQWLR_PLG plug framework.

PDQ-WLR GUI Enable

This environment provides operation panels for setting the test conditions of the following algorithms. You can use your framework without modification or you can use different algorithms. However, if you want to have operation panels for the additional algorithms, you must modify your framework. See “To Add Operation Panels” on page 2-15.

- ISO_4_EMR algorithm
- TCR_3_EMR algorithm
- JRAMP_3_CAP algorithm
- JTDDB_3_CAP algorithm
- VRAMP_3_CAP algorithm
- VTDDB_3_CAP algorithm
- MBLION_SHS algorithm
- HCI_3_MOS algorithm

PDQ-WLR GUI Disable

This environment does not provide operation panels for PDQ-WLR algorithms. This means you cannot change the test conditions (the setting of the algorithm input parameters) in the run-time framework. The test conditions must be set in a test plan.

Modification Overview

To perform the PDQ-WLR test using the SPECS, use the following procedure.

1. Creating your framework
   a. Combines the plug framework with the HPSTD framework. See “To Create Your Framework” on page 2-8.
   b. (Optional) If you want to add operation panels to change the test conditions in the run-time framework, see “To Add Operation Panels” on page 2-15.
   c. (Optional) You can modify operation panels or functions. See *“Agilent SPECS Creating Your Framework”*.
2. Selecting the framework execution environment (GUI Enable or Disable)

   See Chapter 3.
3. Creating a test plan for the tests you want to run

   See “To Create a Test Plan” on page 2-10 for special instructions on creating a test plan.

NOTE

For details on the plug framework modifications, see *“Agilent SPECS Creating Your Framework”*. Also see Chapter 4 for details on the PDQWLR_PLG plug framework.

NOTE

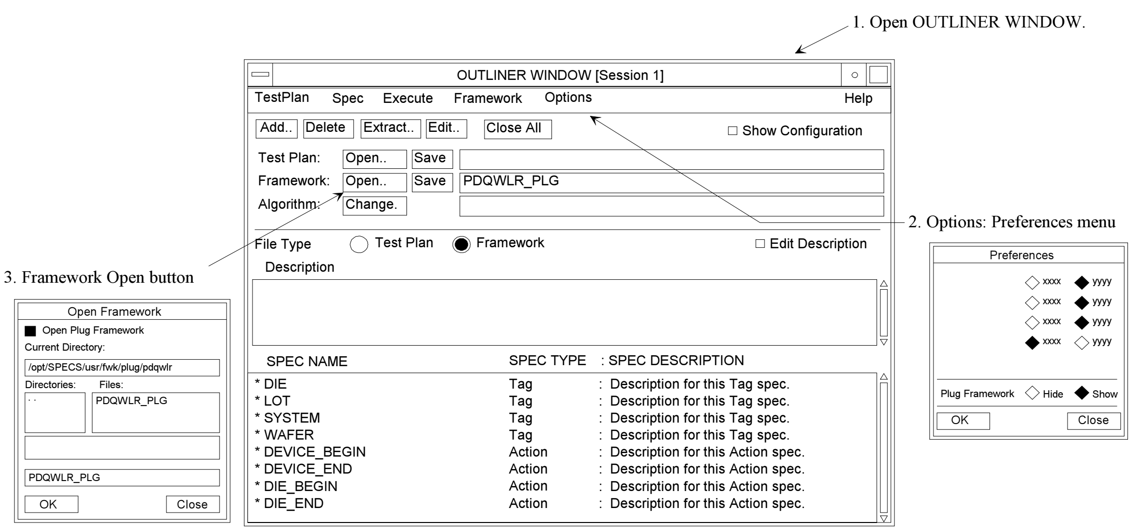
Plug Framework

The plug framework can be combined with the original HPSTD framework. To create your framework, use one of the HPSTD frameworks.

To Create Your Framework

Create your framework for the PDQ-WLR test.

1. Open the SPECS OUTLINER window.
2. Set the OUTLINER so it can open plug framework. See below:
   a. Select the Option: Preferences menu to open the Preferences dialog box.
   b. Set the Plug Framework Hide/Show button to Show.
   c. Click OK.
3. Open the plug framework you want to use in the OUTLINER window.
   a. To open the Open Framework dialog box, click the Framework Open button.
   b. To show the list of plug frameworks in the Files area, click the Open Plug Framework button.
   c. Change the Current Directory to /opt/SPECS/usr/fwk/plug/pdqwlr.
   d. In the Files area, select PDQWLR_PLG.
   e. Click OK.



4. (optional) Add the desired modifications to the plug framework.

   For details on how to modify the plug framework, see *"Agilent SPECS Creating Your Framework"*.

5. (optional) Save the plug framework as a new file.

   a. To open the Save Framework (Plug) dialog box, select the Framework: Save As menu.

   b. Change the Current Directory to /opt/SPECS/usr/fwk/plug/pdqwlr.

   c. Enter a new file name in the Framework Name field, for example, PDQWLR_2.

   d. Click OK.

6. Combine the plug framework with the HPSTD framework.

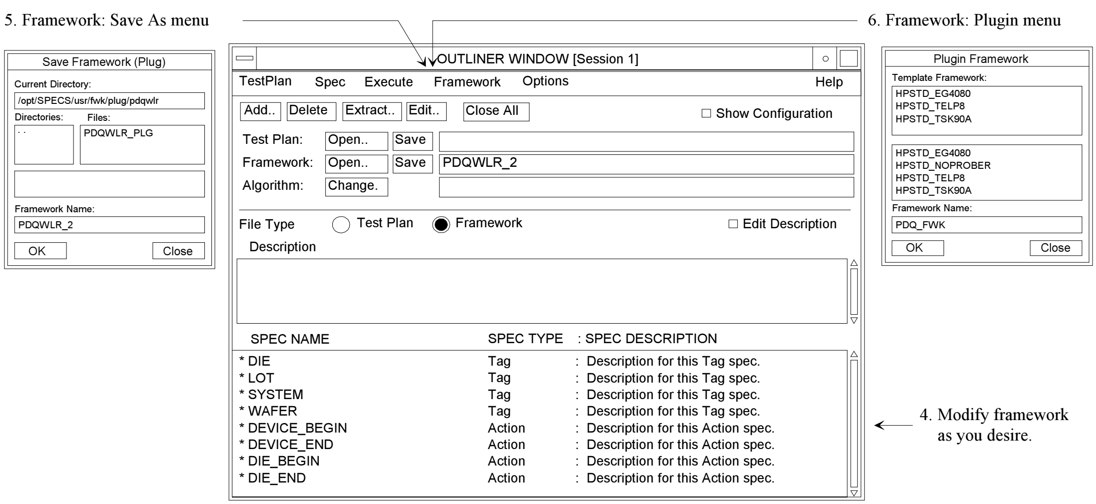
   a. To display the Plugin Framework dialog box, select the Framework: Plugin menu.

   b. From the Template Framework area, select an HPSTD framework, such as HPSTD_EG4080, HPSTD_TELP8, or HPSTD_TSK90A.

   c. Enter a new framework name in the Framework Name field, for example, PDQ_FWK.

   d. Click OK.

7. Wait until your framework is displayed in the /opt/SPECS/usr/fwk directory.



To Create a Test Plan

This section provides the instructions needed to create and the SPECS test plan for PDQ-WLR test.

- "Test Plan for GUI Enable"
- "Test Plan for GUI Disable"

NOTE For further information on creating a test plan, refer to the *"Agilent SPECS User's Guide"*.

Test Plan for GUI Enable

If you use the framework in PDQ-WLR GUI Enable environment, follow these instructions to create a test plan. For defining wafer and probe specifications, you do not need special instructions. For defining die and test specifications, read this section.

Die Specifications

Die specifications must be created for each test specification.

When you define a die and test specification pair in the NAVIGATOR window, do not use a die or test specification which has already been paired in the test plan. The term "paired" means selecting a test specification and a die specification and then clicking the Add Die-Test button in the NAVIGATOR window.

Test Specifications

Test specifications must be created for each algorithm. Only one algorithm can be defined in a test specification. For the algorithms listed in the table below, the name is critical. You must use the test specification names listed below.

For algorithms not listed in the table, you are free to select a name. If you want to have an operation panel for the algorithm, you must modify your framework. See "To Add Operation Panels" on page 2-15.

Test Specification	PDQ-WLR Algorithm	SPECS Algorithm
EM_ISO	ISO_4_EMR	ISO_4_EMR_XL
EM_TCR	TCR_3_EMR	TCR_3_EMR_XL
GOI_JRAMP	JRAMP_3_CAP	JRAMP_3_CAP_XL
GOI_JTDDB	JTDDB_3_CAP	JTDDB_3_CAP_XL
GOI_MBLION_SHS	MBLION_SHS	MBLION_SHS_XL
GOI_VRAMP	VRAMP_3_CAP	VRAMP_3_CAP_XL
GOI_VTDDB	VTDDB_3_CAP	VTDDB_3_CAP_XL
MOS_HCI	HCI_3_MOS	HCI_3_MOS_XL

Algorithm Names

To define PDQ-WLR algorithms in the test specifications, use a special name with an _XL or _X suffix. For example, the TCR_3_EMR algorithm must be defined as TCR_3_EMR_XL in the SPECS. For algorithm names available in the SPECS, see the *“Agilent PDQ-WLR User’s Guide”*. This manual refers to the algorithm by the SPECS translation name.

Input Parameters

Use SYSTEM tag variables to define the input parameters of the algorithms. If you enter actual values instead of SYSTEM tag variables, the values on the operation panels are ignored. The algorithms use these actual values. Before using the variables, confirm which variables are available for the operation panels. Operation panels do not cover all of the input parameters of the algorithms. For the operation panels and the SYSTEM tag variables, see Chapter 4.

Example Test Spec for GUI Enable

The Spec Editor of the test specification uses the following columns to define the specification. This example test specification defines the TCR_3_EMR algorithm. This is the first line defined in the EM_TCR test specification of the PDQWLR_TPT sample test plan.

Molule Name	Device Name	Algorithm	Input	Pad Number	Output	Limit	Comment
MinWidth_A		TCR_3_E	Soak=	F1=1,F2=2,S			

Module Name Name of the module defined in the die specification, for example, MinWidth_AM1.

Device Name Name of the device in the module.

Algorithm Name of the algorithm, for example, TCR_3_EMR_XL.

Input Input parameters of the algorithm.

For example, the input parameters of the TCR_3_EMR_XL algorithm are entered as shown below:

```
V_cool=0.1
Soak=WLR_TCR_Soak
Lowrtmp=WLR_TCR_Lowrtmp
Upprtmp=WLR_TCR_Upprtmp
Ntemps=WLR_TCR_Ntemp
Plot=WLR_TCR_Plot
```

Where, the algorithm input parameters are V_cool, Soak, Lowrtmp, Upprtmp, Ntemps, and Plot. The SYSTEM tag variables are WLR_TCR_Soak, WLR_TCR_Lowrtmp, and so on. The V_cool parameter is not defined in the operation panels of the PDQWLR_PLG plug framework.

Pad Number Pad numbers of the device terminals, for example, F1=1, F2=2, S1=3, S2=4, E1=5, E2=6.

Output (optional) Output parameters of the algorithm.

Limit (optional) Limit value of the output parameter.

Comment (optional) Comment for this line.

Test Plan for GUI Disable

If you use the framework in the PDQ-WLR GUI Disable environment, use the following instructions to create a test plan. For defining the wafer, probe, and die specifications, you do not need special instructions. For defining the test specification, read this section.

Algorithm Names

To define the PDQ-WLR algorithms in the test specifications, use a special name with an _XL or _X suffix. For example, the TCR_3_EMR algorithm must be defined as TCR_3_EMR_XL in the SPECS. For the algorithm names available in the SPECS, see the *"Agilent PDQ-WLR User's Guide"*. This manual refers to the algorithm by the SPECS translation name.

Input Parameters

Enter the actual values used to define the input parameters of the algorithms. These are the values that will be used by the algorithms.

In the GUI Disable environment, the Plot$ input parameter of the PDQ-WLR algorithms is used to select the data files to save and also whether of not Xgraph is displayed. Do not forget to define the Plot$ parameter. In the Spec Editor Assist dialog, this parameter will appear as Plot, not Plot$. For the available values of Plot/Plot$, see the *"Agilent PDQ-WLR User's Guide"*.

Use SYSTEM Tag Variables

The PDQWLR_PLG plug framework defines the following SYSTEM tag variables for the GUI Disable environment. To use the variables, see the *"Agilent PDQ-WLR User's Guide"*.

- Maxro (for ISO_4_EMR algorithm)
- Ntimes (for LIFETIME_MOS algorithm)
- Pa (for LIFETIME_MOS algorithm)
- Times (for HCSTRESS_MOS and LIFETIME_MOS algorithms)

Example Test Spec for GUI Disable

The Spec Editor of the test specification uses the following columns to define the specification. This example defines the TCR_3_EMR algorithm.

Molule Name	Device Name	Algorithm	Input	Pad Number	Output	Limit	Comment
MinWidth_A		TCR_3_E		F1=1,F2=2,S			

Module Name Name of the module defined in the die specification, for example, MinWidth_AM1.

Device Name Name of the device in the module.

Algorithm Name of the algorithm, for example, TCR_3_EMR_XL.

Input Input parameters of the algorithm.

For example, the input parameters of the TCR_3_EMR_XL algorithm are entered as shown below:

```
V_cool=0.1
Soak=300
Lowrtmp=29
Upprtmp=100
Ntemps=4
Plot="B;Y"
```

Where, the algorithm input parameters are V_cool, Soak, Lowrtmp, Upprtmp, Ntemps, and Plot.

Pad Number Pad numbers of the device terminals, for example, F1=1, F2=2, S1=3, S2=4, E1=5, E2=6.

Output (optional) Output parameters of the algorithm.

Limit (optional) Limit value of the output parameter.

Comment (optional) Comment for this line.

To Add Operation Panels

If you want to add operation panels for algorithms, you will need to modify the PDQWLR_PLG plug framework. This procedure shows you how to modify the PDQWLR_PLG plug framework and how to create your framework:

1. Perform steps 1 to 3 described in "To Create Your Framework" on page 2-8.
2. Select the test specification name (*TestSpecName*) for the test algorithm you add. The name (*TestSpecName*) is critical when performing the following steps. For example, EM_SWEAT for the SWEAT_3_EMR algorithm.
3. Open the SYSTEM tag specification, and add the SYSTEM tag variables you need. The variables are used for the input parameters of the algorithm you add. for example, WLR_SWEAT_Ea for the SWEAT_3_EMR algorithm Ea parameter.

   The total number of the SYSTEM tag variables must be 1024 or less.
4. Copy the WLR_TestName panel specification. A new name must be in the format, WLR_*TestSpecName*, for example, WLR_EM_SWEAT.
5. Copy the WLR_TCS_TestName action specification. The new name must be in the format, WLR_TCS_*TestSpecName*, for example, WLR_TCS_EM_SWEAT.
6. Modify the new specifications as shown below. This example is for creating an "Ea [eV]" entry field on the new operation panel.

   a. Open the new panel specification, for example, WLR_EM_SWEAT.
   Add a number sign (#) on the lines VarInput2 to VarInput7 as shown below:

	Widget Name	Widget Type	Parameter	Variable	Range	Message
	PanelTitle	Label	label=WLR_TCS_Title+"Test			
	SelectTitle	Label	label="Test Parameters:",x=10			
	VarInput1	SingleInput	label=WLR_TCS_VarLabel[1]	WLR_TCS_Var[1]		
#	VarInput2	SingleInput	label=WLR_TCS_VarLabel[2]	WLR_TCS_Var[2]		
#	VarInput3	SingleInput	label=WLR_TCS_VarLabel[3]	WLR_TCS_Var[3]		
#	VarInput4	SingleInput	label=WLR_TCS_VarLabel[4]	WLR_TCS_Var[4]		
#	VarInput5	SingleInput	label=WLR_TCS_VarLabel[5]	WLR_TCS_Var[5]		
#	VarInput6	SingleInput	label=WLR_TCS_VarLabel[6]	WLR_TCS_Var[6]		
#	VarInput7	SingleInput	label=WLR_TCS_VarLabel[7]	WLR_TCS_Var[7]		
	AskPlot	ToggleSelect	label="Data Output Options:	WLR_PlotSelecte	WLR_	
	DB_DirPath	Label	label="Directory: (* :Algorith			
	DB_FileName	SingleInput	label="File name: ",x=63,y=4	WLR_DB_FileNa		
	AskTCS	RadioSelect	label="Open Setup Panels on:	WLR_TCS_Select	WLR_	
			label="OK",bgcolor=PNL_B			
	InputConfirm	AcceptKey	label="Exec.Algorithm",pos=			
	OpenAlgPanel	ActionKey	label="Reset Input",pos=3,bg			
	InputReset	ResetKey	label="Cancel",pos=4,bgcolor			
	InputCancel	CancelKey				

b. Open a new action specification, for example, WLR_TCS_EM_SWEAT.
c. Define the panel title in the WLR_TCS_Title, for example, EM/SWEAT.
d. Define the label of the entry field in the WLR_TCS_VarLabel[1], for example, Ea [eV] .
e. Delete the number sign (#) form the beginning of the lines for the WLR_TCS_Var[1].
f. Replace the WLR_TestName_ParmName1 variable with the SYSTEM tag variable added in step 3, for example, WLR_SWEAT_Ea.
g. Specify a new panel specification, for example, WLR_EM_SWEAT for the PANEL commands.
h. Delete the number sign (#) at the beginning of the line for the ACTION command.

Steps c to h modify the new action specifications as shown below.

	Branch Label	Command	Parameter	Comment
	OpenTemplate			
		LET	WLR_TCS_Title=”EM/SWEAT”	See c.
		LET	WLR_TCS_VarLabel[1]=”Ea [eV]”	See d.
		LET	WLR_TCS_VarLabel[2]=”TCS Template Label2”	
		LET	WLR_TCS_VarLabel[3]=”TCS Template Label3”	
		LET	WLR_TCS_VarLabel[4]=”TCS Template Label4”	
		LET	WLR_TCS_VarLabel[5]=”TCS Template Label5”	
		LET	WLR_TCS_VarLabel[6]=”TCS Template Label6”	
		LET	WLR_TCS_VarLabel[7]=”TCS Template Label7”	
		LET	WLR_TCS_Var[1]=WLR_SWEAT_Ea	See e and f.
#		LET	WLR_TCS_Var[2]=WLR_TestName_ParmName2	
#		LET	WLR_TCS_Var[3]=WLR_TestName_ParmName3	
#		LET	WLR_TCS_Var[4]=WLR_TestName_ParmName4	
#		LET	WLR_TCS_Var[5]=WLR_TestName_ParmName5	
#		LET	WLR_TCS_Var[6]=WLR_TestName_ParmName6	
#		LET	WLR_TCS_Var[7]=WLR_TestName_ParmName7	
		IF	WLR_TCS_Swap=1	
		PANEL	“WLR_EM_SWEAT”	See g.
		ELSE		
		PANEL	“WLR_EM_SWEAT”,2	See g.
		PANEL	“WLR_EM_SWEAT”,0	See g.
		END IF		
		LET	WLR_SWEAT_Ea=WLR_TCS_Var[1]	See e and f.
#		LET	WLR_TestName_ParmName2=WLR_TCS_Var[2]	
#		LET	WLR_TestName_ParmName3=WLR_TCS_Var[3]	
#		LET	WLR_TestName_ParmName4=WLR_TCS_Var[4]	
#		LET	WLR_TestName_ParmName5=WLR_TCS_Var[5]	
#		LET	WLR_TestName_ParmName6=WLR_TCS_Var[6]	
#		LET	WLR_TestName_ParmName7=WLR_TCS_Var[7]	
		ACTION	“WLR_CheckPlotOptions”	See h.

7. Copy the WLR_TestName_OpenAlgPanel action specification. A new name must be of the form WLR_*TestSpecName*_OpenAlgPanel, for example, WLR_EM_SWEAT_OpenAlgPanel.

8. Perform steps 5 and 6 described in “To Create Your Framework” on page 2-8.

To Confirm the Operation panel You Added

After performing the procedure described above, you can confirm that the new operation panel is correctly displayed. Perform the following steps. The new panel is displayed after the Copyright panel.

1. Open your framework.
2. Open the PLG_FWK_BEGIN action specification.
3. Delete the two number signs (#) for the Branch Label name: OpenTemplateTCS.
4. Specify the WLR_TCS_*TestName* action specification, for example, WLR_TCS_EM_SWEAT for the ACTION command in the OpenTemplateTCS branch label.

	Branch Label	Command	Parameter	Comment
	OpenTemplateTCS	ACTION	“WLR_TCS_EM_SWEAT”	

5. Close the PLG_FWK_BEGIN action specification, and execute the framework.

NOTE

Do *not* save the framework after making the above modifications. This procedure is to be used only to confirm the accuracy of the display.

To Modify Your Test Plan

After creating your framework, you will need to modify your test plan to add the algorithms for the new operation panel. A modification example is shown below.

1. Open the SPECS NAVIGATOR window.
2. Open the test plan to be modified, for example, the PDQWLR_TPT sample test plan.
3. Edit the probe specification if needed.
4. Edit the wafer specification to define the new die specification to be used.

   Example of Wafer Specification (Body):

Die Name	X	Y	Die Label	Comment
EM_SWEAT	2	2		

5. Enter the new die name, for example, EM_SWEAT in Die entry field of the NAVIGATOR window, and define a new specification.

   Example of Die Specification:

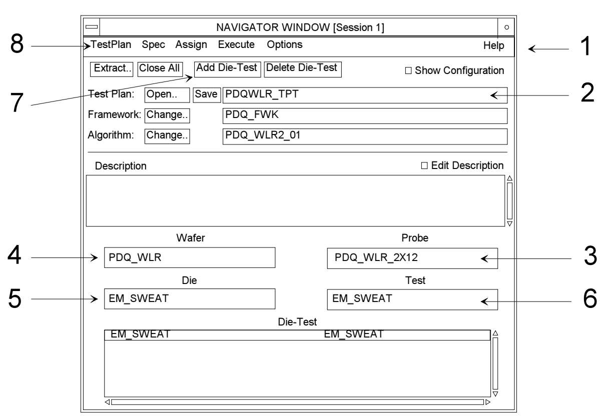
Molule Name	X(um)	Y(um)	Comment
Module_S1	0	0	

6. Enter the new test name, for example, EM_SWEAT in the Test entry field of the NAVIGATOR window, and define a new specification.

   Example of Test Specification:

Molule Name	Device Name	Algorithm	Input	Pad Number	Out	L	C
Module_S1	Device_S1	SWEAT_3_E_XL	Ea=WL	T1=1,T2=2,T3=			

7. Click the Add Die-Test button.
8. Save the test plan with a new name.



3 Executing a PDQ-WLR Test

You can execute the PDQ-WLR test using the framework you created in the procedure described in Chapter 2. The framework has been created by combining the PDQWLR_PLG plug framework with the HPSTD framework. For more details on the HPSTD framework, refer to the *“Agilent SPECS Framework Operation Guide”*. Also see Chapter 4 for more information on the additional operation panels in the PDQWLR_PLG plug framework.

This chapter explains how to execute the PDQ-WLR test, and consists of the following sections:

- “To Launch Your Framework”
- “To Change PDQ-WLR Environment”
- “To Execute PDQ-WLR Test”
- “To Set PDQ-WLR Options”

NOTE

After Executing Test

After the test, you will have the test result data files; CSV files, Xgraph files, and/or database files. For information on the data files, see Chapter 2. See *“Agilent PDQ-AT User’s Guide”* for information on data analysis.

To Launch Your Framework

This section explains how to launch your framework. Your framework can be opened three ways.

- "Using NAVIGATOR"
- "Using OUTLINER"
- "Using the tplexec Command"

Using NAVIGATOR

1. Open the SPECS NAVIGATOR window.
2. Click Framework Change, and select your framework, for example, PDQ_FWK.
3. Click Test Plan Open, and select the test plan to execute, for example, MY_TEST.
4. Click Algorithm Change, and select the algorithm library to use, for example, PDQ_WLR2_01.
5. Select Execute:Execute. The RUN PANEL and OPERATION PANEL are displayed on the screen. See Figure 3-1.
6. Click Start on the RUN PANEL to launch the framework. Figure 3-1 shows an OPERATION PANEL after clicking Start.

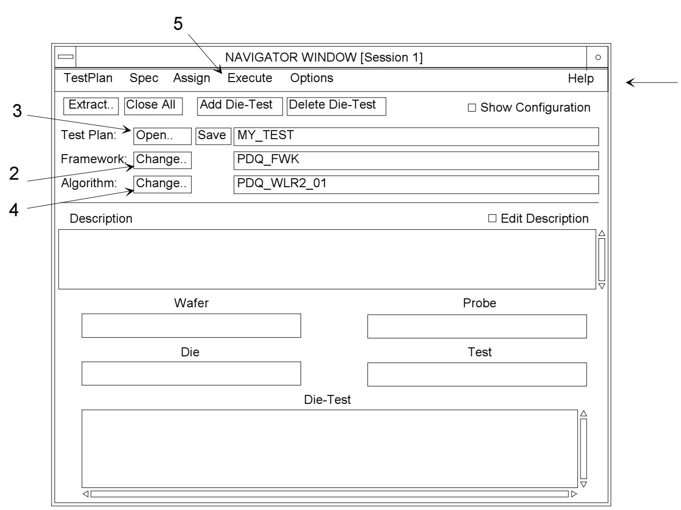
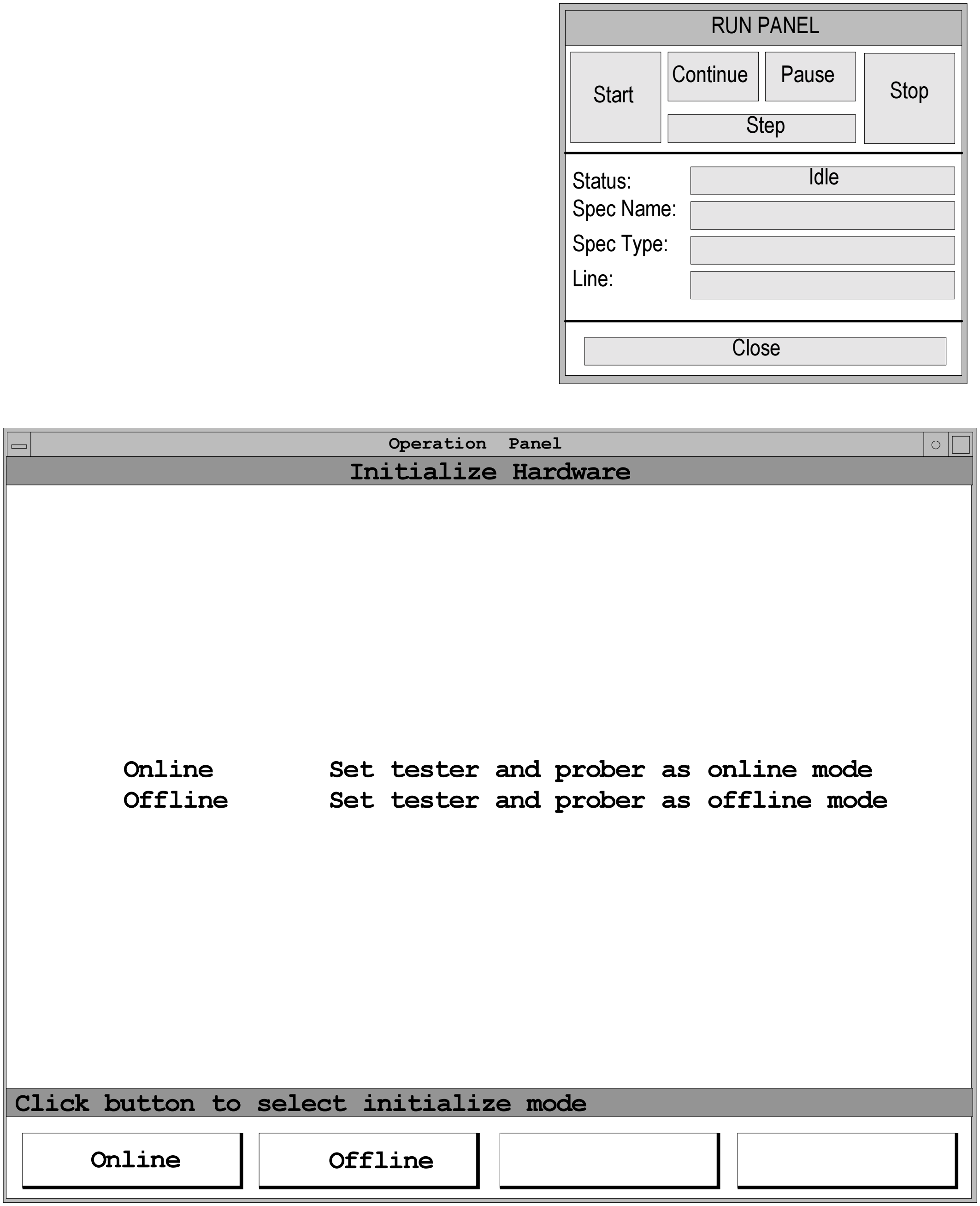


Figure 3-1 Launching the Framework



Using OUTLINER

1. Open the SPECS OUTLINER window.
2. Click Framework Open, and select your framework, for example, PDQ_FWK.
3. Click Test Plan Open, and select the test plan to execute, for example, MY_TEST.
4. Click Algorithm Change, and select the algorithm library you use, for example, PDQ_WLR2_01.
5. Select Execute:Execute. The RUN PANEL and OPERATION PANEL are displayed on the screen. See Figure 3-1.
6. Click Start on the RUN PANEL to launch the framework. Figure 3-1 shows an OPERATION PANEL after clicking Start.

Using the tplexec Command

The tplexec command launches your framework. Command syntax, options and parameters are shown below:

- **Syntax**

```
tplexec [-m meas] [-f fwk] [-i] tpl
```

- **Options and Parameters**

-m meas	Measurement algorithm library name, for example, TRNG.
-f fwk	Framework name, for example, HPSTD_NOPROBER.
-i	Interactive mode. Specifying the -i option opens the RUN PANEL and OPERATION PANEL, and waits for you to click the Start button. Without the -i option, the tplexec command launches your framework , and closes it immediately after the test.
tpl	Test plan name, for example, TPSMPL1.

NOTE

If you do not specify a -m or a -f option, the tplexec command uses the MEASLIB and FRAMEWORK values defined in the /opt/SPECS/sys/config/sysconf file.

- **Example**

```
tplexec -m PDQ_WLR2_01 -f PDQ_FWK MY_TEST
```

This example executes the PDQ_FWK framework, the PDQ_WLR2_01 algorithm library, and the MY_TEST test plan.

- **Remarks**

If you need help messages, enter `tplexec -?` .

The tplexec command also provides the -t, -p, and -u options. Do not specify these options. The tplexec command will automatically call and use the tester algorithm library (TESTERLIB), the prober algorithm library (PROBERLIB), and the utility algorithm library (UTILLIB) as defined in the /opt/SPECS/sys/config/sysconf file.

To Change PDQ-WLR Environment

Before starting the PDQ-WLR test, you can change the PDQ-WLR environment.

PDQ-WLR Environment

The items you can change are listed below. Set them using the PDQ-WLR Environment Setup panel.

DataBase Directory Path Directory path of the database. The default setting is /var/opt/WLR/database/data/measured/.

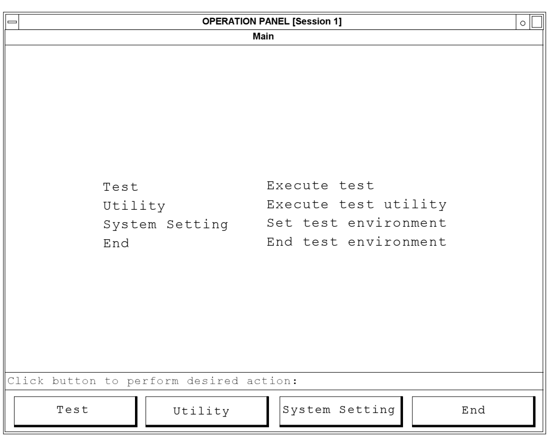
DataBase File Name Name of the test result data file. The default setting is default.dat.

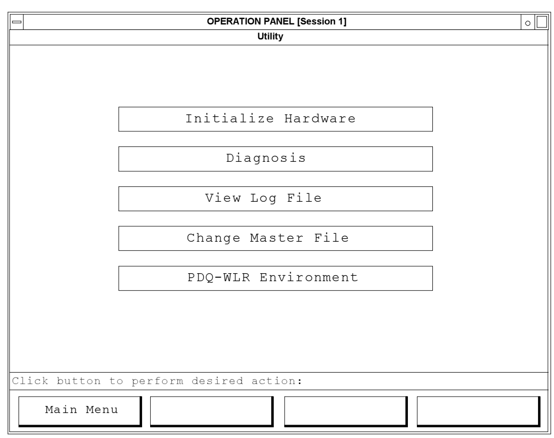
PDQ-WLR GUI Display Enables or disables the PDQ-WLR GUIs. If disabled, the operation panels for PDQ-WLR are never displayed. The default setting is Enable.

Instruction

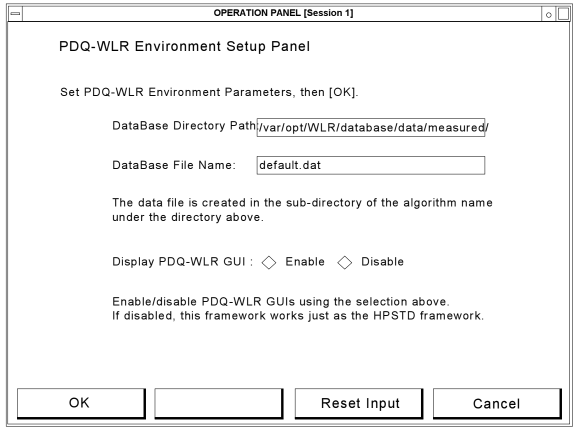
The following instructions show how to change the PDQ-WLR environment, and then update the /opt/SPECS/sys/config/sysconf file.

1. Launch your framework. Wait until the Initialize Hardware panel is displayed.
2. Click Offline to display the Hardware Configuration panel.
3. Click Next to display the Main panel shown below.
4. Click Utility to display the Utility panel shown below.





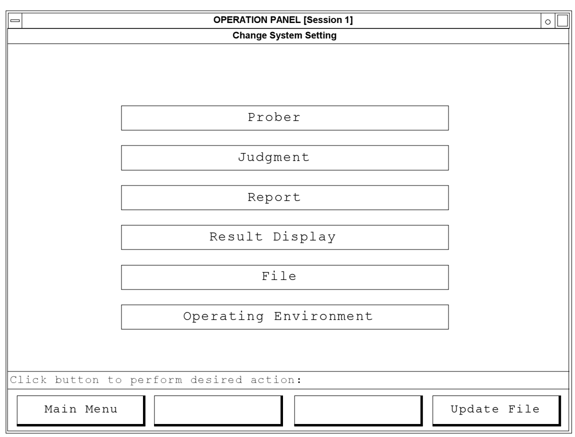
5. Click PDQ-WLR Environment to display the PDQ-WLR Environment Setup panel. Change the settings as you desire.



6. To return to the Utility panel, click OK.

   To apply the default values to the panel, click Reset Input.

   To apply the initial values to the panel and open the Utility panel, click Cancel.
7. On the Utility panel, click Main Menu to return to the Main panel.
8. On the Main panel, click System Setting to display the Change System Setting panel.



9. To store the new PDQ-WLR environment settings, click the Update File. The changes are saved in the sysconf file.
10. Click Main Menu to return to the Main panel.
11. On the Main panel, click End to exit your framework.

To Execute PDQ-WLR Test

You can run your framework, and execute the PDQ-WLR test as shown below. The following instructions are for the PDQ-WLR GUI Enable environment.

NOTE For details on using the HPSTD framework, refer to the *"Agilent SPECS Framework Operation Guide"*. See Chapter 4 for information on the additional operation panels in the PDQWLR_PLG plug framework.

1. Launch your framework. Wait until the Initialize Hardware panel is displayed.
2. **Initialize Hardware panel**

   To select the online execution mode and initialize the hardware, click Online.
3. **Hardware Configuration panel**

   After the initialization is finished, click Next.
4. **Main panel**

   To continue with the test setup, click Test.
5. **Register Operator panel**

   Enter the operator name in the Operator Name entry field, then click Next.
6. **Set Test Condition panel**

   Enter the lot ID, cassette ID, and process name in the entry fields (optional). Do *not* select the Limit File. It is not available for the PDQ-WLR test.

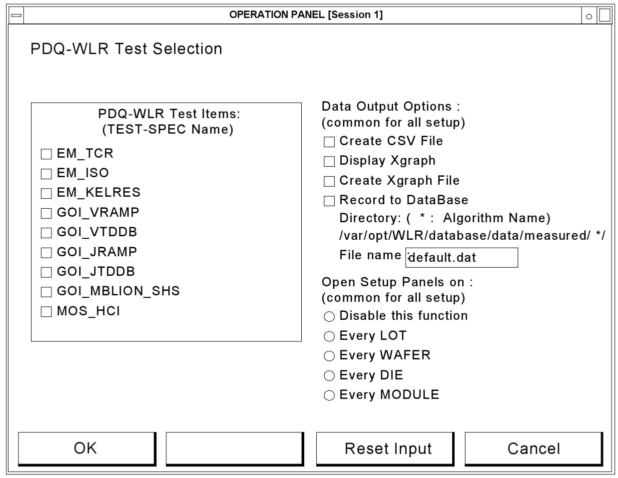
   To continue with the test setup, click Next.

   To return to the Main panel, click Main Menu.
7. **Select Wafer panel**

   Select the wafer ID, and click Start Test.

   To return to the Set Test Condition panel, click Abort Test.

8. **PDQ-WLR Test Selection panel**



Set the following as desire, and then click OK.

a. PDQ-WLR Test Items:

Select the test to execute. This area lists all the test specifications paired with die specifications in the test plan. If you open the PDQWLR_TPT test plan, the panel will be as shown above.

b. Data Output Options and Open Setup Panels on:

Select the options you desire. For information on selecting options, see “To Set PDQ-WLR Options” on page 3-13.

To apply the default values to the panel, click Reset Input.

To apply the default values to the panel and open the next panel, click Cancel.

9. **(Optional) Test Condition Setup panels**

If you selected “Every LOT” on the PDQ_WLR Test Selection panel in step 8 above, an operation panel will open. An example of an operation panel is shown in the next figure. It is for the GOI_VTDDB test. On the panel, do the following:

a. Set the test parameter values in the Test Paramters area.

See Panel Specifications in Chapter 4 for test parameter definitions.

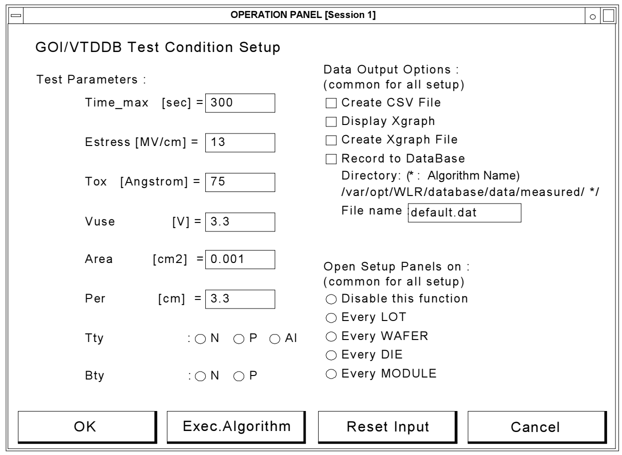
b. You can change the setup of the “Data Output Options” and “Open Setup Panels on”.

Click OK to accept the test setup and open the next panel.

To execute the algorithm, click Exec. Algorithm.

To apply the default values to the panel, click Reset Input.

To apply the default values to the panel and open the next panel, click Cancel.



10. **Select Die/Module panel**

    Select the dice and modules to test, then click Next. This starts the test.

    To apply the default settings to the panel, click Undo.

11. **Execute Test panel**

    This panel is displayed during test execution.

    To immediately stop the test, click Pause. See “To Set PDQ-WLR Options” on page 3-13 for more information.

12. **(Optional) PDQ-WLR Test Condition Setup panels**

    During test execution, a panel can be displayed for every wafer test, die test, or module test. The timing of the display depends on the setting of the “Open Setup Panels on” in steps 8 and 9.

13. **Test Result panel**

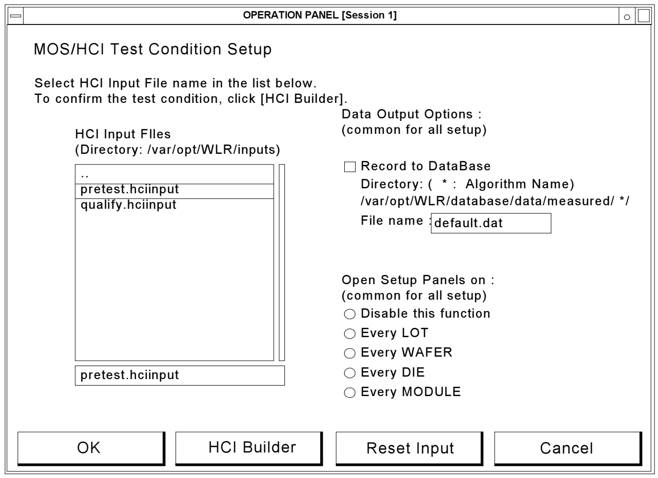
    This panel is displayed after the test, and shows the test result list.

    To return to the Set Test Condition panel, click Complete Test.

    To run the test again, select a wafer from the list, and select Start Retest.

If You Execute MOS_HCI Test

If your test plan contains a MOS_HCI test specification, and you select MOS_HCI on the PDQ-WLR Test Selection panel in step 8 of the previous procedure, you will see this panel in step 9 or 12.



On the panel, do following:

1. Select an HCI input file from the HCI Input Files list.
2. You can change the setup of the “Data Output Options” and “Open Setup Panels on”.

Click OK to accept the setup and open the next panel.

To execute the HCI builder, click HCI Builder.

To apply the default values to the panel, click Reset Input.

To apply the default values to the panel and open the next panel, click Cancel.

If you want to see, modify, or create the HCI input files, click the HCI Builder button. The HCI builder provides a graphical user interface to create the files. For details on the HCI builder, see the *“Agilent PDQ-WLR User’s Guide”*.

To Set PDQ-WLR Options

You can change the PDQ-WLR options while the PDQ-WLR test is in progress. The options can be changed as shown below.

PDQ-WLR Options

Options that can be changed are listed below. They are set using the PDQ-WLR Option Setup panel.

Data Output Options Selects the output data listed below. Multiple selections are available. The default settings are Display Xgraph and Record to DataBase. You can set the name of the test result data file for the database.

- Create CSV File (The CSV file is created after the test.)
- Display Xgraph (An Xgraph is displayed after test.)
- Create Xgraph File (An Xgraph file is created after test.)
- Record to Database (A .dat file is stored in database.)

Open Setup Panels on Selects the panel display option which specifies when the Test Condition Setup panel is displayed. The default is Every LOT selected.

- Disable this function (The panel is never displayed.)
- Every LOT (A panel is opened for every lot test).
- Every WAFER (A panel is opened for every wafer test.)
- Every DIE (A panel is opened for every die test.)
- Every MODULE (A panel is opened for every module test.)

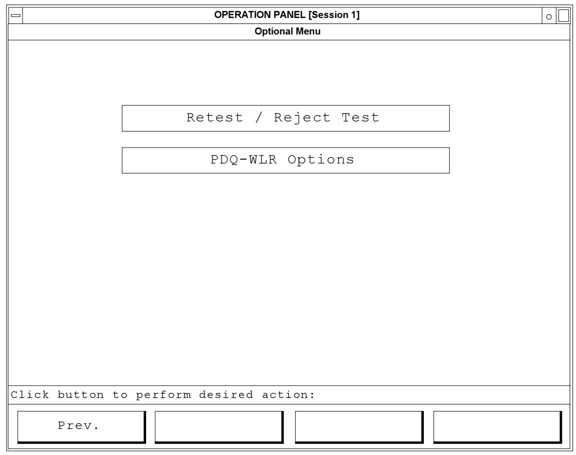
NOTE

The changes of the PDQ-WLR option setup are effective for the tests (algorithms) to be executed after closing the panel.

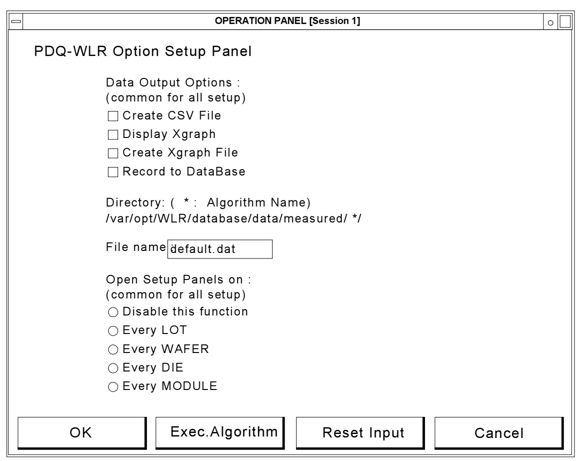
Instruction

You can change the PDQ-WLR options while a PDQ-WLR test is being executed and the Execute Test panel is displayed.

1. Click Pause on the Execute Test panel. Click Option to display the Optional Menu panel.



2. Click PDQ-WLR Options to display the PDQ-WLR Option Setup panel. Set the options as you desire.



3. Click OK to return to the Optional Menu panel.

4. Click Prev. to return to the Execute Test panel.

4 PDQWLR_PLG Plug Framework

The Agilent PDQ-WLR software provides plug framework PDQWLR_PLG.fwk. This chapter describes the PDQWLR_PLG plug framework, and consists of the following sections:

- "Overview"

  Explains the program flow and the additional specifications of the PDQWLR_PLG plug framework.

- "Action Specifications"

  Describes the action specifications that have been modified and added to the HPSTD framework.

- "Panel Specifications"

  Describes the panel specifications added to the HPSTD framework.

- "SYSTEM Tag Specification"

  Lists the tag variables added to the SYSTEM tag specification.

- "Configuration File"

  Lists the differences between the PDQWLR_PLG.cf file and the HPSTD framework configuration file.

NOTE

After installing the PDQ-WLR software, the PDQWLR_PLG plug framework is stored in the /opt/SPECS/usr/fwk/plug/pdqwlr directory.

Overview

This section describes the following topics:

- "Execution Flow" of the PDQWLR_PLG plug framework
- "Additional Specifications" of the PDQWLR_PLG plug framework

Execution Flow

The flowchart in Figure 4-1 shows the program flow of the PDQWLR_PLG plug framework. The program flow inside the dotted line is added to the HPSTD framework.

PDQ-WLR Environment Setup and PDQ-WLR Option Setup are called by the configuration file (PDQWLR_PLG.cf). For information on the settings in the configuration file, see "Configuration File" on page 4-33.

1. PDQ-WLR Environment Setup

   You can change the PDQ-WLR environment using the following specifications.

   - WLR_ENVS action specification
   - WLR_SetEnvs panel specification

2. PDQ-WLR Test Selection

   You can select PDQ-WLR test items and options using the following specifications.

   - WLR_TEST_SELECT panel specification
   - WLR_CheckPlotOptions action specification

3. Open Setup Panel every lot/wafer/die/module?, Test Condition Setup

   You can set test conditions, and change the PDQ-WLR options for every lot, wafer, die, or module using the following specifications.

   - WLR_TCS_XXXX action specification
   - WLR_CheckPlotOptions action specification
   - WLR_XXXX_OpenAlgPanel action specification
   - WLR_OpenAlgPanel action specification
   - WLR_XXXX panel specification

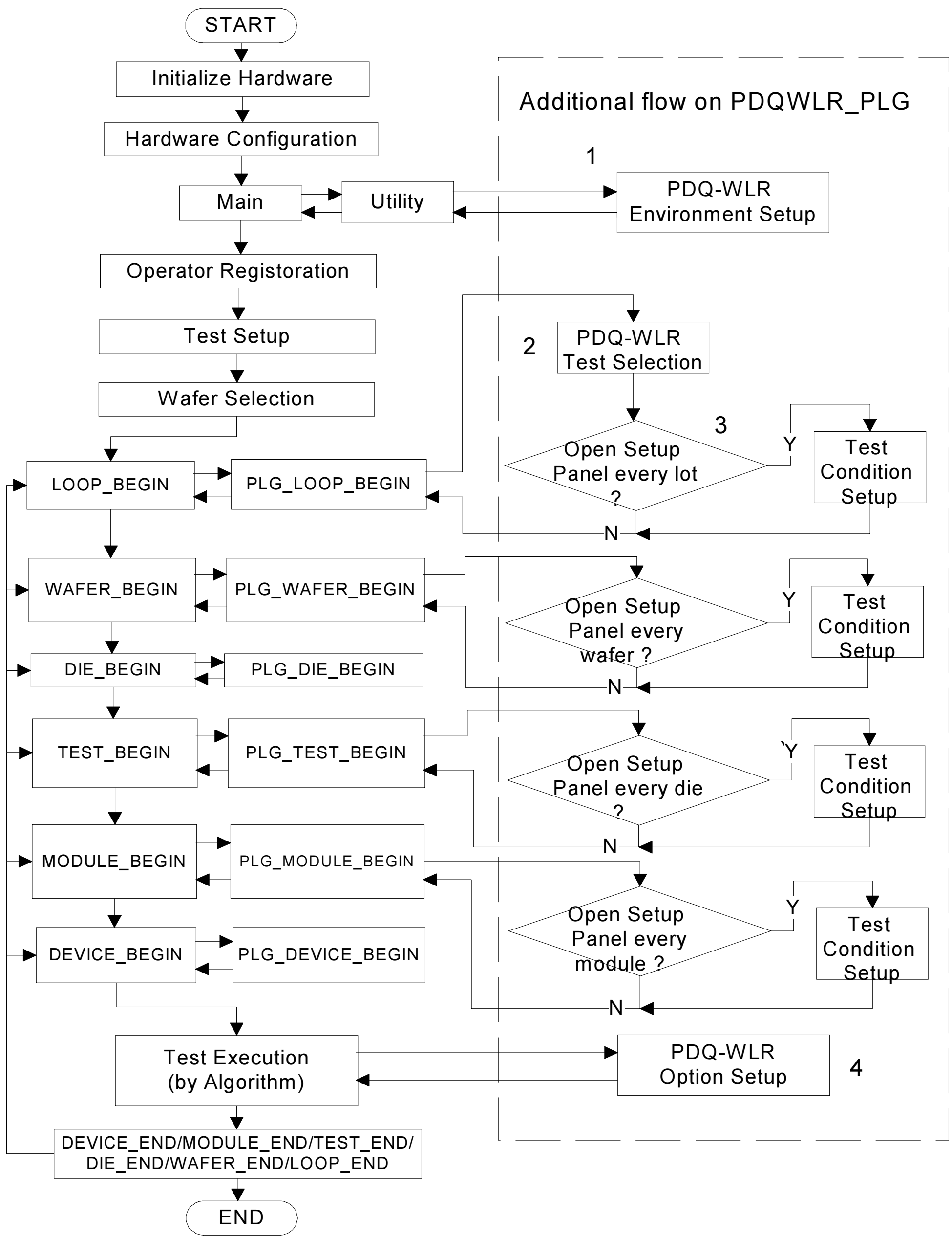
   where, XXXX is a test specification name.

4. PDQ-WLR Option Setup

   You can change PDQ-WLR options during test execution using the following specifications.

   - WLR_OPTIONS action specification
   - WLR_SetOptions_OpenAlgPanel action specification
   - WLR_OpenAlgPanel action specification
   - WLR_SetOptions panel specification

Figure 4-1 Execution Flow



Additional Specifications

The flowchart in Figure 4-2 shows the program flow of the PDQWLR_PLG plug framework. The program flow inside the dotted line is added to the HPSTD framework.

1. WLR_ENVS.Action and WLR_SetEnvs.Panel

   This is called by the PDQ-WLR Environment menu button on the Utility panel. The WLR_SetEnvs panel specification is used to display the PDQ-WLR Environment Setup panel. This panel is used to set the directory and file name of the database, and to select the PDQ-WLR GUI environment.
   The Utility panel is displayed by clicking the Utility button on the Main panel which is called by the SYSTEM system specification through the HP_SEL_SYSTEM_JOB action specification.

2. WLR_TEST_SELECT.Panel

   The PLG_LOOP_BEGIN action specification calls this panel which displays the PDQ-WLR Test Selection panel. This panel is used to select the desired test, the data output option, and the panel display option. The panel display option determines when the Test Condition Setup panels are displayed.

3. WLR_TCS_XXXX.Action and WLR_XXXX.Panel

   The PLG_YYYY_BEGIN action specification checks the panel display option and executes the action specification that calls the WLR_XXXX panel specification used to display the Test Condition Setup panel. The panel is used to set the test condition for the test selected on the PDQ-WLR Test Selection panel, the data output option, and the panel display option, where, YYYY is LOOP, WAFER, TEST, or MODULE, and XXXX is the name of the test specification, for example, EM_ISO.

4. WLR_CheckPlotOptions.Action

   After closing the PDQ-WLR Test Selection panel or the Test Condition Setup panel, the PLG_YYYY_BEGIN action specification executes the specification which checks the data output option.

5. WLR_XXXX_OpenAlgPanel.Action

   Selecting the Exec. Algorithm button on the Test Condition Setup panel executes this specification that calls the WLR_OpenAlgPanel.Action.

6. WLR_OPTIONS.Action and WLR_SetOptions.Panel

   If you click the PDQ-WLR Options button on the Optional Menu panel, this specification calls the WLR_SetOptions panel specification used to display the

PDQ-WLR Options panel. This operation panel selects the data output option and the panel display option. To display the Optional Menu panel, click the Pause button on the Execute Test panel and then click the Option button.

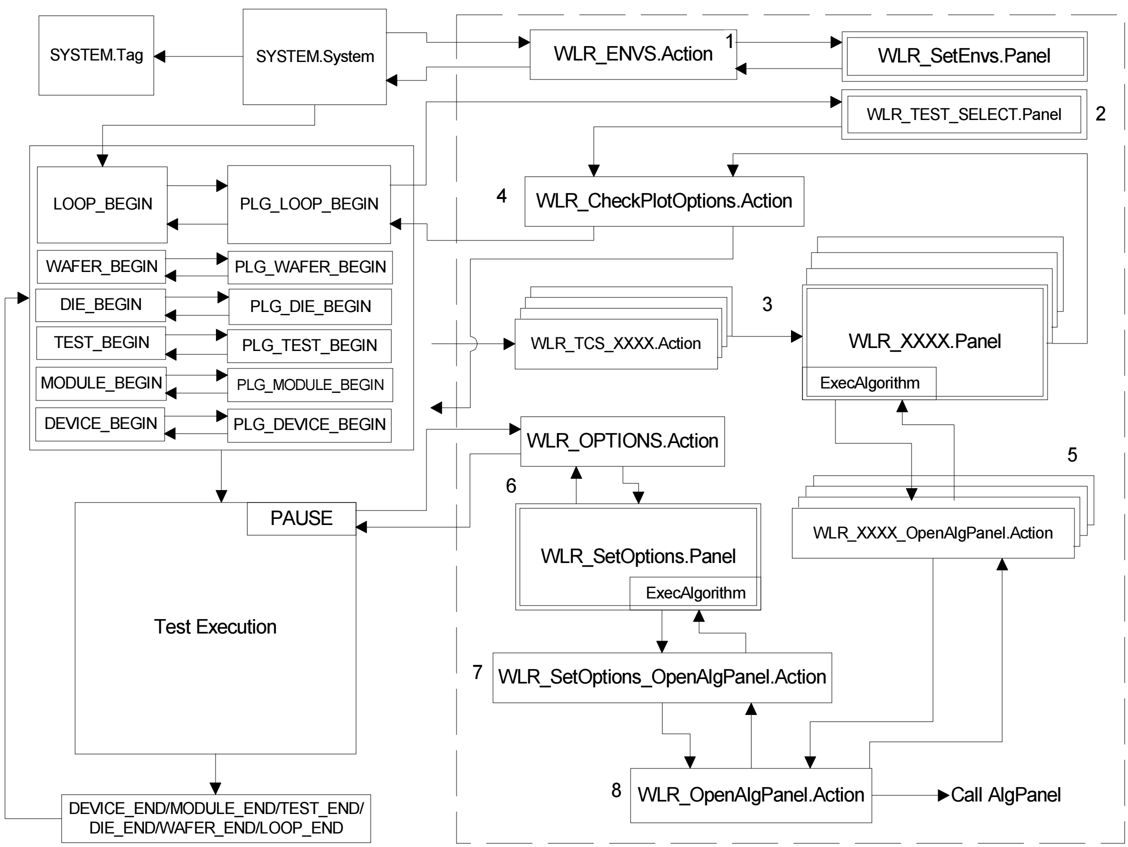
7. WLR_SetOptions_OpenAlgPanel.Action

   This is called by the Exec. Algorithm button on the PDQ-WLR Options panel. This action specification calls the WLR_OpenAlgPanel action specification.

8. WLR_OpenAlgPanel.Action

   WLR_XXXX_OpenAlgPanel or WLR_SetOptions_OpenAlgPanel action specification executes the specification that calls the Algorithm Panel.

Figure 4-2 Additional Specifications



Additional Specifications on PDQWLR_PLG

Action Specifications

The following action specifications are modified, or added to the HPSTD framework to create the PDQWLR_PLG plug framework.

Specification Name	Remarks
PLG_FWK_BEGIN	Modified. See page 4-9.
PLG_LOOP_BEGIN	Modified. See page 4-10.
PLG_MODULE_BEGIN	Modified. See page 4-12.
PLG_TEST_BEGIN	Modified. See page 4-11.
PLG_WAFER_BEGIN	Modified. See page 4-11.
WLR_CheckPlotOptions	
WLR_EM_ISO_OpenAlgPanel	See “WLR_XXXX_OpenAlgPanel”
WLR_EM_TCR_OpenAlgPanel	See “WLR_XXXX_OpenAlgPanel”
WLR_ENVS	
WLR_GOI_JRAMP_OpenAlgPanel	See “WLR_XXXX_OpenAlgPanel”
WLR_GOI_JTDDB_OpenAlgPanel	See “WLR_XXXX_OpenAlgPanel”
WLR_GOI_MBLION_SHS_OpenAlgPanel	See “WLR_XXXX_OpenAlgPanel”
WLR_GOI_VRAMP_OpenAlgPanel	See “WLR_XXXX_OpenAlgPanel”
WLR_GOI_VTDDB_OpenAlgPanel	See “WLR_XXXX_OpenAlgPanel”
WLR_HCI_OpenHCI	
WLR_OpenAlgPanel	
WLR_OPTIONS	
WLR_SetOptions_OpenAlg_Panel	See “WLR_XXXX_OpenAlgPanel”
WLR_TCS_EM_ISO	See “WLR_TCS_XXXX”
WLR_TCS_EM_TCR	See “WLR_TCS_XXXX”
WLR_TCS_GOI_JRAMP	See “WLR_TCS_XXXX”
WLR_TCS_GOI_JTDDB	See “WLR_TCS_XXXX”
WLR_TCS_GOI_MBLION_SHS	See “WLR_TCS_XXXX”
WLR_TCS_GOI_VRAMP	See “WLR_TCS_XXXX”
WLR_TCS_GOI_VTDDB	See “WLR_TCS_XXXX”
WLR_TCS_MOS_HCI	
WLR_TCS_TestName	
WLR_TCS_TestName_OpenAlgPanel	

PLG_FWK_BEGIN

This action specification is called from the SYSTEM system specification, and executed after the Copyright panel is displayed.

This specification executes following:

1. (InitGUI_OnOff) Checks the initial setting of the GUI environment.
2. (TCS_ActionList) Registers the Test Condition Setup panels available.
3. (PlotOptionLabel) Sets the values in the WLR_PlotOptions and WLR_PlotSelected arrays used to set the data output option.
4. (TestConditionLabel) Sets the values in the WLR_TCS_Options and WLR_TCS_Selected arrays used to select the panel display option.
5. (DataBaseAccessLabel) Sets the value of the variables.
6. (Initialize_Arrays) Sets the values in the WLR_ISO_Maxro array and WLR_TCR_LinkOptions array.
7. (VRAMP_InitialTry) Sets the values in WLR_GOI_TtyOptions array and WLR_XXXX_TtySelected array, where, XXXX is VRAMP, VTDDB, JRAMP or JTDDB.
8. (VRAMP_InitialBty) Sets the values in the WLR_GOI_BtyOptions array and WLR_XXXX_BtySelected array, where, XXXX is VRAMP, VTDDB, JRAMP or JTDDB.
9. (OpenTemplateTCS) Normally commented out. Useful for debugging the operation panels. Calls the WLR_TCS_TestName action specification.

PLG_LOOP_BEGIN

This action specification is called from the LOOP_BEGIN action specification, and executes the following:

1. (Check_GUI_OnOff) Checks the PDQ-WLR GUI display environment, Enable or Disable. If Disable is selected, it quits this specification. If Enable is selected, the following is executed.
2. (Initialize_Labels) Gets the test specification names defined in the test plan to execute.
3. (InitializeDieTestSelected) Initializes the WLR_DieSelected array.
4. (DefineSelectRow) Sets the maximum number of test items to 15.
5. (Open_TestSelectPanel) Calls the WLR_TEST_SELECT panel specification that displays the PDQ-WLR Test Selection panel.
6. (CheckPlotOptions) Calls the WLR_CheckPlotOptions action specification that checks the panel display option setting.
7. (Check_Test_Selection) Checks the number of the test items selected in the PDQ-WLR Test Selection panel, and gets the die specification names paired to the tests selected on the PDQ-WLR Test Selection panel.
8. (UNSELECT_ALL_TESTs) UNSELECTs all the tests defined in the test plan.
9. (SELECT_TESTs) SELECTs the tests selected in the panel.
10. (UNSELECT_ALL_DIEs) UNSELECTs all the dice defined in the test plan.
11. (SELECT_DIEs) SELECTs the dice selected in the panel.
12. (SelectedTestList) Creates a list of the selected tests.
13. (CheckTCS_Flag) If the panel display option is “Every LOT”, the following is performed:

    a. Calls the WLR_TCS_XXXX action specification (XXXX: test specification name) that displays the Test Condition Setup panels.

    b. Calls the WLR_CheckPlotOptions action specification that checks the panel display option setting.

PLG_WAFER_BEGIN

This action specification is called from the WAFER_BEGIN action specification, and executes the following:

1. Checks the PDQ-WLR GUI display environment, Enable or Disable. If Disable is selected, it quits this specification. If Enable is selected, the following is executed.
2. If the panel display option is “Every WAFER”, the following is performed:
    a. Calls the WLR_TCS_XXXX action specification (XXXX: test specification name) that displays the Test Condition Setup panels.
    b. Calls the WLR_CheckPlotOptions action specification that checks the panel display option setting.

PLG_TEST_BEGIN

This action specification is called from the TEST_BEGIN action specification, and executes the following:

1. Checks the PDQ-WLR GUI display environment, Enable or Disable. If Disable is selected, it quits this specification. If Enable is selected, the following is executed.
2. If the panel display option is “Every DIE”, the following is performed:
    a. Calls the WLR_TCS_XXXX action specification (XXXX: test specification name) that displays the Test Condition Setup panels.
    b. Calls the WLR_CheckPlotOptions action specification that checks the panel display option setting.

PLG_MODULE_BEGIN

This action specification is called from the MODULE_BEGIN action specification, and executes following:

1. Checks the PDQ-WLR GUI display environment, Enable or Disable. If Disable is selected, it quits this specification. If Enable is selected, the following is executed.
2. If the panel display option is "Every MODULE", the following is performed:
   a. Calls the WLR_TCS_XXXX action specification (XXXX: test specification name) that displays the Test Condition Setup panels.
   b. Calls the WLR_CheckPlotOptions action specification that checks the panel display option setting.

WLR_CheckPlotOptions

This action specification checks the data output options; Create CSV File, Display Xgraph, Create Xgraph File, and Record to DataBase. It also checks the database directory and file name. This specification creates the Plot (Plot$) parameter for the PDQ-WLR algorithms.

WLR_ENVS

This action specification calls the WLR_SetEnvs panel specification that is used to set the database directory and file name, and the PDQ-WLR GUI display environment, GUI enable or GUI disable.

WLR_HCI_OpenHCI

This action specification calls the HCI Builder used to create the HCI input file.

WLR_OpenAlgPanel

This specification calls the Algorithm Panel used to execute the algorithms directly.

WLR_OPTIONS

This specification calls the WLR_SetOptions panel specification used to select the data output option and the panel display option.

WLR_TCS_MOS_HCI

This action specification calls the WLR_MOS_HCI panel specification.

WLR_TCS_TestName

This is an action specification template. You can use this specification to add a new operation panel to your framework. The specification must operate the same as the WLR_TCS_XXXX action specification. See “To Add Operation Panels” in Chapter 2.

WLR_TCS_TestName_OpenAlgPanel

This is an action specification template. You can use this specification to add a new operation panel to your framework. The specification must operate the same as the WLR_XXXX_OpenAlgPanel action specification. See “To Add Operation Panels” in Chapter 2.

WLR_TCS_XXXX

This specification calls the WLR_XXXX panel specification that is used to set the test condition of the test specification, where, XXXX is a test specification name such as EM_ISO.

WLR_XXXX_OpenAlgPanel

This action specification calls the WLR_OpenAlgPanel action specification which calls the Algorithm Panel, where, XXXX is SetOptions, or a test specification name such as EM_ISO.

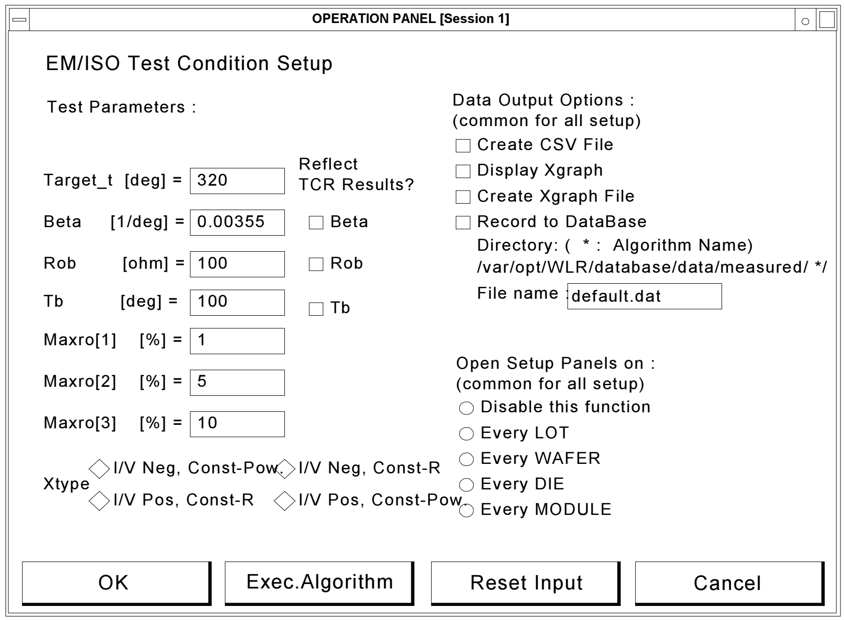
Panel Specifications

The PDQWLR_PLG plug framework defines the following additional panel specifications against the HPSTD framework.

Specification Name	Refer to
WLR_EM_ISO	page 4-15
WLR_EM_TCR	page 4-16
WLR_ErrDisp	page 4-23
WLR_GOI_JRAMP	page 4-17
WLR_GOI_JTDDB	page 4-18
WLR_GOI_MBLION_SHS	page 4-19
WLR_GOI_VRAMP	page 4-20
WLR_GOI_VTDDB	page 4-21
WLR_MOS_HCI	page 4-22
WLR_SetEnvs	page 4-23
WLR_SetOptions	page 4-24
WLR_TEST_SELECT	page 4-25
WLR_TestName	page 4-25

WLR_EM_ISO

This panel specification displays the EM/ISO Test Condition Setup panel shown below. This panel is used to set the test condition of the EM_ISO test specification.

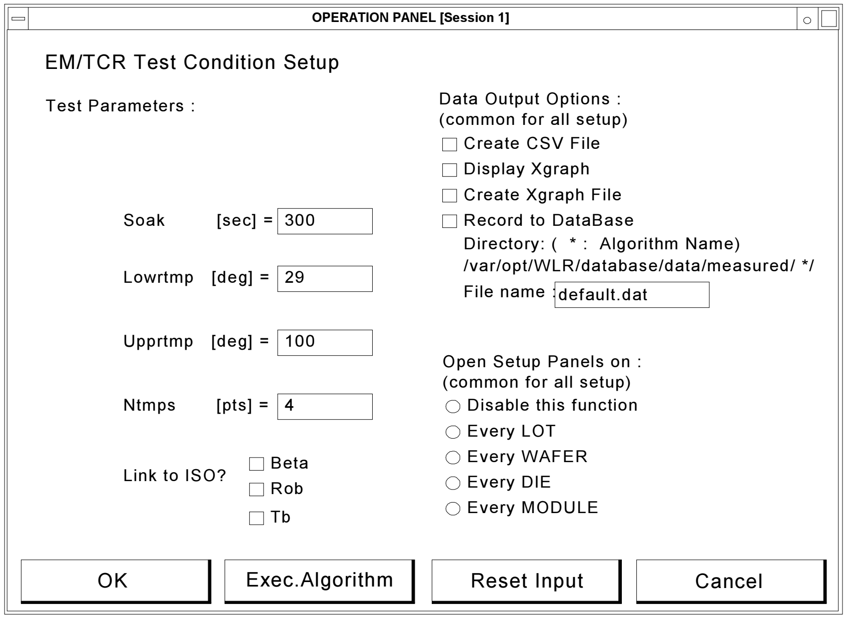


The relationship between the SYSTEM tag variables and the entry fields on the operation panel is shown below. See also “WLR_SetOptions” on page 4-24.

Entry Field Name	Tag Variable Name	Description
Reflect TCR Results?	WLR_TCR_LinkSelected	Uses EM/TCR test result Beta/Rob for this test, or not
Target_t [deg]	WLR_ISO_Target_t	Desired stress temperature
Beta [1/deg]	WLR_ISO_Beta	Temperature coefficient of resistance
Rob [ohm]	WLR_ISO_Rob	Ro from TCR algorithm
Tb [deg]	WLR_ISO_Tb	Tb from TCR algorithm
Maxro[1] [%]	WLR_ISO_Maxro[1]	Maximum allowable change in Delta_ro
Maxro[2] [%]	WLR_ISO_Maxro[2]	
Maxro[3] [%]	WLR_ISO_Maxro[3]	
Xtype	WLR_ISO_XtypeSelected	Execution type

WLR_EM_TCR

This panel specification displays the EM/TCR Test Condition Setup panel shown below. This panel is used to set the test condition of the EM_TCR test specification.

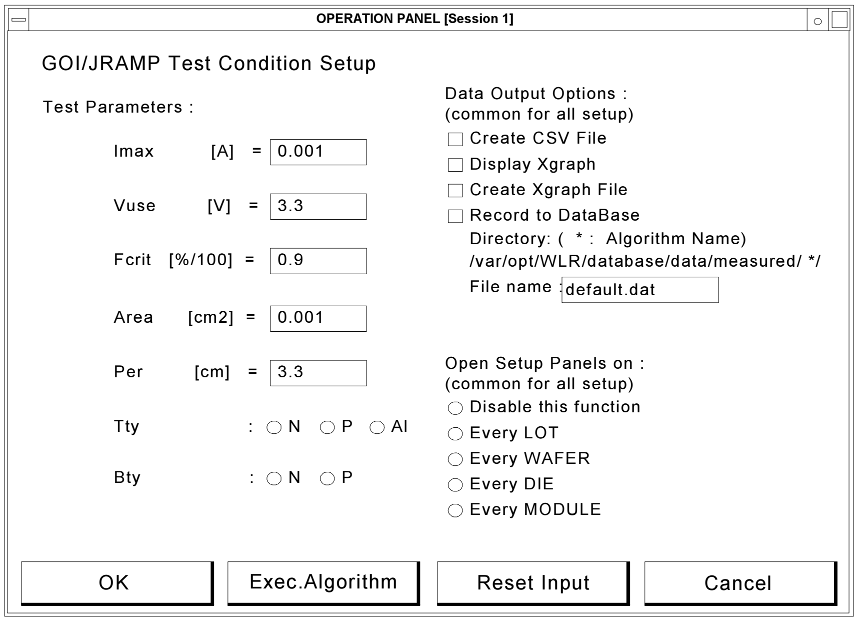


The relationship between the SYSTEM tag variables and the entry fields on the operation panel is shown below. See also “WLR_SetOptions” on page 4-24.

Entry Field Name	Tag Variable Name	Description
Soak [sec]	WLR_TCR_Soak	Soak time at temperature
Lowrtmp [deg]	WLR_TCR_Lowrtmp	Lower limit for temperature range
Upprtmp [deg]	WLR_TCR_Upprtmp	Upper limit for temperature range
Ntmps [pts]	WLR_TCR_Ntmps	Total number of at-temperatures measurements
Link to ISO?	WLR_TCR_LinkSelected	Links Beta/Rob results to EM/ISO test, or not

WLR_GOI_JRAMP

This panel specification displays the GOI/JRAMP Test Condition Setup panel shown below. This panel is used to set the test condition of the GOI_JRAMP test specification.

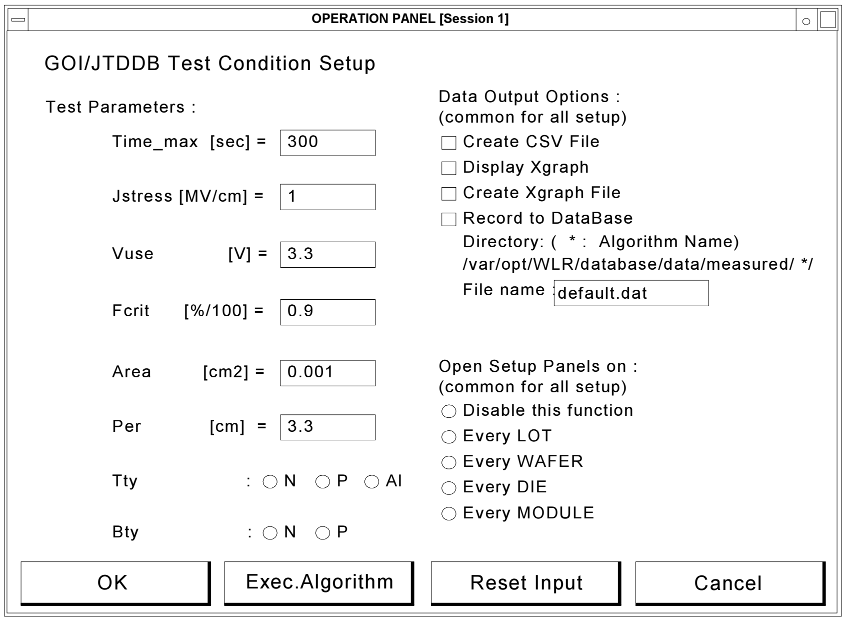


The relationship between the SYSTEM tag variables and the entry fields on the operation panel is shown below. See also “WLR_SetOptions” on page 4-24.

Entry Field Name	Tag Variable Name	Description
Imax [A]	WLR_JRAMP_Imax	Maximum ramp current
Vuse [V]	WLR_JRAMP_Vuse	Pre and Post test compliance voltage
Fcrit [%/100]	WLR_JRAMP_Fcrit	Voltage failure criteria
Area [cm2]	WLR_JRAMP_Area	Area of active region [cm^2]
Per [cm]	WLR_JRAMP_Per	Perimeter of active region [cm]
Tty	WLR_JRAMP_Tty	Top electrode type. “N”, “P”, or “Al”
Bty	WLR_JRAMP_Bty	Dopant type of bulk region. “N” or “P”

WLR_GOI_JTDDB

This panel specification displays the GOI/JTDDB Test Condition Setup panel shown below. This panel is used to set the test condition of the GOI_JTDDB test specification.

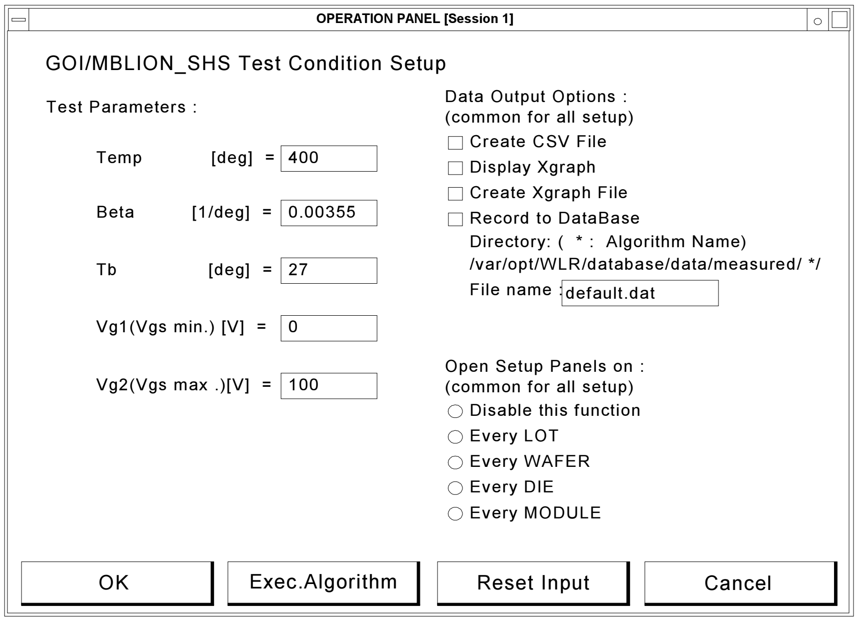


The relationship between the SYSTEM tag variables and the entry fields on the operation panel is shown below. See also “WLR_SetOptions” on page 4-24.

Entry Field Name	Tag Variable Name	Description
Time_max [sec]	WLR_JTDDB_Time_max	Maximum time to wait for breakdown
Jstress [MV/cm]	WLR_JTDDB_Jstress	Stressing current density
Vuse [V]	WLR_JTDDB_Vuse	Pre and Post test voltage
Fcrit [%/100]	WLR_JTDDB_Fcrit	Voltage failure criteria
Area [cm2]	WLR_JTDDB_Area	Area of active region [cm^2]
Per [cm]	WLR_JTDDB_Per	Perimeter of active region [cm]
Tty	WLR_JTDDB_Tty	Top electrode type. “N”, “P”, or “Al”
Bty	WLR_JTDDB_Bty	Dopant type of bulk region. “N” or “P”

WLR_GOI_MBLION_SHS

This panel specification displays the GOI/MBLION_SHS Test Condition Setup panel shown below. This panel is used to set the test condition of the GOI_MBLION_SHS test specification.

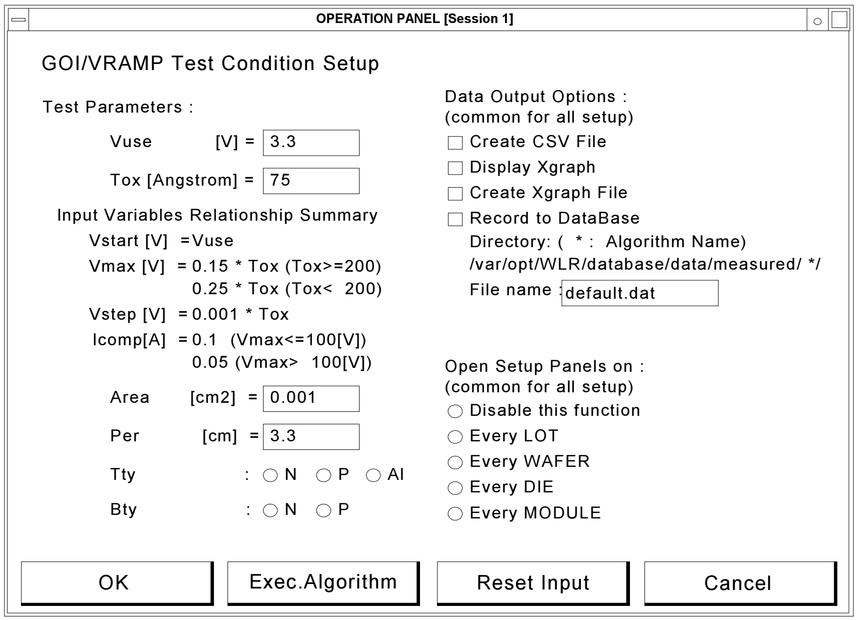


The relationship between the SYSTEM tag variables and the entry fields on the operation panel is shown below. See also “WLR_SetOptions” on page 4-24.

Entry Field Name	Tag Variable Name	Description
Temp [deg]	WLR_MBLION_Temp	Temperature of device
Beta [1/deg]	WLR_MBLION_Beta	Temperature coefficient of resistance
Tb [deg]	WLR_MBLION_Tb	Temperature at which Beta is defined
Vg1(Vgs min.) [V]	WLR_MBLION_Vgmin	Minimum gate voltage
Vg2(Vgs max.) [V]	WLR_MBLION_Vgmax	Maximum gate voltage

WLR_GOI_VRAMP

This panel specification displays the GOI/VRAMP Test Condition Setup panel shown below. This panel is used to set the test condition of the GOI_VRAMP test specification.

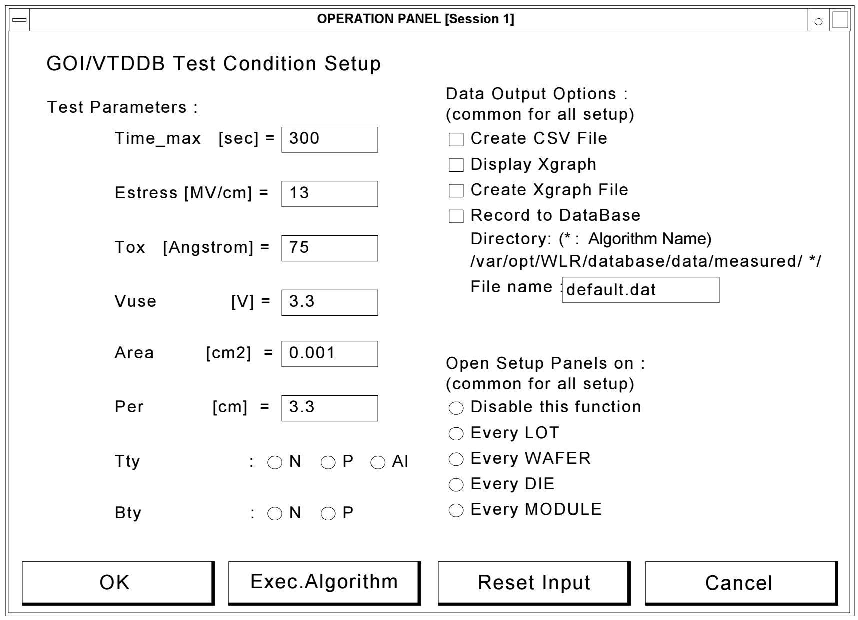


The relationship between the SYSTEM tag variables and the entry fields on the operation panel is shown below. See also “WLR_SetOptions” on page 4-24.

Entry Field Name	Tag Variable Name	Description
Vuse [V]	WLR_VRAMP_Vuse	Post test check voltage
Tox [Angstrom]	WLR_VRAMP_Tox	Design oxide thickness
Area [cm2]	WLR_VRAMP_Area	Area of active region [cm^2]
Per [cm]	WLR_VRAMP_Per	Perimeter of active region [cm]
Tty	WLR_VRAMP_Tty	Top electrode type. “N”, “P”, or “Al”
Bty	WLR_VRAMP_Bty	Dopant type of bulk region. “N” or “P”

WLR_GOI_VTDDB

This panel specification displays the GOI/VTDDB Test Condition Setup panel shown below. This panel is used to set the test condition of the GOI_VTDDB test specification.



The relationship between the SYSTEM tag variables and the entry fields on the operation panel is shown below. See also “WLR_SetOptions” on page 4-24.

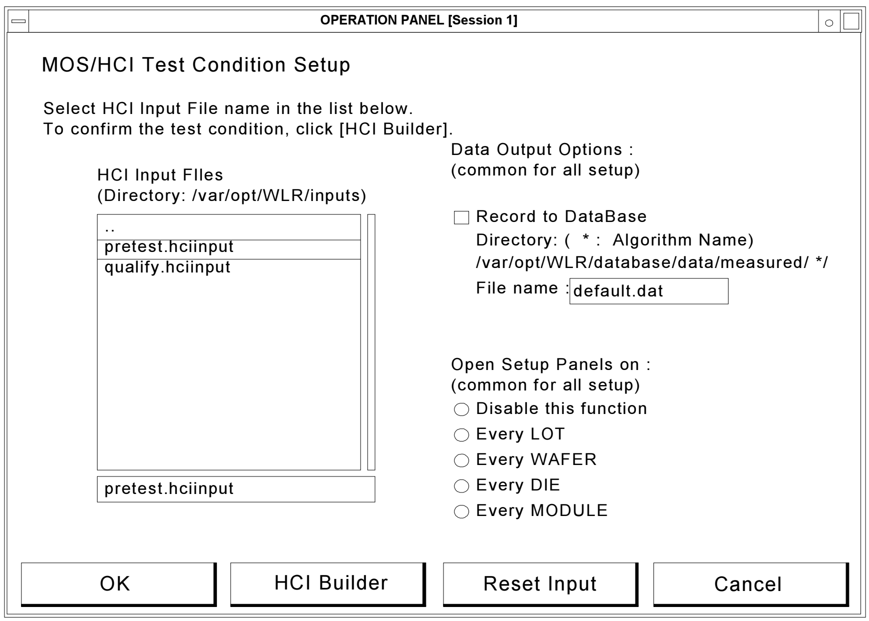
Entry Field Name	Tag Variable Name	Description
Time_max [sec]	WLR_VTDDB_Time_max	Maximum time to wait for breakdown
Estress [MV/cm]	WLR_VTDDB_Estress	Field at which capacitor is stressed
Tox [Angstrom]	WLR_VTDDB_Tox	Design oxide thickness
Vuse [V]	WLR_VTDDB_Vuse	Pre and post test check voltage
Area [cm2]	WLR_VTDDB_Area	Area of active region [cm^2]
Per [cm]	WLR_VTDDB_Per	Perimeter of active region [cm]
Tty	WLR_VTDDB_Tty	Top electrode type. “N”, “P”, or “Al”
Bty	WLR_VTDDB_Bty	Dopant type of bulk region. “N” or “P”

WLR_MOS_HCI

This panel specification displays the MOS/HCI Test Condition Setup panel as shown below. This panel is for the MOS_HCI test specification, and is used for selecting a HCI input file which must be passed to the HCI_3_MOS_XL algorithm to execute the HCI test.

To select the file, select one from the HCI Input Files list area, and then click OK.

If you want to see/modify/create the HCI input file, click HCI Builder button. The HCI builder provides graphical user interface to create the file. For details of and how to use the HCI builder, see *“Agilent PDQ-WLR User’s Guide”*.



The relationship between the SYSTEM tag variables and the entry fields on the operation panel is shown below. See also “WLR_SetOptions” on page 4-24.

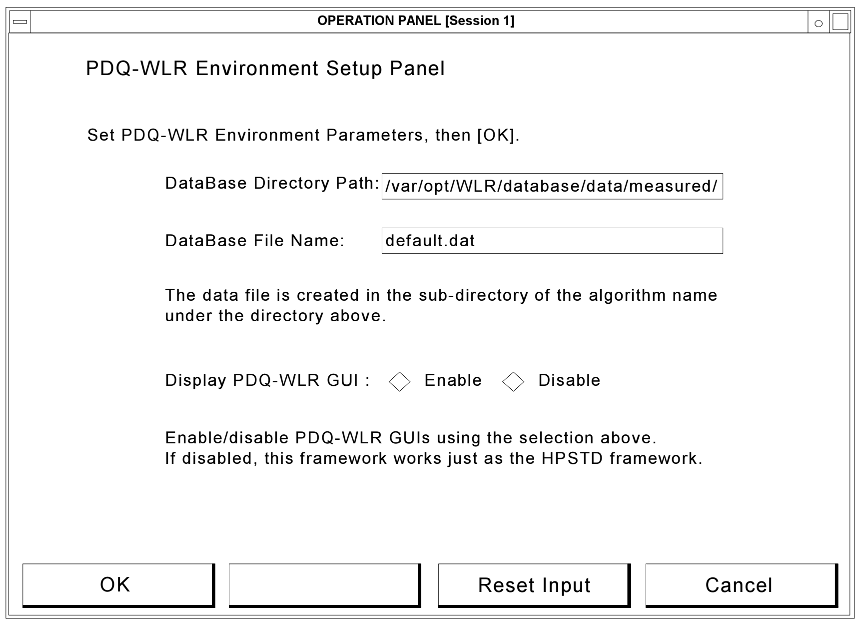
Entry Field Name	Tag Variable Name	Description
HCI Input Files (selected)	WLR_HCI_File_in	HCI input file used for the test

WLR_ErrDisp

This panel specification displays error messages on the panel, as the errors occur. Error messages are defined in the action specifications that display this panel.

WLR_SetEnvs

This panel specification displays the PDQ-WLR Environment Setup panel shown below. This panel is used to set the directory and file name of the database, and the PDQ-WLR GUI environment.

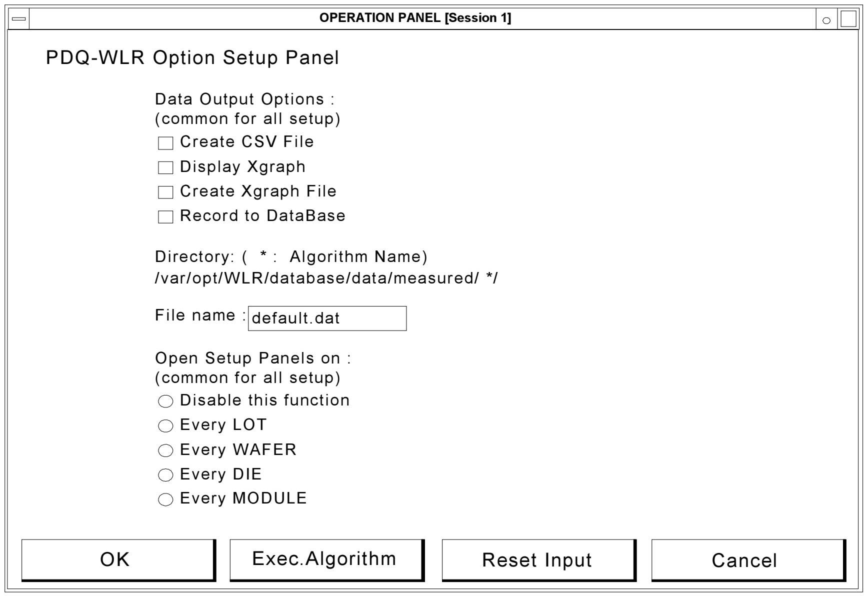


The relationship between the SYSTEM tag variables and the entry fields on the operation panel is shown below.

Entry Field Name	Tag Variable Name	Description
DataBase Directory Path?	WLR_DB_DirPath	Directory path of database
DataBase File Name?	WLR_DB_FileName	Name of test result data file for database
Display PDQ-WLR GUI	WLR_GUI_OnOff	GUI display mode Enable or Disable

WLR_SetOptions

This panel specification displays the PDQ-WLR Option Setup panel shown below. The panel is used to set the data output option and panel display option.



The OK button accepts the setup, and opens the next panel.

The Reset Input button applies the default settings to the panel.

The Cancel button applies the default settings, and opens the next panel.

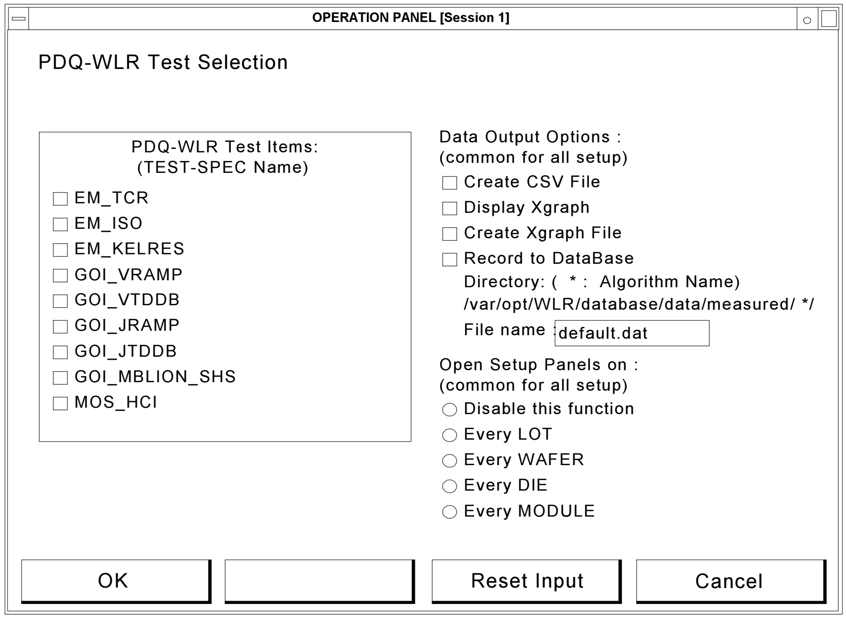
The Exec.Algorithm button opens the Algorithm Panel. For details on the Algorithm Panel, see the *“Agilent SPECS Measurement Algorithm Development Guide”*.

The relationship between the SYSTEM tag variables and the entry fields on the operation panel is shown below.

Entry Field Name	Tag Variable Name	Description
Data Output Options	WLR_PlotSelected	Data output option selected
File Name	WLR_DB_FileName	Name of test result data file for database
Open Setup Panels on	WLR_TCS_Selected	Panel display option selected

WLR_TEST_SELECT

This panel specification displays the PDQ-WLR Test Selection panel shown below.



The relationship between the SYSTEM tag variables and the entry fields on the operation panel is shown below. See also “WLR_SetOptions” on page 4-24.

Entry Field Name	Tag Variable Name	Description
PDQ-WLR Test Items	WLR_TestSelected	Test items selected
	WLR_TestLabel	

WLR_TestName

This is an panel specification template. You can use this specification to add a new operation panel to your framework. The new operation panel is used to set the test conditions of the test specification you add. See “To Add Operation Panels” in Chapter 2.

The panel has seven predefined entry fields to make modification easier. Use the WLR_TCS_VarLabel[ ] array variable to define the label of the fields.
Use the WLR_TCS_Var[ ] array variable to define the values.

SYSTEM Tag Specification

The PDQWLR_PLG plug framework defines the following additional SYSTEM tag variables. Variables marked with an asterisk (*) are used in the operation panels.

SYSTEM Tag Variables for ISO_4_EMR Algorithm

Name	Type	Description	Initial Value
WLR_ISO_Alpha	REAL	Slope of T_peak vs T_avg.	1
WLR_ISO_Beta *	REAL	Temperature coefficient of resistance [1/°C]	0.00355
WLR_ISO_Chuck_tmp	REAL	Ambient temperature of chuck [°C]	29
WLR_ISO_Maxro *	REAL[3]	Maximum allowable charge in Delta_ro [%]	
WLR_ISO_Rob *	REAL	Ro from TCR algorithm [ohm]	100
WLR_ISO_Target_t *	REAL	Desired stress temperature [°C]	320
WLR_ISO_Tb	REAL	Temperature at which Beta is defined [°C]	29
WLR_ISO_V_cool	REAL	Initial trial voltage to measure resistance without heating [V]	0.1
WLR_ISO_Xtype *	INTEGER	Execution type	1
WLR_ISO_XtypeOptions *	STRING[4]	Labels for execution type selections	
WLR_ISO_XtypeSelected *	STRING[1]	Execution type selected	

SYSTEM Tag Variables for KELRES_3_EMR Algorithm

Name	Type	Description	Initial Value
WLR_KELRES_V_cool	REAL	Initial trial voltage to measure resistance without heating [V]	0.1

SYSTEM Tag Variables for TCR_3_EMR Algorithm

Name	Type	Description	Initial Value
WLR_TCR_Lowrtmp *	INTEGER	Lower limit for temperature range [°C]	29
WLR_TCR_Ntemps *	INTEGER	Total number of at-temperatures measurements	4

Name	Type	Description	Initial Value
WLR_TCR_Soak *	REAL	Soak time at temperature [sec]	300
WLR_TCR_Upprtmp *	INTEGER	Upper limit for temperature range [°C]	100
WLR_TCR_V_cool	REAL	Initial trial voltage to measure resistance without heating [V]	0.1

SYSTEM Tag Variables to Link TCR_3_EMR to ISO_4_EMR

Name	Type	Description	Initial Value
WLR_TCR_Beta	REAL	Linear temperature coefficient of resistance [1/°C]	0.0035
WLR_TCR_LinkBeta	INTEGER	Linking Beta value or not	0
WLR_TCR_LinkOptions *	STRING[2]	Labels for selections	
WLR_TCR_LinkRob	INTEGER	Linking Rob value or not	0
WLR_TCR_LinkSelected *	STRING[2]	Parameters selected	
WLR_TCR_Rob	REAL	Resistance measured at Lowrtmp [ohm]	100

SYSTEM Tag Variables for JRAMP_3_CAP Algorithm

Name	Type	Description	Initial Value
WLR_JRAMP_Area *	REAL	Area of active region [cm^2]	0
WLR_JRAMP_Bty *	STRING	Dopant type of bulk region. “N” or “P”	“N”
WLR_JRAMP_BtySelected	STRING[1]		
WLR_JRAMP_F	REAL	Current increase factor	1.25
WLR_JRAMP_Fcrit *	REAL	Voltage failure criteria [%/100]	0.9
WLR_JRAMP_Imax *	REAL	Maximum ramp current [A]	0.001
WLR_JRAMP_Io	REAL	Initial ramp current (pre/post test current)[A]	0.000001
WLR_JRAMP_Per *	REAL	Perimeter of active region [cm]	0
WLR_JRAMP_Ramp_rate	REAL	Current ramp rate [Decade/sec]	2
WLR_JRAMP_Testcon	INTEGER	Test in accumulation (1), or in inversion (2)	1
WLR_JRAMP_Tty *	STRING	Top electrode type. “N”, “P”, or “Al”	“N”
WLR_JRAMP_TtySelected	STRING[1]		
WLR_JRAMP_Vcomp	REAL	Voltage compliance of current ramp [V]	100
WLR_JRAMP_Vuse *	REAL	Pre and post test compliance voltage [V]	3.3

SYSTEM Tag Variables for JTDDB_3_CAP Algorithm

Name	Type	Description	Initial Value
WLR_JTDDB_Area *	REAL	Area of active region [cm^2]	0
WLR_JTDDB_Bty *	STRING	Dopant type of bulk region. “N” or “P”	“N”
WLR_JTDDB_BtySelected	STRING[1]		
WLR_JTDDB_Fcrit *	REAL	Voltage failure criteria [%/100]	0.9
WLR_JTDDB_Io	REAL	Pre/post test current failure criteria [A]	0.000001
WLR_JTDDB_Jstress *	REAL	Stressing current density [A/cm^2]	1
WLR_JTDDB_Per *	REAL	Perimeter of active region [cm]	0
WLR_JTDDB_Testcon	INTEGER	Test in accumulation (1), or in inversion (2)	1
WLR_JTDDB_Time_max *	REAL	Maximum time to wait for breakdown [sec]	300
WLR_JTDDB_Tty *	STRING	Top electrode type. “N”, “P”, or “Al”	“N”
WLR_JTDDB_TtySelected	STRING[1]		
WLR_JTDDB_Vcomp	REAL	Voltage compliance for current stress [V]	24
WLR_JTDDB_Vuse *	REAL	Pre and post test voltage [V]	3.3

SYSTEM Tag Variables for MBLION_SHS Algorithm

Name	Type	Description	Initial Value
WLR_MBLION_Beta *	REAL	Temperature coefficient of resistance [1/°C]	0.00355
WLR_MBLION_Chuck_tmp	REAL	Temperature of thermochuck [°C]	27
WLR_MBLION_Dirs	INTEGER	Sweep direction. 1, 2 or 3.	1
WLR_MBLION_Idth	REAL	Drain current	0.0000001
WLR_MBLION_Tb *	REAL	Temperature at which Beta is defined [°C]	27
WLR_MBLION_Temp *	REAL	Temperature of device [°C]	400
WLR_MBLION_Time	REAL	Stress time [sec]	
WLR_MBLION_Vds	REAL	Drain-Source voltage [V]	
WLR_MBLION_Vgmax *	REAL	Maximum gate voltage [V]	100
WLR_MBLION_Vgmin *	REAL	Minimum gate voltage [V]	0
WLR_MBLION_Vgstrs	REAL	Gate stress voltage [V]	30

SYSTEM Tag Variables for VRAMP_3_CAP Algorithm

Name	Type	Description	Initial Value
WLR_VRAMP_Area *	REAL	Area of active region [cm^2]	0
WLR_VRAMP_Bty *	STRING	Dopant type of bulk region. “N” or “P”	“N”
WLR_VRAMP_BtySelected	STRING[1]		
WLR_VRAMP_Icomp	REAL	Compliance limit of sweep [A]	0.1
WLR_VRAMP_Icrit	REAL	Lowest current level of search [A]	0.0000000001
WLR_VRAMP_Io	REAL	Pre/post test leakage current [A]	0.000001
WLR_VRAMP_Per *	REAL	Perimeter of active region [cm]	0
WLR_VRAMP_Ramp_rate	REAL	Electric field ramp rate [MV/cm sec]	1.0
WLR_VRAMP_Testcon	INTEGER	Test in accumulation (1), or in inversion (2)	1
WLR_VRAMP_Tox *	REAL	Design oxide thickness [Angstrom]	75
WLR_VRAMP_Tty *	STRING	Top electrode type. “N”, “P”, or “Al”	“N”
WLR_VRAMP_TtySelected	STRING[1]		
WLR_VRAMP_Vmax	REAL	Gate ending voltage [V]	19
WLR_VRAMP_Vstart	REAL	Gate start voltage [V]	3.3
WLR_VRAMP_Vstep	REAL	Gate bias step size [V]	0.075
WLR_VRAMP_Vuse *	REAL	Post test voltage [V]	3.3

SYSTEM Tag Variables for VTDDB_3_CAP Algorithm

Name	Type	Description	Initial Value
WLR_VTDDB_Area *	REAL	Area of active region [cm^2]	0
WLR_VTDDB_Bty *	STRING	Dopant type of bulk region. “N” or “P”	“N”
WLR_VTDDB_BtySelected	STRING[1]		
WLR_VTDDB_Estress *	REAL	Field at which capacitor is stressed [MV/cm]	13
WLR_VTDDB_Icomp	REAL	Current compliance of SMU [A]	0.01
WLR_VTDDB_Io	REAL	Pre and post test current failure criteria [A]	0.000001
WLR_VTDDB_Per *	REAL	Perimeter of active region [cm]	0
WLR_VTDDB_Testcon	INTEGER	Test in accumulation (1), or in inversion (2)	1
WLR_VTDDB_Time_max *	REAL	Maximum time to wait for breakdown [sec]	300
WLR_VTDDB_Tox *	REAL	Design oxide thickness [Angstrom]	75
WLR_VTDDB_Tty *	STRING	Top electrode type. “N”, “P”, or “Al”	“N”
WLR_VTDDB_TtySelected	STRING[1]		
WLR_VTDDB_Vuse *	REAL	Pre and post test voltage [V]	3.3

SYSTEM Tag Variables for HCI_3_MOS Algorithm

Name	Type	Description	Initial Value
WLR_HCI_File_in *	STRING	HCI input file used for the test	“pretest.hciinput”

SYSTEM Tag Variables for BEM_3_EMR Algorithm

Name	Type	Description	Initial Value
WLR_BEM_Alpha	REAL	Slope of T_peak vs T_avg	1
WLR_BEM_Beta	REAL	Temperature coefficient of resistance [1/°C]	0.00355
WLR_BEM_Chktmp	REAL	Ambient temperature of chuck [°C]	29
WLR_BEM_E_a	REAL	Activation energy [eV]	0.75
WLR_BEM_L_s	REAL	Test structure length [cm]	0.08
WLR_BEM_Maxro	REAL[3]	Maximum Del_ro change points [%]	
WLR_BEM_Nstep	INTEGER	Number of temperature steps	100
WLR_BEM_Rob	REAL	Resistance measured at Tb [ohm]	100
WLR_BEM_Tb	REAL	Temperature at which Beta is defined [°C]	29
WLR_BEM_Tend	REAL	Ramp end temperature [°C]	350
WLR_BEM_Tiramp	REAL	Total ramp time [sec]	100
WLR_BEM_Tmaxq	REAL	Maximum temperature used to measure Q [°C]	150
WLR_BEM_Tstrt	REAL	Ramp start temperature [°C]	200
WLR_BEM_Vcl	REAL	Initial trial voltage to measure resistance without heating [V]	0.1
WLR_BEM_Xtype	INTEGER	Execution type	1

SYSTEM Tag Variables for HFCV_3_CAP Algorithm

Name	Type	Description	Initial Value
WLR_HFCV_Calc	STRING	Run analysis calculations? “Y” or “N”	“Y”
WLR_HFCV_Ccorr	INTEGER	Cable length [m]	4
WLR_HFCV_Chktmp	REAL	Chuck temperature [°C]	27
WLR_HFCV_Dirswp	INTEGER	Sweep direction. 1, 2, or 3	3
WLR_HFCV_Freq	REAL	Test frequency [Hz]	1000000
WLR_HFCV_Integ	INTEGER	Integration time. 1 Short, 2 medium, or 3 long	2
WLR_HFCV_Level	REAL	Test signal level [Vrms]	0.025
WLR_HFCV_O_cor	STRING	Open correction. “Y” or “N”	“N”

Name	Type	Description	Initial Value
WLR_HFCV_Range	REAL	Measurement range [ohm]	0
WLR_HFCV_S_cor	STRING	Short correction. “Y” or “N”	“N”
WLR_HFCV_Start	REAL	Sweep start voltage [V]	3.3
WLR_HFCV_Step	REAL	Sweep step voltage [V]	0.1
WLR_HFCV_Stop	REAL	Sweep stop voltage [V]	3.3
WLR_HFCV_Tdelay	REAL	Delay time between each step [sec]	0.05

SYSTEM Tag Variables for PDQ-WLR GUI Disable Environment

Name	Type	Description	Initial Value
Maxro	REAL[3]	Parameter for ISO_4_EMR_XL algorithm.	
Ntimes	INTEGER	Parameters for HCSTRESS_MOS, LIFETIME_MOS algorithms. See *“Agilent PDQ-WLR User’s Guide”*.	
Pa	REAL[100]		
Times	REAL[100]		

Other Additional SYSTEM Tag Variables

Name	Type	Description	Initial Value
WLR_BEGIN	INTEGER	Used to find test items selected	1
WLR_CSV	STRING	CSV file output enable or disable	
WLR_DB_DirPath *	STRING	Directory path of database. Initial value: “/var/opt/WLR/database/data/measured/”	
WLR_DB_FileName *	STRING	File name of .dat file. Initial value: “default.dat”	
WLR_DB_OnOff	STRING	database output enable or disable	“ON”
WLR_DB_Options	STRING[2]	Selections of database output	
WLR_DB_Selected	STRING[1]	database output selected. ON or OFF	
WLR_DieSelected	STRING[20]	Test dice selected	
WLR_ErrHeight	INTEGER	Used to display PDQ-WLR Error panel	20
WLR_ErrMessage	STRING	Used to display PDQ-WLR Error panel	
WLR_ErrPosX	INTEGER	Used to display PDQ-WLR Error panel	10
WLR_ErrPosY	INTEGER	Used to display PDQ-WLR Error panel	30
WLR_ErrWidth	INTEGER	Used to display PDQ-WLR Error panel	80
WLR_GOI_BtyOptions	STRING[3]	Selections of Bty value for GOI algorithms	

Name	Type	Description	Initial Value
WLR_GOI_TtyOptions	STRING[3]	Selections of Tty value for GOI algorithms	
WLR_GRAPH	STRING	Xgraph display/save selection	
WLR_GUI_Initial	STRING	Initial value of GUI display mode	"Enable"
WLR_GUI_OnOff *	STRING[2]	Selections of GUI display mode	
WLR_GUI_Selected *	STRING[1]	GUI display mode selected	
WLR_I	INTEGER	Counter used in several specifications	1
WLR_J	INTEGER	Counter used in several specifications	1
WLR_Nitem	INTEGER	Number of test items	20
WLR_Nselected	INTEGER	Number of test items selected	20
WLR_Plot	STRING	For all algorithms. Plot$ parameter	
WLR_PlotOptions *	STRING[4]	Selections of data output options	
WLR_PlotSelected *	STRING[4]	Data output options selected.	
WLR_TCS_ActionList	STRING[20]	List of Test Setup panels available	
WLR_TCS_ActionName	STRING	Name of action spec to call panel spec	
WLR_TCS_Flag	INTEGER	Flag if Test Setup panels are disabled	0
WLR_TCS_Options *	STRING[5]	Selections of panal display option	
WLR_TCS_PanelName	STRING	Used to specify new panel spec name	
WLR_TCS_Selected *	STRING[1]	Panel display option selected	
WLR_TCS_Swap	INTEGER	Specifies how to open/swap/close panel	1
WLR_TCS_Title	STRING	Used to specify title of new panel	
WLR_TCS_Var	REAL[10]	Values of entry fields on new panel	
WLR_TCS_VarLabel	STRING[10]	Labels of entry fields on new panel	
WLR_TCS_VarName	STRING[20]	Just defined in SYSTEM tag spec	
WLR_TCS_VarNum	INTEGER	Just defined in SYSTEM tag spec	5
WLR_TestFlag	INTEGER[20]	Used to find test items selected	
WLR_TestLabel *	STRING[20]	For WLR_TEST_SELECT panel. Selections of test items	
WLR_TestSelected *	STRING[20]	For WLR_TEST_SELECT panel. Test items selected	
WLR_TS_row	INTEGER	Number of test items on Test Select panel	11
WLR_VRAMP_Explains *	STRING	For WLR_GOI_VRAMP panel. Messages appeared on GOI/VRAMP panel	

Configuration File

The PDQWLR_PLG plug framework uses the PDQWLR_PLG.cf configuration file to call the PDQ-WLR Environment Setup and the PDQ-WLR Option Setup from the HPSTD framework execution flow. The file also defines the default values of some of the variables defined in the plug framework. Differences between the PDQWLR_PLG.cf and the HPSTD framework configuration file are listed below:

- To call the PDQ-WLR Environment:

  Sets the following parameters in the configuration file:

  ```
  MNU_UTIL2_LABEL:PDQ-WLR Environment
  MNU_UTIL2_ACT:WLR_ENVS
  ```

- To call the PDQ-WLR Option Setup:

  Sets the following parameters in the configuration file:

  ```
  MNU_OPT1_LABEL:PDQ-WLR Options
  MNU_OPT1_ACT:WLR_OPTIONS
  ```

- To define initial values:

  Adds the following parameters to the configuration file to define the default values of the variables used in the PDQWLR_PLG plug framework:

  ```
  WLR_DB_DirPath:/var/opt/WLR/data/database/measured/
  WLR_DB_FileName:default.dat
  WLR_GUI_Initial:Enable
  ```

  The meaning of the variables is explained below:

`WLR_DB_DirPath`	Directory path of database.
`WLR_DB_FileName`	Name of test result data file stored in database.
`WLR_GUI_Initial`	PDQ-WLR GUI display environment. If this variable is set to Enable, the framework displays operation panels added to the PDQWLR_PLG plug framework.

- Other changes:

  The default value of the following parameter is changed as follows. This disables the lot summary report after the test.

  ```
  RPT_LOTSTAT_USE:0
  ```

5 PDQWLR_TPT Sample Test Plan

The Agilent PDQ-WLR software provides a sample test plan, PDQWLR_TPT.tpl. This chapter describes the PDQWLR_TPT test plan, and consists of the following sections:

- “Probe Specification”

  Explains the probe specifications defined in the sample test plan.

- “Wafer Specification”

  Explains the wafer specification defined in the sample test plan.

- “Die Specification”

  Lists the die specifications defined in the sample test plan.

- “Test Specification”

  Lists the test specifications defined in the sample test plan.

To open the test plan file, open the SPECS NAVIGATOR window and click Test Plan Open. The Open Test Plan dialog box opens.

NOTE

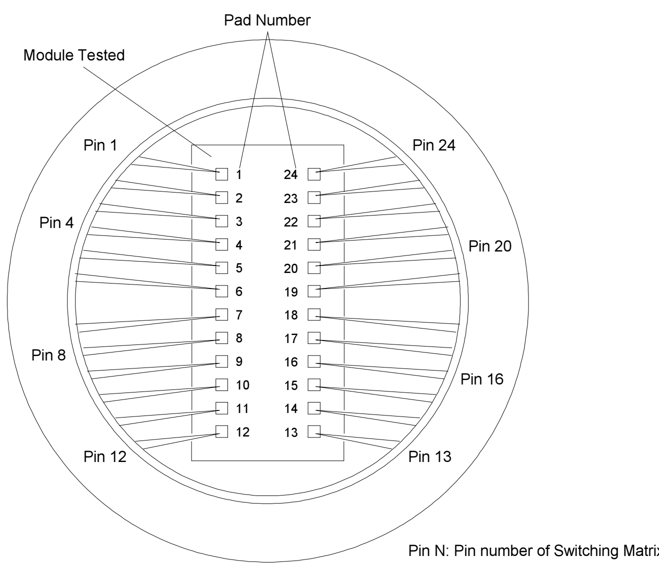
After installing the PDQ-WLR software, the PDQWLR_TPT test plan is stored in the /opt/SPECS/demo directory.

Probe Specification

The probe specification defines the relationship between the pad number of the module tested and the pin number of the switching matrix. The following two probe specifications are defined in the PDQWLR_TPT sample test plan. The definition of both specifications is the same, only the specification name is different.

- PDQ_WLR_12x2
- PDQ_WLR_2x12

Both specifications define the probing information shown below.

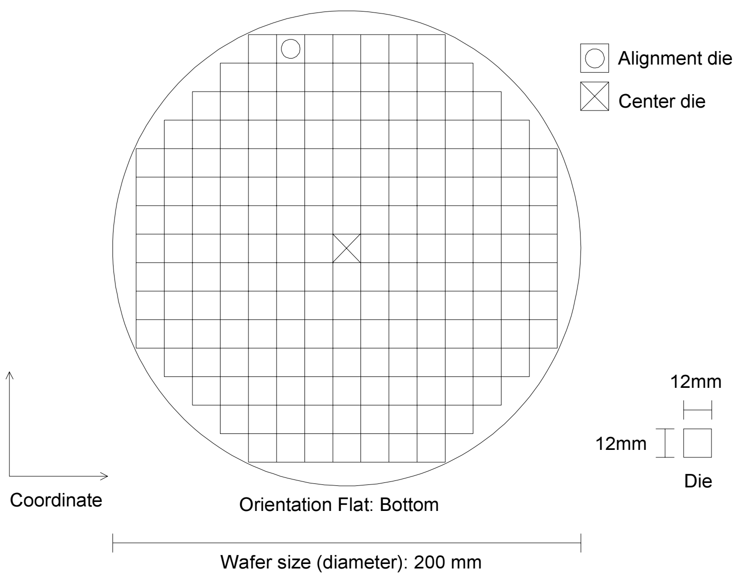


Wafer Specification

The wafer specification registers the attribute information and the dice on the wafer being tested. The PDQWLR_TPT sample test plan defines the PDQ_WLR wafer specification.

The wafer specification attribute defines the following attribute information. See figure below.

- Wafer size (diameter): 200 mm
- Die step index size: 12 mm (X), 12 mm (Y)
- Orientation flat: Bottom (FLAT=180)
- Alignment die index: (-2,7)
- Center die index: (0,0)
- Coordinate: see below (COORDINATE=1)



The wafer specification body defines the following die names with an X-Y index of (0, 0). For the actual test, you must enter the correct values of the X-Y index.

- EM_TCR

  Die for the EM_TCR test specification.
- EM_ISO

  Die for the EM_ISO test specification.
- EM_KELRES

  Die for the EM_KELRES test specification.
- GOI_JRAMP

  Die for the GOI_JRAMP test specification.
- GOI_JTDDB

  Die for the GOI_JTDDB test specification.
- GOI_MBLION_SHS

  Die for the GOI_MBLION_SHS test specification.
- GOI_VRAMP

  Die for the GOI_VRAMP test specification.
- GOI_VTDDB

  Die for the GOI_VTDDB test specification.
- MOS_HCI

  Die for the MOS_HCI test specification.

Die Specification

The die specification specifies the module information for the die tested. The names of the die specifications to test must be defined in the wafer specification. The sample test plan defines the following die specifications.

- EM_TCR

  Die specification for the EM_TCR test specification.
- EM_ISO

  Die specification for the EM_ISO test specification.
- EM_KELRES

  Die specification for the EM_KELRES test specification.
- EM_BEM

  Die specification for the EM_BEM test specification.
- GOI_JRAMP

  Die specification for the GOI_JRAMP test specification.
- GOI_JTDDB

  Die specification for the GOI_JTDDB test specification.
- GOI_MBLION_SHS

  Die specification for the GOI_MBLION_SHS test specification.
- GOI_VRAMP

  Die specification for the GOI_VRAMP test specification.
- GOI_VTDDB

  Die specification for the GOI_VTDDB test specification.
- GOI_HFCV

  Die specification for the GOI_HFCV test specification.
- MOS_HCI

  Die specification for the MOS_HCI test specification.

The die specifications define the module names shown below with X=0 [um] and Y=0 [um] dimensions. For the actual test, you must enter the actual values of the dimensions. The name of the modules tested must also be defined in the test specification.

EM_TCR, EM_ISO, EM_KELRES, and EM_BEM:

Module Name	Description
MinWidth_AM1	Module EM_A_M1
MinWidth_CBR1	Module EM_CBR_M1
GrnBndry_BM1	Module EM_B_M1
ViaVoid_A	Module EM_VIA_A
ContactP	Module EM_CONT_P
ContactN	Module EM_CONT_N
MetalStep_A1	Module EM_STEP_A_M1
MetalStep_B1	Module EM_STEP_B_M1
ThinOxd_A	Module EM_T_A_M1
ThinOxd_B	Module EM_T_B_M1
ThinOxd_CBR	Module EM_T_CBR_M1

GOI_JRAMP, GOI_JTDDB, GOI_VRAMP, GOI_VTDDB, and GOI_HFCV:

Module Name	Description
LogScaleArea_AN	Module CAP_A_N
LogScaleArea_AP	Module CAP_A_P
EdgeCap_FIAN	Module CAP_FIA_N
EdgeCap_FIAP	Module CAP_FIA_P
EdgeCap_TRANSN	Module CAP_TRANS_N
EdgeCap_TRANSP	Module CAP_TRANS_P
IntLevel_IDF	Module CAP_ID_F
IntLevel_IDFW	Module CAP_ID_FW
IntLevel_IDN	Module CAP_ID_N
IntLevel_IDNE	Module CAP_ID_NE

GOI_MBLION_SHS:

Module Name	Description
MobileIon_AN	Module CAP_A_N
MobileIon_AP	Module CAP_A_P

MOS_HCI:

Module Name	Description
HCXTR_N	Module HCXTR_N
HCXTR_P	Module HCXTR_P
HCXTRV_N	Module HCXTRV_N
HCXTRV_P	Module HCXTRV_P
HCXTROT	Module HCXTROT

Test Specification

The test specification specifies the modules and devices to be tested, the test items (algorithms), and the pad numbers of the device terminals. The sample test plan defines the following test specifications relative to the die specifications as shown below.

Test Specification	Die Specification	Algorithm defined
EM_TCR	EM_TCR	TCR_3_EMR_XL
EM_ISO	EM_ISO	ISO_4_EMR_XL
EM_KELRES	EM_KELRES	KELRES_3_EMR_XL
EM_BEM	EM_BEM	BEM_3_EMR_X
GOI_JRAMP	GOI_JRAMP	JRAMP_3_CAP_XL
GOI_JTDDB	GOI_JTDDB	JTDDB_3_CAP_XL
GOI_MBLION_SHS	GOI_MBLION_SHS	MBLION_SHS_XL
GOI_VRAMP	GOI_VRAMP	VRAMP_3_CAP_XL
GOI_VTDDB	GOI_VTDDB	VTDDB_3_CAP_XL
GOI_HFCV	GOI_HFCV	HFCV_3_CAP_XL
MOS_HCI	MOS_HCI	HCI_3_MOS_XL

The module names defined in the test specifications must also be defined in the relative die specification. Only one test algorithm can be defined for the module.

The test specifications also use the SYSTEM tag variables to set the algorithm input parameters. See Chapter 4 for the variables defined in the PDQWLR_PLG plug framework and are available for algorithms.