Logic Analyzer Modules

TLA7BBx Series

The TLA Series logic analyzer modules offer the highest performance for today's demanding applications.

Breakthrough Solutions for Real-time Digital Systems Analysis

Today's digital design engineers face daily pressures to speed new products to the marketplace. The TLA7BBx Series logic analyzer modules answer the need with breakthrough solutions for the entire design team, providing the ability to quickly monitor, capture and analyze real-time digital system operation in order to debug, verify, optimize and validate digital systems.

Hardware developers, hardware/software integrators and embedded software developers will appreciate the range of capabilities of the TLA7BBx Series logic analyzer modules. Its broad feature set includes capturing and correlating elusive hardware and software faults; providing simultaneous state, high-speed timing and analog analysis through the same probe; using deep state acquisition to find the cause of complex problems; real-time, non-intrusive software execution tracing that correlates to source code and to hardware events; and non-intrusive connectorless probing.

The TLA7BBx Series logic analyzer modules offer Tektronix' breakthrough MagniVu technology for providing high-speed sampling (up to 50 GHz) that dramatically changes the way logic analyzers work and enables them to provide startling new measurement capabilities.

The TLA7BBx modules offer high-speed state synchronous capture, high-speed timing capture and analog capture through the same set of probes. They capitalize on MagniVu technology to offer up to 20 ps timing on all channels, glitch and setup/hold triggering and display and timestamp that is always on at up to 20 ps resolution.

Features & Benefits

68/102/136 channel logic analyzers with up to 64 Mb depth

MagniVu™ acquisition technology provides up to 20 ps (50 GHz) timing resolution to find and measure elusive timing problems quickly

Up to 156 ps (6.4 GHz)/256 Mb deep memory timing analysis

Up to 1.4 GHz clock with up to 3.0 Gbs data with a data valid window of 180 ps for state acquisition analysis of high-performance synchronous buses

Simultaneous state, high-speed timing, and analog analysis through the same probe pinpoints elusive faults

Glitch and setup/hold triggering and display finds and displays elusive hardware problems

Transitional storage extends the signal analysis capture time for signals that transition infrequently

Trace problems from symptom back to root cause in real-time across multiple modules by viewing time-correlated data in a wide variety of display formats

Compatible with the wide assortment of P6800/P6900 series probes for both single-ended and differential signals that provide capacitive loading down to 0.5 pF

Purchase only the state speed and record length needed now and later upgrade with PowerFlex

Broad processor and bus support

Applications

Hardware debug and verification

Processor/bus debug and verification including source synchronous clocking

Embedded software integration, debug and verification

Tektronix®

Characteristics

General Characteristics

Number of Channels (all channels are acquired including clocks)	
TLA7BB2	68 channels (4 are clock channels)
TLA7BB3	102 channels (4 are clock and 2 are qualifier channels)
TLA7BB4	136 channels (4 are clock and 4 are qualifier channels)
Channel Grouping	No limit to number of groups or number of channels per group (all channels can be reused in multiple groups)
Module "Merging"	Up to five 68 channel, 102 channel or 136 channel modules can be "merged" to make up to a 680 channel module Merged modules exhibit the same depth as the lesser of the five individual modules Word/setup-and-hold/glitch/transition recognizers span all five modules Range recognizers limited to three module merge Only one set of clock connections is required
Time Stamp	54-Bits at 20 ps resolution (>4 days duration)
Clocking/Acquisition Modes	Asynchronous and Synchronous 20 ps (50 GHz) MagniVu, high-speed timing is available simultaneous with all modes
Number of Mainframe Slots Required per TLA Series Module	2

Input Characteristics (with P68xx or P69xx probes)

Capacitive Loading	0.5 pF clock/data (P69xx)
	<0.7 pF clock/data (P68xx)
	(1.0 pF for P6810 when 8 channel podlet grouper is used)
Threshold Selection Range	From –2.0 V to +4.5 V in 5 mV increments. Threshold presets include TTL (1.5 V), CMOS (2.5 V), ECL (–1.3 V), PECL (3.7 V), LVPECL (2.0 V), LVCMOS 1.5 V (0.75 V), LVCMOS 1.8 V (0.9 V), LVCMOS 2.5 V (1.25 V), LVCMOS 3.3 V (1.65 V), LVDS (0 V) and user-defined
Threshold Selection Channel Granularity	Separate selection for each of the clock/qualifier and individual channels
Threshold Accuracy (including probe)	±(35 mV + 1%)
Input Voltage Range	
Operating	–2.5 V to 5.0 V
Nondestructive	±15 V
Minimum Input Signal Swing	200 mV (single-ended)
	$\bar{V}_{MAX} - V_{MIN} > 100$ mV (differential)
Input Signal Minimum Slew Rate	200 mV/ns typical

State Acquisition Characteristics (with P68xx or P69xx probes)

State Acquisition

Configuration	Full Channel	Half Channel
750 MHz Standard	750 MHz/750 Mbs (1 sample/clock) 750 MHz/1.5 Gbs (2 samples/clock)	750 MHz/3 Gbs (4 samples/clock)
1.4 GHz Optional	1.4 GHz/1.4 Gbs (1 sample/clock)	1.4 GHz/2.8 Gbs (2 samples/clock)
State Memory Depth with Timestamps (half/full channels)	4/2 Mb, 8/4 Mb, 16/8 Mb, 32/16 Mb, 64/32 Mb, 128/64 Mb per channel	
Setup and Hold Time Selection Range	From 15 ns before, to 7.5 ns after clock edge in 20 ps increments Range may be shifted towards the setup region by 0 ns [+7.5, –7.5] ns, 2.5 ns [+10, –5] ns or 7.5 ns [+15, 0] ns	
Setup-and-hold Window		
Single Channel	180 ps typical	
Minimum Clock Pulse Width	200 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880), 250 ps (P6810)	
Demux Channel Selection	Channels can be demultiplexed to other channels through user interface with 8 channel granularity	

Timing Acquisition Characteristics (with P68xx or P69xx probes)

MagniVu™ Timing – 20 ps max, adjustments to 40 ps, 80 ps, 160 ps, 320 ps and 640 ps.

MagniVu Timing Memory Depth – 128 Kb per channel, with adjustable trigger position.

Deep Timing Resolution (quarter/half/full channels) – 156.25 ps/312.5 ps/625 ps to 50 ms.

Deep Timing Resolution with Glitch Storage Enabled – 1.25 ns to 50 ms.

Deep Timing Memory Depth (quarter/half/full channels) – 8/4/2 Mb, 16/8/4 Mb, 32/16/8 Mb, 64/32/16 Mb, 128/64/32 Mb, 256/128/64 Mb per channel.

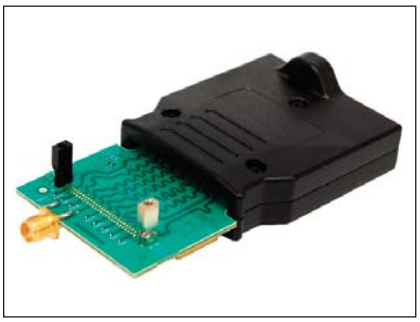
Deep Timing Memory Depth with Glitch Storage Enabled – Half of default main memory depth.

Channel-to-Channel Skew (module + probes)
Before Customer Deskew – +/– 80 ps typical.
After Customer Deskew (See AutoDeskew information below) – +/– 20 ps typical.

Minimum Recognizable Pulse/Glitch Width (single channel) – 200 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880) 250 ps (P6810).

Minimum Detectable Setup/Hold Violation – 40 ps.

Minimum Recognizable Multi-channel Trigger Event – Sample period + channel-to-channel skew.



AutoDeskew and Customer Deskew Fixture

Tektronix recommends **AutoDeskew,** a standard feature available within the TLA Application, for deskewing probe channels and setting the sample point for synchronous applications. However, for tight time alignment in both synchronous and asynchronous applications (including MagniVu™), Tektronix recommends the **Customer Deskew Fixture.** This is an optional accessory to the TLA7BBx modules that is used to perform a "channel-to-channel deskew" of the probes connected to the TLA7BBx module to ensure tight time alignment between all channels across all probes. Two different fixtures are available:

– Customer Deskew Fixture for P6800 Series Probes

– Customer Deskew Fixture for P6900 Series Probes

For ordering details, please see the Ordering Information section.

Analog Acquisition Characteristics (with P68xx or P69xx probes)

Bandwidth	3 GHz typical
Attenuation	10x, ±1%
Offset and Gain (Accuracy)	±50 mV, +/–2% of Signal Amplitude
Channels Demultiplexed	4
Run/Stop Requirements	None, analog outputs are always active
iView™ Analog Outputs	Compatible with any supported external TDS oscilloscope
iView Analog Output BNC Cables	Four (4) low loss, 10x, 36-in

Trigger Characteristics

Independent Trigger States	16
Maximum Independent If/then Clauses per State	16
Maximum Number of Events per If/then Clause	8
Maximum Number of Actions per If/then Clause	8
Maximum Number of Trigger Events	26 (2 counter/timers plus any 24 other resources)
Number of Word Recognizers	24
Number of Transition Recognizers	24
Number of Range Recognizers	8
Number of Counter/Timers	2
Trigger Event Types	Word, group, channel, transition, range, anything, counter value, timer value, signal, glitch, setup-and-hold violation, snapshot
Trigger Action Types	Trigger module, trigger all modules, trigger main, trigger MagniVu, store, don't store, start store, stop store, increment counter, decrement counter, reset counter, start timer, stop timer, reset timer, snapshot current sample, goto state, set/clear signal, do nothing
Maximum Triggerable Data Rate	3.0 Gb/s
Trigger Sequence Rate	DC to 800 MHz (1.25 ns)
Counter/Timer Range	48 bits each (~4 days at 1.25 ns)
Counter Rate	DC to 800 MHz (1.25 ns)
Timer Clock Rate	800 MHz (1.25 ns)
Counter/Timer Test Latency	0 ns
Range Recognizers	Double bounded (can be as wide as any group (408 channel max), must be grouped according to specified order of significance)
Setup-and-hold Violation Recognizer	
Setup Time Range	From 7.5 ns before to 7.5 ns after clock edge in 20 ps increments
Hold Time Range	This range may be shifted towards the positive region by 0 ns, 2.5 ns, 5 ns or 7.5 ns
Trigger Position	Any data sample
MagniVu Trigger Position	MagniVu position can be set from 0% to 60% centered around the MagniVu trigger
Storage Control (data qualification)	All, Global (conditional), by state (start/stop), block, by trigger action or transitional. Also force main prefill selection available

Physical Characteristics

Dimensions	mm	in.
Height	262	10.3
Width	61	2.4
Depth	381	15

Weight	kg	lb.
Net	3.1	6.7
Shipping	6.3	13.7

Ordering Information

TLA7BBx Logic Analyzer Modules

TLA7BB2 – 68 channel logic analyzer module, 50 GHz MagniVu timing, 750 MHz state clock, 2 Mb record length. Options for up to 64 Mb depth and/or up to 1.4 GHz state clock.

TLA7BB3 – 102 channel logic analyzer module, 50 GHz MagniVu timing, 750 MHz state clock, 2 Mb record length. Options for up to 64 Mb depth and/or up to 1.4 GHz state clock.

TLA7BB4 – 136 channel logic analyzer module, 50 GHz MagniVu timing, 750 MHz state clock, 2 Mb record length. Options for up to 64 Mb depth and/or up to 1.4 GHz state clock.

Includes: Certificate of calibration, one-year warranty (return to Tektronix) and installation manual.

Note: Probes must be ordered separately.

TLA7BBx Module Options

Base configuration is 2 Mb record length at 750 MHz state clock.

Opt 1S – Increase to 4 Mb Record Length at 750 MHz State Clock.

Opt 2S – Increase to 8 Mb Record Length at 750 MHz State Clock.

Opt 3S – Increase to 16 Mb Record Length at 750 MHz State Clock.

Opt 4S – Increase to 32 Mb Record Length at 750 MHz State Clock.

Opt 5S – Increase to 64 Mb Record Length at 750 MHz State Clock.

Opt 6S – Increase to 2 Mb Record Length at 1.4 GHz State Clock.

Opt 7S – Increase to 4 Mb Record Length at 1.4 GHz State Clock.

Opt 8S – Increase to 8 Mb Record Length at 1.4 GHz State Clock.

Opt 9S – Increase to 16 Mb Record Length at 1.4 GHz State Clock.

Opt AS – Increase to 32 Mb Record Length at 1.4 GHz State Clock.

Opt BS – Increase to 64 Mb Record Length at 1.4 GHz State Clock.

TLA Series Module Upgrades

You can increase the memory depth and state speed of most existing TLA Series logic analyzer modules. You can also install a TLA7BBx logic analyzer module into an existing TLA7012/7016 mainframe. Please refer to the TLA Family Upgrade Guide for further details.

Logic Analyzer Probe Selection Guidelines

A flexible choice of logic analyzer probes is available for use with TLA7BBx modules. Please see the logic analyzer probe data sheets for further information.

TLA7Bxx Customer Deskew Fixture

020-2942-00 – TLA7Bxx Customer Deskew Fixture for P6800 Series Probes.

020-2940-00 – TLA7Bxx Customer Deskew Fixture for P6900 Series Probes.

TLA7BBx Service Options

Opt. CA1 – Provides a single calibration event or coverage for the designated calibration interval, whichever comes first.

Opt. C3 – Calibration Service 3 Years.

Opt. C5 – Calibration Service 5 Years.

Opt. D1 – Calibration Data Report.

Opt. D3 – Calibration Data Report 3 Years (with Option C3).

Opt. D5 – Calibration Data Report 5 Years (with Option C5).

Opt. R3 – Repair Service 3 Years.

Opt. R5 – Repair Service 5 Years.

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For Further Information

Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit **www.tektronix.com**

Product(s) are manufactured in ISO registered facilities.

Product(s) complies with IEEE Standard 488.1-1987, RS-232-C and with Tektronix Standard Codes and Formats.

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