APPLICOS
MEASUREMENT & CONTROL

Hardware Manual

PG24192

DUAL 24BIT PXI ARBITRARY WAVEFORM GENERATOR

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PXI

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1 Introduction

The PG24192 is a two channel high accuracy 24-bit arbitrary waveform generator intended for audio and telecom signal generation. The 24-bit resolution and extremely low noise design ensures a superior dynamic performance. All commonly used audio sample rates are supported. By applying an external clock the user can use any update rate from 1 kHz up to 192 kHz.
The module has analog and digital anti-imaging filters. These filters remove the unwanted out-of-band components caused by the over sampling process. The analog signal path from the two channels are complete separate so the output configuration and the analog filters can be set separate for each channel. Figure 1 shows the functional block diagram from the PG24192.

On the left side of the diagram there is the PXI interface to control the card and the trigger and clock inputs.
The next step is the stimulus memory that is connected to the 24 bit digital to analog converter. In the middle there is the clock and trigger control block, with all the trigger and clock lines connected to it. The attenuator is a digital attenuator and is integrated in the DA converter. After the digital to analog conversion there are three selectable analog filters and a DC offset DAC. This DAC can add a DC offset voltage to the output signal. The last stage is the differential output driver that is connected to the front connectors. On the front is also a external clock- and trigger input.

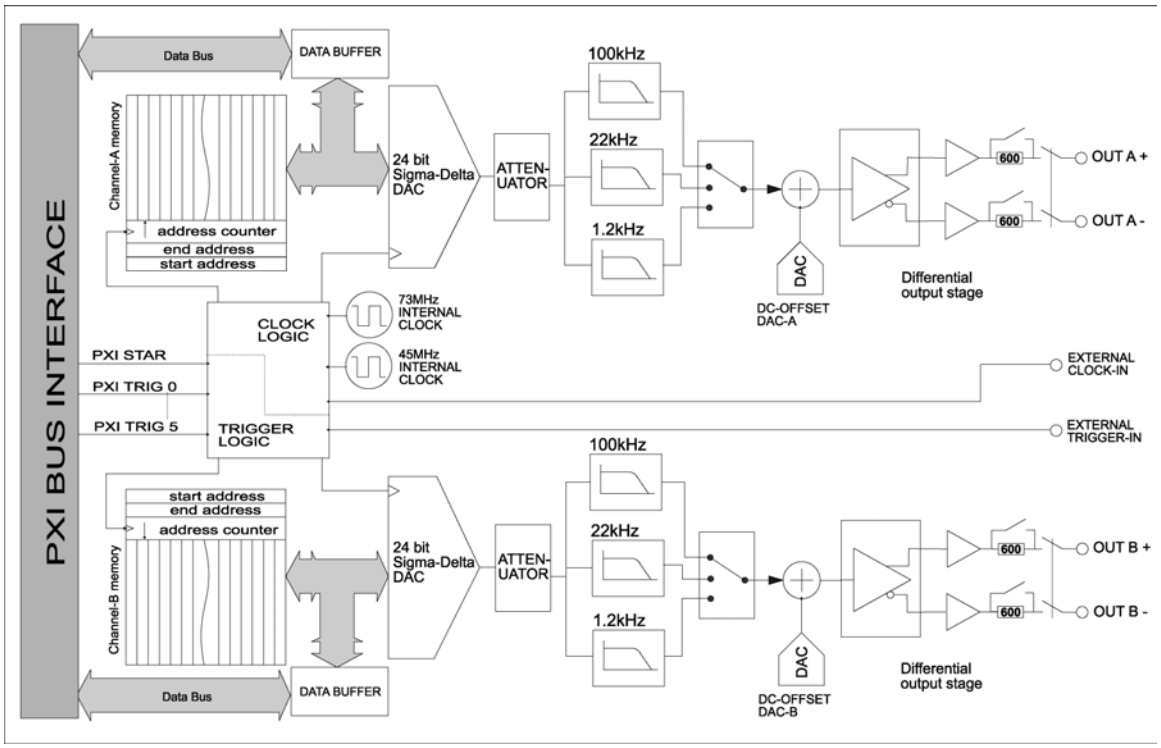

Figure 1 PG24192 functional block diagram

2 Analog circuit

The SMB connectors marked A+, A- ,B+ and B-, on the front of the PG24192, are the analog differential outputs for channel A and channel B. With the output offset DAC a DC mid level can be programmed.
Important: Be sure to tighten the screws at the top and bottom of the front face of the PG24192 for a reliable ground connection.

2.1 Analog output configuration

The PG24192 is equipped with a differential output for each channel. Figure 2 shows the analog output circuit from one of these channels. The analog output impedance is selectable, 600 Ω or low impedance. If the analog output is disconnected, the circuit is disconnected from the output by a mechanical switch. The settings for the output mode is separate for each channel, a different configuration for both channels

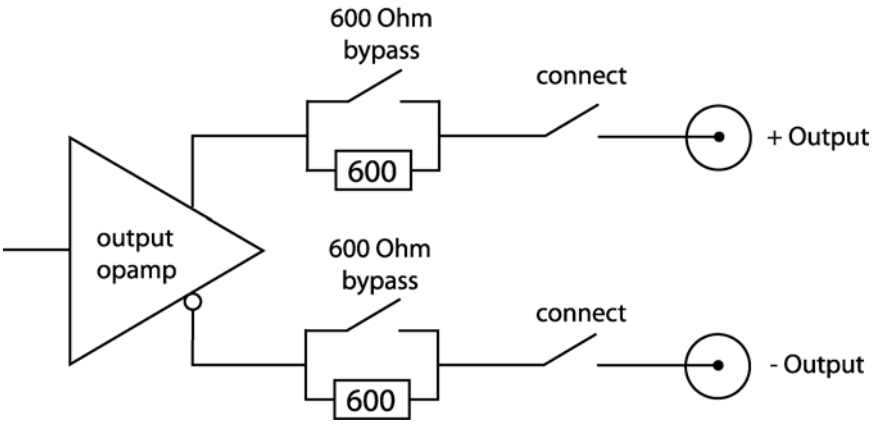

Figure 2 PG24192 analog output circuit

2.2 Output ranges:

The attenuator is a digital attenuator integrated in the delta sigma DA converter
The programmable output ranges is from 0 to 80dB.
A signal with 0 dB attenuation has a peak amplitude of 5V (10Vpp).

Output range	Gain
10Vpp	0dB
1mVpp	80dB

2.3 programmable DC offset source

The programmable DC offset source is a 16 bit DAC with a range of +5Volt to –5Volt.
This 16 bit DAC can add a DC offset voltage to the output signal.

2.4 Analog output filters

The module has three analog low pass filters. These analog filters are required to suppress high frequency noise caused by the over sampling process and to improve the signal to noise ratio. The filters limit the bandwidth of the signal path and is useful for rejecting out of band noise.

Each channel has three selectable 3-pole low pass filters with cutoff frequencies of: 1.2 kHz, 22kHz and 100kHz. Figure 3 shows the typical frequency response from the PG24192 filters.

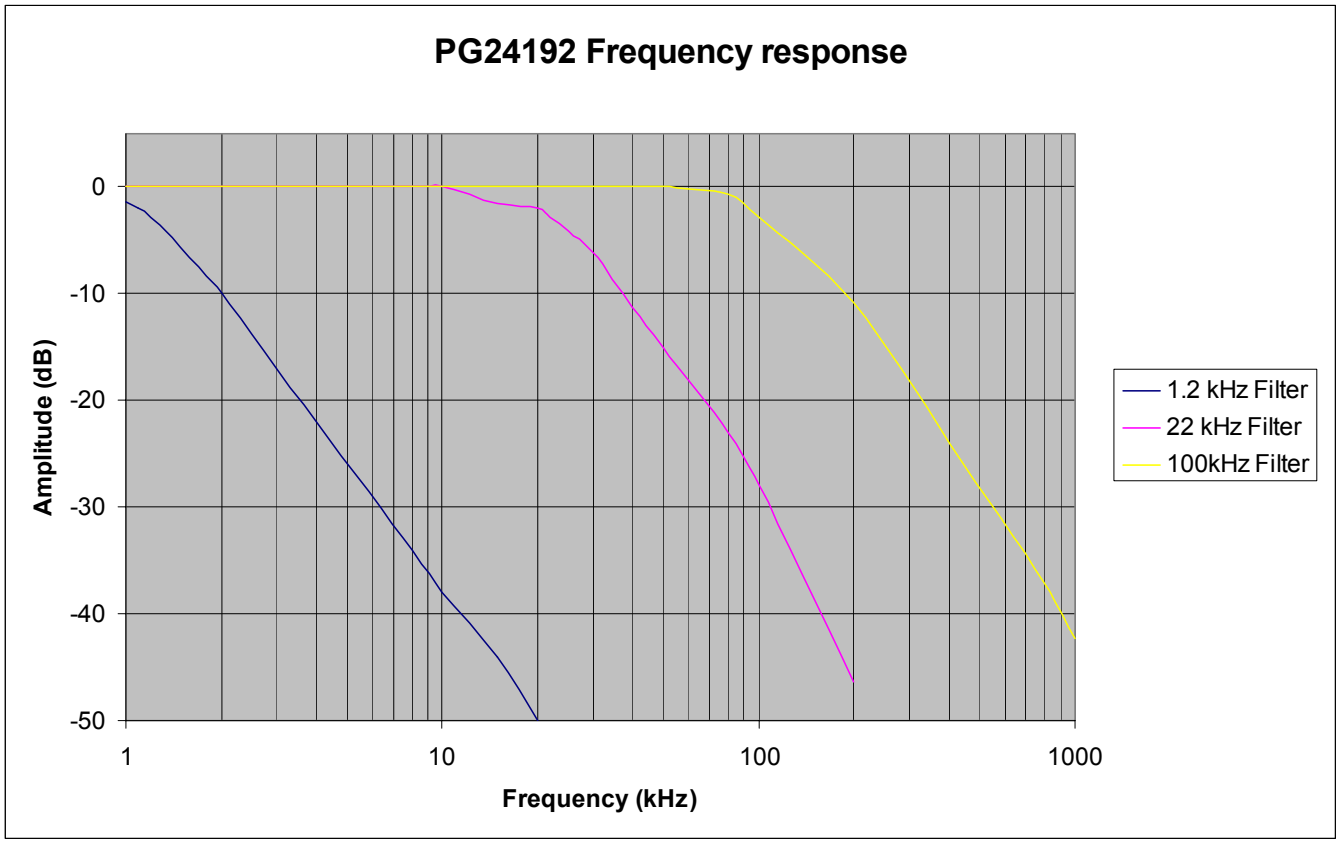

Figure 3 Typical frequency response

3 Clocking

The delta sigma Digital to Analog Converter require an oversampled clock to convert. The oversample clock (master clock) frequency is higher than the sample rate. The PG24192 can run on four different clock sources, two internal and two external clock sources. The internal clock sources are two onboard crystal oscillators from 73.728 MHz and 45.1584 MHz. The external clock sources can be the external clock source, connected to the front SMB connector or the 10 MHz PXI clock provided through the PXI connector.

If the generator is used in combination with the 24 bit waveform digitizer*, it is possible to synchronize both modules. The arbitrary waveform generator passes on the main clock through PXI local bus 0 to the 24 bit waveform digitizer. Notice this is the main clock frequency and not the update frequency from the arbitrary waveform generator. (undivided clock). If this synchronize option is used both modules must be placed next to each other and the waveform generator must be on the left side of the waveform digitizer.

To synchronize the PG24192 to other devices in a measurement system, an external sample clock can be connected on the front panel clock input. The front panel clock input has a 50-Ohm termination.

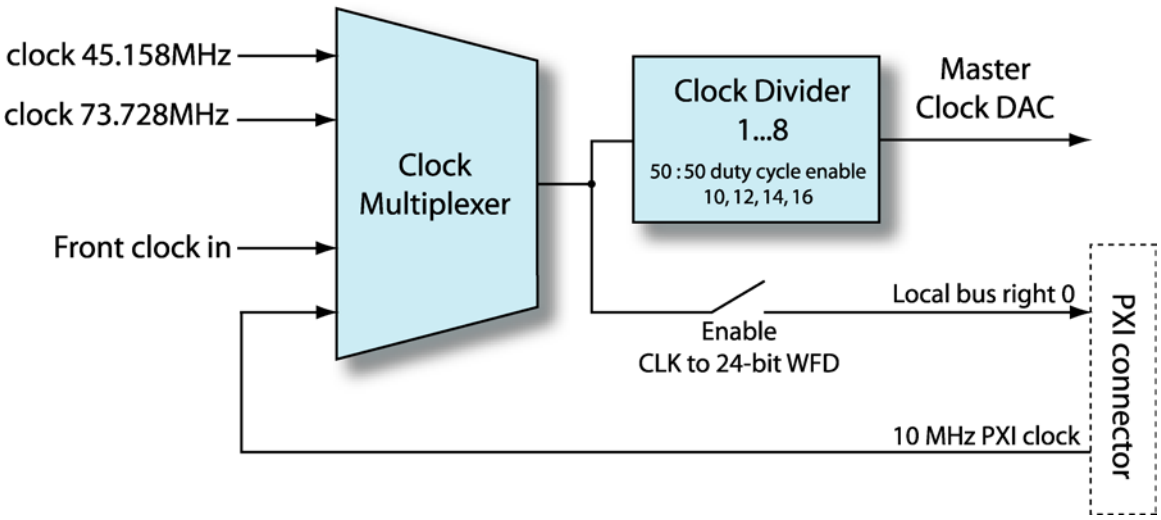

Figure 4 PG24192 clock circuit

3.1 Clock source divider

With the clock source divider, the fixed onboard clock oscillators or the front clock can be divided to the required master clock. The divider is 3 bit so can divide with a maximum of 8. With the 50 percent duty cycle setting enabled these divider ratios are doubled (10, 12, 14 and 16)

3.2 Sample rate

The sample rate not only depend on the clock source frequency and clock source divider, but also of the clock oversampling mode and the filter interpolation mode from the DA converter.
The DAC has three clock oversampling modes, see Table 1.
The interpolation filter is a digital input filter in the DAC.

- When you select a sample rate from 0 to 48 kHz., the filter interpolation mode must be set to 8 times. Possible master clock modes are: 256 -, 512 - and 768 times the sample frequency
- When you select a sample rate from 48 kHz to 96 kHz., the filter interpolation mode must be set to 4 times. Possible master clock modes are: 128 -, 256 - and 384 times the sample frequency
- When you select a sample rate from 96 kHz to 192 kHz., the filter interpolation mode must be set to 2 times. Possible master clock modes are: 64 -, 128 - and 192 times the sample frequency

f sample = 0 to 48 kHz	f sample = 48 to 96 kHz	f sample 96 to192 kHz
filter interpolation 8x	filter interpolation 4x	filter interpolation 2x
256 x f sample	128 x f sample	64 x f sample
512 x f sample	256 x f sample	128 x f sample
768 x f sample	384 x f sample	192 x f sample

Table 1 Maximum clock frequencys

The final sample rate depend on the Clock source, the clock divider and the DAC operation mode. The sample frequency can be derived by the following formula :

$$f_{sample} = \frac{f_{clock}}{(a \div n) \cdot x}$$

f_{clock} = Clock source frequency
a = Clock operation mode : 256, 512 or 768
n = Interpolation mode : n = 1 at Interpolation 8x
n = 2 at Interpolation 4x
n = 4 at Interpolation 2x
x = Clock divider programmed by the user, n = 0 to 16

Here some examples from common used sample rates.

Sample Rate (kHz)	Clock Source (MHz)	Clock source divider	Master clock mode	Interpolation mode
24	73,728	4	768 fs	8x
32	73,728	3	768 fs	8x
44,1	45,1584	4	256 fs	8x
48	73,728	2	768 fs	8x
96	73,728	2	384 fs (768 fs / 2)	4x
192	73,728	2	192 fs (768 fs / 4)	2x

Table 2 Examples of sample rates

4 Triggering

To prevent triggering during connection or initializing there is a “lock” bit.
After writing a logic ‘1’ into the lock bit in the PG24192 register, the PG24192 comes in the active mode. In the active mode the card is sensitive for a trigger event. The PG24192 can trigger on two trigger sources: Digital input triggers and Software trigger.
The separate trigger circuits from Channel-A and Channel-B makes that each channel can start on different trigger sources and on different trigger edges or levels. Figure 5 shows the trigger capabilities.

4.1 Digital input triggering

The digital trigger accepts triggers from the front panel and from the PXI back plane including PXI TRIGGER 0 to 7 and PXI STAR TRIGGER, see Figure 5. The front panel trigger input uses normal TTL logic levels, with a 0.5V nominal threshold for a low level and a 2V nominal threshold for a high level.
All the trigger inputs except the software trigger can handle different trigger events. It is possible to trigger on positive and negative level or positive and negative edge trigger signals.
For settings see the *PG24192_SetTriggerInput* command in the **PG24192 driver manual.**
In level trigger mode the generating starts when trigger goes active and stops when trigger goes inactive. Edge trigger mode has two options, normal or continuous. In normal mode the generating starts at a trigger edge and either stops on the next trigger edge. In continuously mode the generator runs until stopped by the software. Every measurement can be stopped with the software by forcing the channel out of “lock mode”. When the module is out of lock mode the trigger register will be cleared.

4.2 Software triggering

If trigger timing is not a issue, there is a software initiated trigger. By writing the trigger register the capturing can be started or stopped.

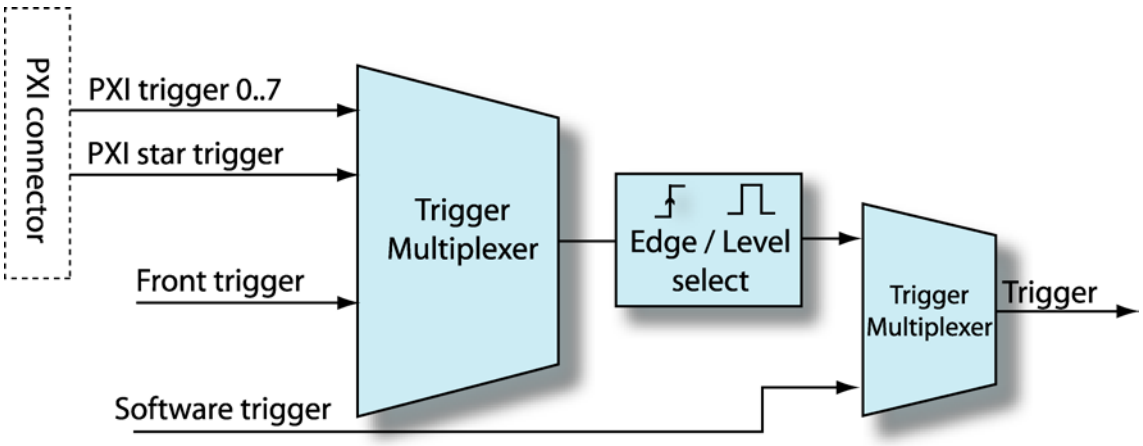

Figure 5 PG24192 trigger capabilities

5 Onboard Memory

Each channel of the PG24192 has a 1M x 24bit stimulus memory for waveform storage.
The stimulus memory of the PG24192 is addressed through a counter. This counter is active as well during generating as during reading or writing the memory via the bus. In bus access mode the clock for the memory counter is the read or write signal, and in generation mode the counter counts on the sample clock.
Before a measurement or a memory read or write action cycle the start and stop address from the address counter must be set. With the start and stop address it is possible to use the memory only for one signal (start address 0) or to split the memory in smaller segments (memory segmentation). (see Figure 6) With memory segmentation, every segment can holds a different waveform that can be written or outputted by setting the right start and stop address for that segment.

In bus access mode the counter increments after each memory write, until it reaches the programmed stop address. Since the memory can not be written during pattern generation, there is a lock bit that should be set to allow pattern generation. After setting the lock-bit, the card comes into active mode and is ready for triggering. In this mode the memory is locked for reading or writing. After clearing the lock-bit the memory is accessible again, a measurement that was running at that moment will be aborted.

After entering the active mode, and a trigger event is occurred the measurement is started and the counter starts counting from the programmed start address. The counter increments on each sample clock edge, until it reaches the programmed stop address. From the stop address the counter jumps back to the start address and counts up again. This loop repeats until stopped by the user. It is not possible to change the start and stop address or jump to another memory segment during a measurement.

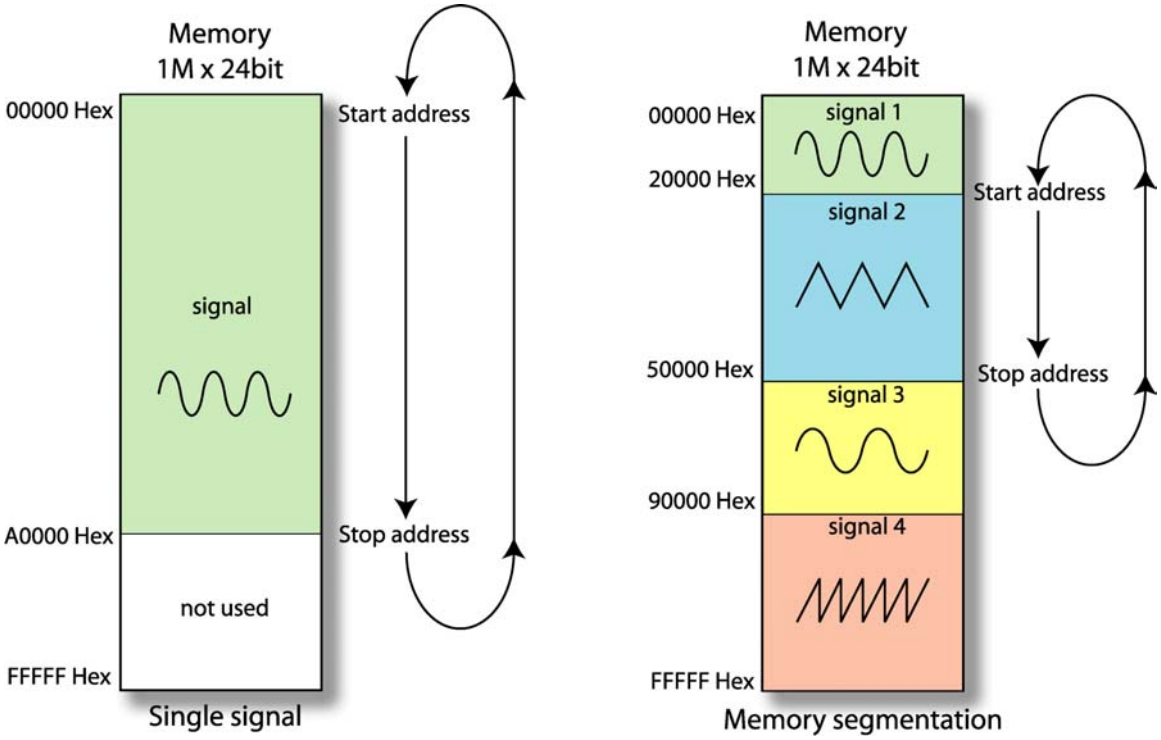

Figure 6 Different memory modes

6 Calibration

Calibration is a test that compares the values indicated by the PG24192 with a external reference source. The result of a calibration is used to determine the gain and offset error so the PG24192 can correct the error.
For optimum performance use self-calibration when the digitizer is placed in a new system or if the temperature changes more than 5°C from the previous calibration
The maximum recommended amount of time between two calibrations is six months.

The calibration can be done with the software tool **PG24192 calibration.**
Once the calibration process is done, the calibration constants will be stored in EEPROM. These values will be loaded by the software, and used as needed by the board.
The software tool leads you step for step through the calibration process. For details of the DLL function see the **PG24192 driver manual**.

7 Specifications:

General:

Number of channels	2 channel simultaneously sampled
DAC resolution	24 bit
Converter type	Delta Sigma
Sample rate	1kHz….192kHz
Memory depth	1M x 24bit per channel

Analog:

Output configuration	Differential
Output impedance	600Ω or low impedance software selectable
Output coupling	DC coupled
DC offset range	-5 Volt to +5Volt
Analog filters	1.2kHz , 22kHz or 100kHz Lowpass
Output ranges	0 to -80dB

Dynamic characteristics:

Amplitude accuracy	±0.05dB@ 1kHz/10Vpp
Frequency flatness	0.2dB from 20Hz to 20kHz
SFDR (fsample.=192kS/s)	112dB @ 1kHz/10Vpp
THD (fsample.=192kS/s)	110dB @ 1kHz/10Vpp
SINAD (fsample.=192kS/s)	107dB @ 1kHz/10Vpp

Sample clock:

Clock sources	SMB front, internal crystal oscillator, PXI bus
Internal clock frequencies	45.1584 MHz / 73.728 MHz
External clock frequency range	64kHz…100MHz
External clock levels	Vlow < 0.6V Vhigh > 1.4Volt
External clock impedance	50Ω DC

Triggering:

Trigger sources	Front, PXI trigger 0…7, PXI star trigger, software trigger
Trigger modes	Positive level, negative level, positive edge, negative edge, positive edge continuous and negative edge continuous
Front trigger impedance	10kΩ DC
Front trigger levels	Vlow < 0.6V Vhigh > 2.0Volt

Power Requirements:

maximum power consumtion

+3.3 Volt	+5 Volt	+12 Volt	-12 Volt

Environment:

Operating temperature	0 to 50°C
Storage temperature	0 to 70°C
Relative humidity	10 to 80 %, non-condensing

Mechanical

Size	single slot, 3U high
Weight	210 gram

8 Dynamic performance

Figure 7 Dynamic performance with 1kHz input signal