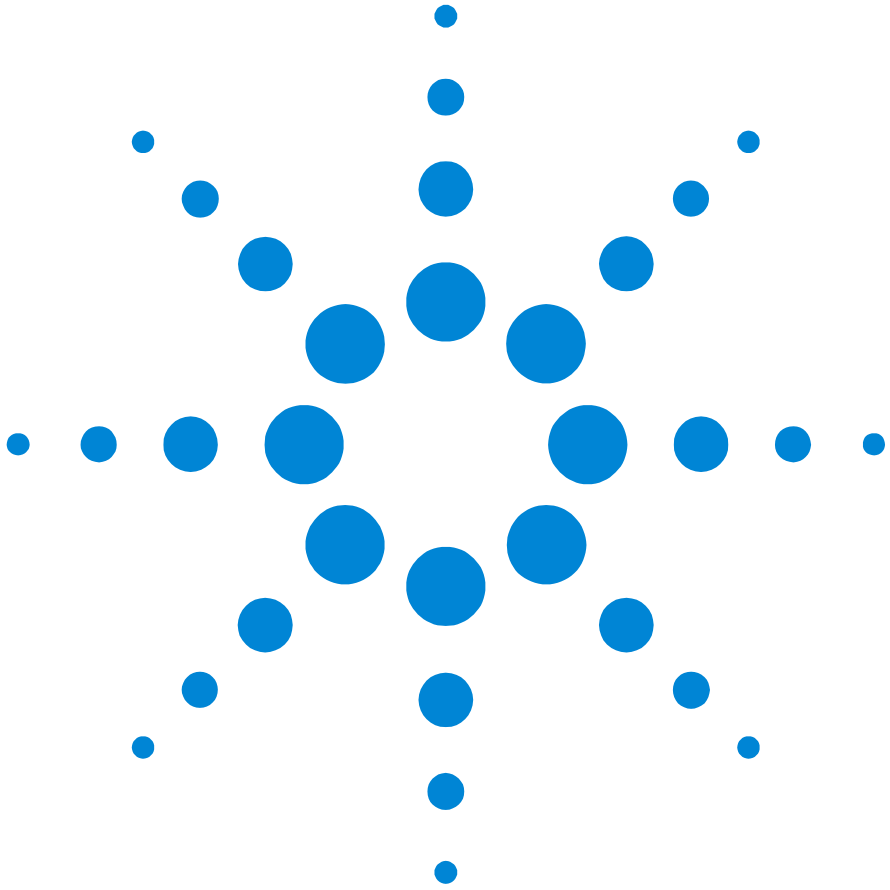

Agilent 81250 ParBERT

VSR4-01.0 Pattern Generator User Guide

Agilent Technologies

Important Notice

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Application Overview

This manual explains how the Agilent 81250 Parallel Bit Error Ratio Tester can be used for testing devices that conform to the OIF-VSR4-01.0 specification (also called VSR OC-192/STM-64 interface specification).

Focus of this manual

The focus of this manual is on how to use the VSR4-01.0 Pattern Generator utility provided by the Agilent 81250 ParBERT user software.

In addition, the manual provides examples that illustrate how VSR4 tests can be set up.

Reader assumptions

Readers should have a basic understanding of data transmission through optical fibers and some experience with electro-optical equipment.

Readers should also have some experience with the use of Agilent 81250 ParBERT systems. They should be familiar with the ParBERT online help and the *Agilent 81250 ParBERT System User Guide*.

Literature

The implementation of the ParBERT VSR4-01.0 Pattern Generator is based on the Implementation Agreement OIF-VSR4-01.0, published by the Optical Internetworking Forum (OIF).

The OC-192 interface is described in SFI-4 (OIF1999.102) “Proposal for a common electrical interface between SONET frame and serializer/deserializer parts for OC-192 interfaces”, published by the OIF.

What is VSR4-01.0

VSR4 is the acronym for “Very Short Reach OC-192/STM-64 Interface Based on Parallel Optics”. Several specifications for VSR4 interfaces exist.

The Implementation Agreement OIF-VSR4-01.0 describes a special SONET/SDH OC-192 interface for VSR applications from a functional point of view.

The VSR4-01.0 interface is targeted to transmit OC-192 data over a distance of up to 300 m through a ribbon fiber cable. It is a bidirectional interface, meant for interconnecting local (collocated) equipment.

Applications for VSR are, for example:

- Routers
- Dense Wavelength Division Multiplexer (DWDM) terminals
- SONET/SDH Add-Drop Multiplexers (ADMs)

Functional Overview

The VSR4-01.0 interface maps OC-192 (SONET) framed data to a parallel optical link. The general scheme is shown in the following figure.

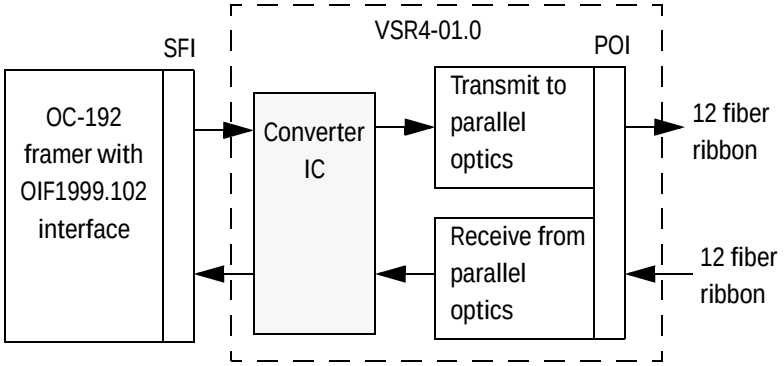


Figure 1 VSR4-01.0 Block Diagram

SFI is the acronym for the SERDES-Framer Interface. POI is the abbreviation for Parallel Optical Interface. The VSR4-01.0 POI uses for each direction, transmit and receive, 12 parallel glass fibers—ten for data transmission, two for error recognition and correction.

NOTE The *Converter IC* is the device to be tested with ParBERT.

Functions of the Converter IC

The converter IC supports both transmit and receive directions.

Transmit Direction

The Framer/SERDES interface should conform to OIF1999.102. This document specifies a 16-bit x 622 Mbit/s LVDS interface. The converter IC requires 16-bit word alignment.

For transmit, the converter IC has the following structure:

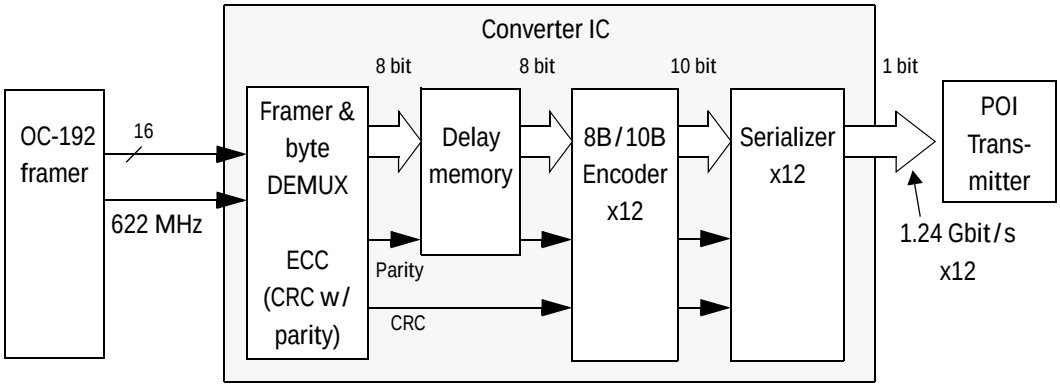


Figure 2 Transmit Direction Block Diagram

The transmit data interface is source synchronous—that means, the required 1.244 Gb/s high-speed data is synchronous with the 622 MHz clock received from the OC-192 framer chip.

The OC-192 frame is byte-wise striped across the 10 data channels. Before transmission, the data is 8B/10B encoded.

Channel 11 is the protection channel. It carries a parity bit, formed by a bit-wise XOR operation of the 10 data channels.

Channel 12 is the error detection channel (EDC). It is created by calculating a separate CRC16 over 24 bytes of data (defined as “virtual blocks”) from each of the other 11 channels of data.

NOTE For details on the frame conversion and data generation, please refer to the specification of the VSR4-01.0 interface.

Receive Direction

In receive direction, the twelve 1.244 Gbit/s data streams enter the receiver section of the converter. A recovered clock is derived from the data on a per-channel basis.

Then, the data streams are 10B/8B decoded. Using the frame delimiters present in each data stream for alignment purposes, the channels are deskewed.

The converter finally reassembles the data channels into a 16-bit wide data bus operating at 622 Mb/s.

The following figure shows a functional block diagram-

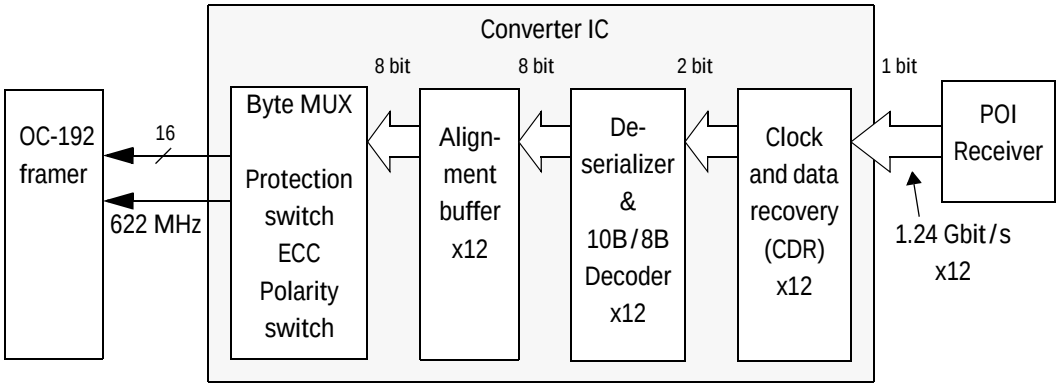


Figure 3 Receive Direction Block Diagram

NOTE OIF proposes a method for using the protection and error detection channels for error correction. For measuring the real bit error rate (BER), error correction should be disabled.

If error correction is enabled, the frame delimiters of reconstructed data channels will be set to “A1”. This is something the analyzers cannot presume. As a result, the measured BER will rise to high values—and possibly make the synchronization for ParBERT impossible.

Agilent 81250 ParBERT VSR4-01.0 Test Support

You need two ParBERT systems for testing VSR4-01.0 converter ICs—a stimulating system and an analyzing system

The ParBERT software provides the VSR4-01.0 Pattern Generator utility and preconfigured ParBERT settings.

The VSR4-01.0 Pattern Generator

The VSR4-01.0 Pattern Generator allows you to generate pattern files in ASCII format. These files can be generated for stimulating and analyzing systems and imported as ParBERT data segments.

The following test modes are supported:

Tests using PRWS data

- Send: OC-192 (16-bit SONET/SDH) framed PRWS

  Receive and analyze: VSR4-01.0 (12--bit) framed PRWS

- Send: VSR4-01.0 framed PRWS

  Receive and analyze: OC-192 framed PRWS

Tests using SONET frames

- Send: OC-192 SONET/SDH frames. Such frames can be generated with the ParBERT SONET/SDH Frame Generator.

  Receive and analyze: VSR4-01.0 framed SONET/SDH frames.

- Send: VSR4-01.0 framed SONET/SDH frames

  Receive and analyze: OC-192 SONET/SDH frames

Note that the analyzers must synchronize to the incoming data. Automatic Bit Synchronization is used. For the analyzing system, the VSR4-01.0 Pattern Generator can generate a special synchronization segment.

Preconfigured ParBERT Settings

The preconfigured settings are text files that can be imported.

TIP It is recommended to inspect the files with a text editor before importing them, because each setting requires a certain system configuration (see *"Prerequisites" on page 11*).

A total of six settings is available—three for the stimulating system and three for the analyzing system.

- The generator settings are located in the directory

  `C:Program Files\Agilent\Agilent81200\samples\settings\VSR4_Generator`

- The analyzer settings are located in the directory

  `C:Program Files\Agilent\Agilent81200\samples\settings\VSR4_Analyzer`

For an overview of the settings see also *"Provided Settings" on page 43*.

The settings contain references to certain memory-type data segments. You will have to replace these segments by your own segments, created with the VSR4-01.0 Pattern Generator and/or the SONET/SDH Frame Generator.

The use of the settings will be discussed in *"Examples for Setting up VSR4-01.0 Tests" on page 31*.

Prerequisites

Testing a VSR4-01.0 converter chip requires two ParBERT systems—a stimulating system and an analyzing system.

The required system configurations depend on the objective of the test.

Prerequisites for Testing the VSR4-01.0 Side

Here, you stimulate the OC-192 side and analyze the VSR side (transmit direction).

Configuration of the Generator System

The generator system requires

- One clock module (E4805B or E4808A)
- Sixteen data generator frontends

You could use four E4832A data modules equipped with sixteen E4838A, 675 MHz, differential output, low voltage amplitude/offset and variable slopes generator frontends.

This configuration, however, would never be able to stimulate also the VSR side of the DUT, because VSR requires a data rate of 1.24 Gbit/s.

Configurations that can be used for both sides are:

- Eight E4861A data modules, equipped with sixteen E4862A, 2.7 GHz, differential generator frontends

NOTE This is the configuration that fits to the preconfigured settings.

- Eight E4861A data modules, equipped with sixteen E4864A, 1.65 GHz, differential generator frontends
- Eight E4861B data modules, equipped with sixteen E4862B, 3.35 GHz, differential output frontends with variable delay and variable signal crossing

Configuration of the Analyzer System

The analyzer system requires

- One clock module (E4805B or E4808A)
- Twelve data analyzer frontends

Possible configurations are:

- Six E4861A data modules, equipped with twelve E4863A, 2.7 Gsa/s, differential/single-ended input frontend.

NOTE This is the configuration that fits to the preconfigured settings.

- Six E4861A data modules, equipped with twelve E4865A, 1.65 Gsa/s, differential/single-ended input frontends
- Six E4861B data modules, equipped with twelve E4863B, 3.35 Gsa/s, differential /single-ended input frontends

ParBERT Setup Example

Your configuration may look as shown in the following figure:

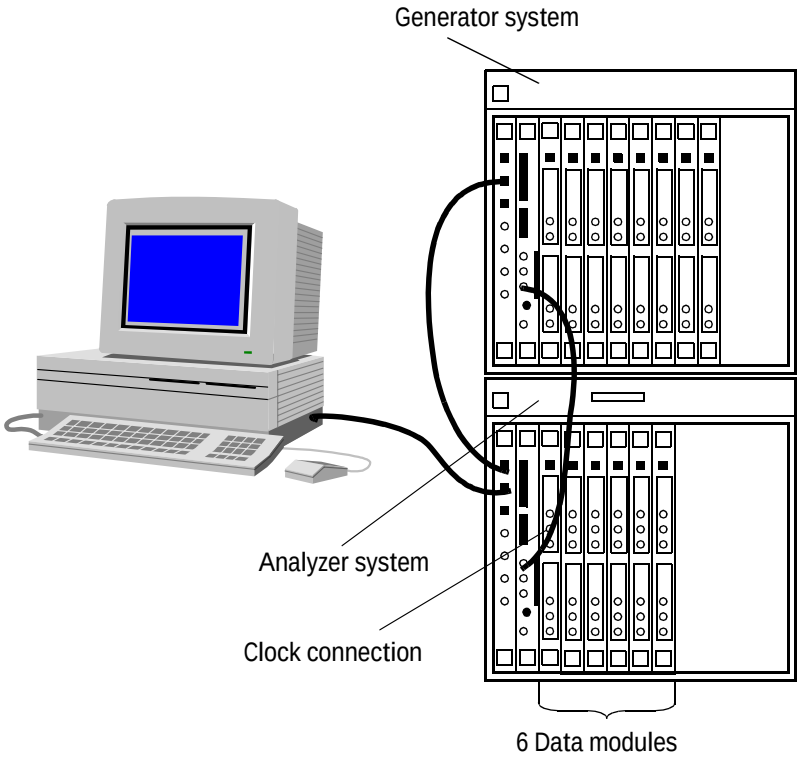


Figure 4 Pattern Generator / Analyzer Setup for Testing the VSR Side

NOTE Note that the generator system provides the clock for the analyzer system, because we are testing a synchronous device. The TRIGGER OUTPUT of the generator system is connected to the CLOCK/REF INPUT of the analyzer system.

NOTE With ParBERT, you can also test the twelve optical outputs of the Parallel Optical Interface (POI). For a configuration example see *"Prerequisites for Testing the POI" on page 16*.

Prerequisites for Testing the OC-192 Side

Here, you stimulate the VSR side and analyze the OC-192 side (receive direction).

Configuration of the Generator System

The generator system requires

- One clock module
- Twelve data generator frontends

Possible configurations are:

- Six E4861A data modules, equipped with twelve E4862A, 2.7 GHz, differential generator frontends

NOTE This is the configuration that fits to the preconfigured settings.

- Six E4861A data modules, equipped with twelve E4864A, 1.65 GHz, differential generator frontends
- Six E4861B data modules, equipped with twelve E4862B, 3.35 GHz, differential output frontends with variable delay and variable signal crossing

NOTE With ParBERT, you can also stimulate the 12 optical inputs of the Parallel Optical Interface (POI). For a configuration example see *"Prerequisites for Testing the POI" on page 16*.

Configuration of the Analyzer System

The analyzer system requires:

- One clock module
- Sixteen data analyzer frontends

You could use four E4832A data modules equipped with sixteen E4835A, 675 MSa/s, differential/single-ended input, high sensitivity analyzer frontends.

This configuration, however, would never be able to analyze also the VSR side of the DUT, because VSR has a data rate of 1.24 Gbit/s.

Configurations that can be used for both sides are:

- Eight E4861A data modules, equipped with sixteen E4863A, 2.7 Gsa/s, differential/single-ended input frontends

NOTE This is the configuration that fits to the preconfigured settings.

- Eight E4861A data modules, equipped with sixteen E4865A, 1.65 Gsa/s, differential/single-ended input frontends
- Eight E4861B data modules, equipped with sixteen E4863B, 3.35 Gsa/s, differential /single-ended input frontends

ParBERT Setup Example

Your configuration may look as shown in the following figure:

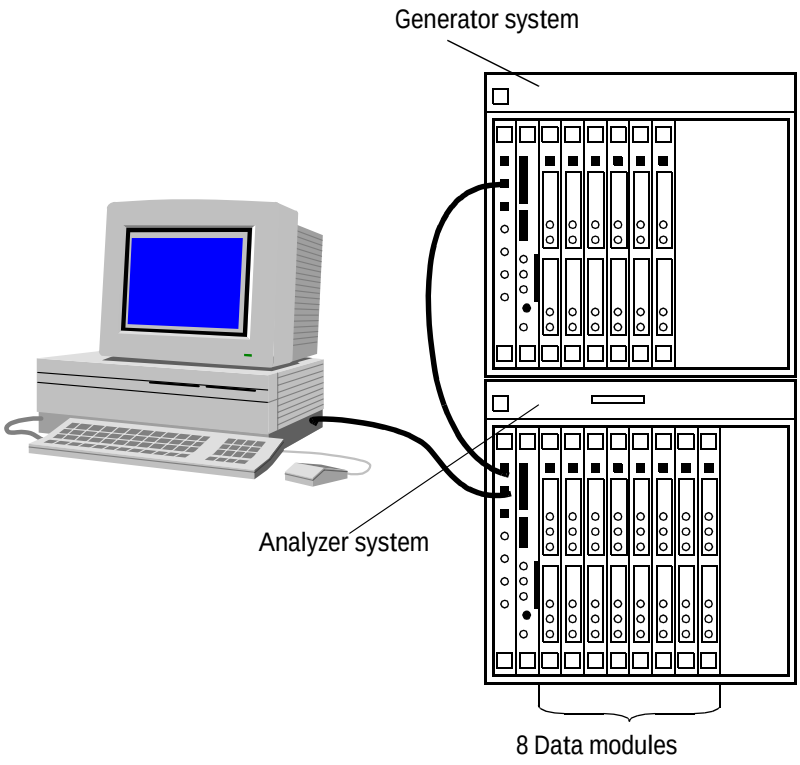


Figure 5 Pattern Generator / Analyzer Setup for Testing the OC-192 Side

When you are testing the receive direction of a VSR4-01.0 converter, the DUT provides the external source clock for the analyzer system.

TIP If you are planning to test both sides of the device, install eight data modules in each of the systems.

If you wish to use the preconfigured VSR4-01.0 settings without any modifications, install E4861A data generator/analyzer modules equipped with 2.7 Gbit/s frontends.

If you use different modules/frontends, edit the preconfigured VSR4-01.0 settings before importing them.

Prerequisites for Testing the POI

ParBERT allows you to test not only the electrical converter IC but also the complete VSR4-01.0 interface, including the Parallel Optical Interface (POI).

Prerequisites for Testing the Transmit Direction

Generator system configuration

For the stimulating system, you can use any of the configurations described in *"Prerequisites for Testing the VSR4-01.0 Side" on page 11*.

An economic solution would be to use:

- One E4805B clock module
- Four E4832A data modules equipped with sixteen E4838A, 675 MHz, differential output, low voltage amplitude/offset and variable slopes generator frontends.

Analyzer system configuration

The analyzing system requires:

- Two E4808A clock modules
- Twelve E4811A optical - electrical data analyzer modules

Prerequisites for Testing the Receive Direction

Generator system configuration

The stimulating system requires:

- Two E4808A clock modules
- Twelve E4810A optical - electrical data generator modules

Analyzer system configuration

For the analyzing system, you can use any of the configurations described in *"Prerequisites for Testing the OC-192 Side" on page 14*.

An economic solution would be to use:

- One E4805B clock module
- Four E4832A data modules equipped with sixteen E4835A, 675 MSa/s, differential/single-ended input, high sensitivity analyzer frontends.

ParBERT Setup Examples

A configuration for testing both directions of a VSR4-01.0 interface may look as shown in the following figure:

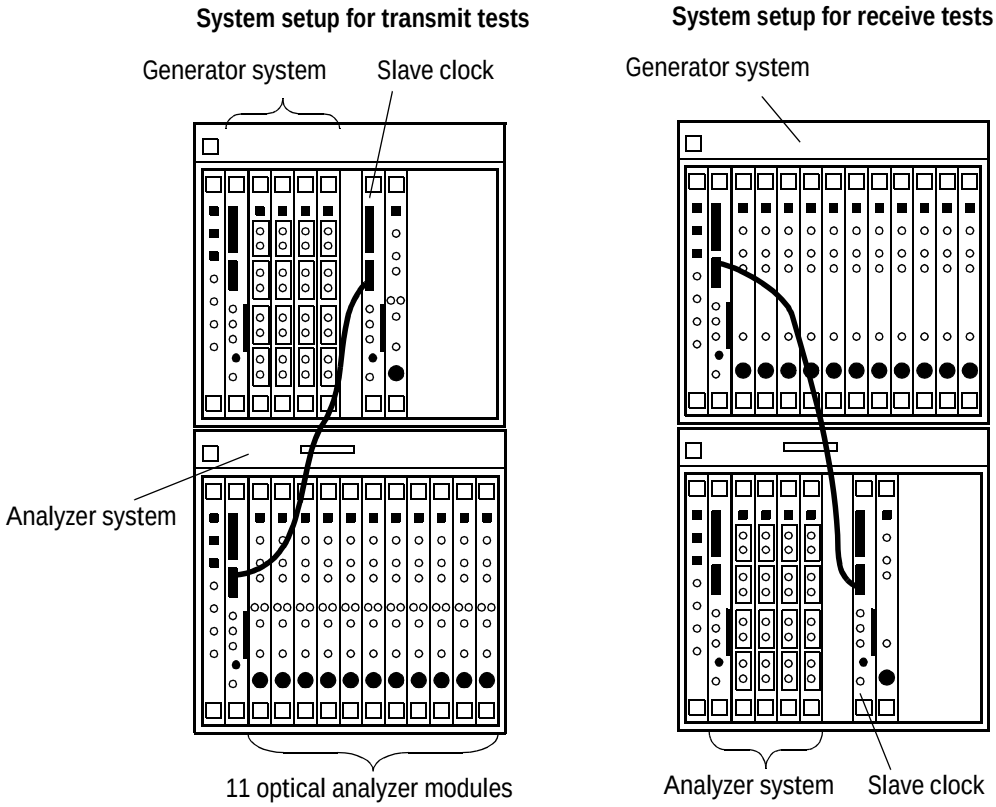


Figure 6 Pattern Generator / Analyzer Setup for Optical / Electrical Tests

Test Setup Procedures

This section provides an overview of the steps you have to perform for testing a VSR4-01.0 converter device.

You can stimulate the OC-192 side and analyze the VSR side (transmit direction). You can also stimulate the VSR side and analyze the OC-192 side (receive direction).

The general ParBERT setup procedures for both directions are essentially the same. Therefore, we differentiate only between generator and analyzer system setup.

NOTE Physical connections have to be made as well. They are not discussed in this manual.

Generate the Segment Files

The first step should be to generate the necessary segment files. This is done with the VSR4-01.0 Pattern Generator.

With this tool, you can generate ASCII files that can be imported into ParBERT as data segments.

You can generate:

- Segment files holding VSR4-01.0 framed PRWS data

  These patterns contain PRWS data that is framed according to VSR4-01.0.

- Segment files holding OC-192 framed PRWS data

  These patterns contain PRWS data that is framed according to OC-192. They correspond to the VSR4-01.0 framed PRWS data. They are not fully coded SONET/SDH frames. See also *"VSR4-01.0 Test Using PRWS Data" on page 32*.

- Segment files holding a VSR4-01.0 frame that contains a fully coded OC-192 SONET/SDH frame as payload

For details on the VSR4-01.0 Pattern Generator, see *"Using the VSR4-01.0 Pattern Generator" on page 25*.

Set Up the Generator System

Proceed as follows:

1 Start the user interface of the generator system.

2 Inspect the preconfigured generator settings (see also *"Preconfigured ParBERT Settings" on page 10*).

You may wish to import one of these settings. This is convenient. If the setting does not fit to your hardware configuration, you can first edit and then import it.

After importing the setting (use *File – Import – Setting*), continue with step 4.

3 If you wish to create your own setting, proceed as usual:

– With the Parameter Editor, set the global *Segment Resolution* and the system clock *Frequency*.

OC-192 requires 622.08 MHz, VSR4-01.0 requires 1244.16 MHz.

The minimum segment resolution for 622.08 MHz is 16 – for 1244.16 MHz, it is 32. The maximum depends on your hardware configuration.

– Adjust the *Trigger Frequency Multiplier*. It defines the clock signal at the TRIGGER OUTPUT of the clock module. This clock will be used by the analyzer system.

Suitable trigger frequencies are, for example, 311.04 MHz or 622.08 MHz.

– With the Connection Editor, create a DUT input port with 12 (VSR side) or 16 (OC-192 side) terminals and establish the connections to the generator frontends.

– Use the Parameter Editor to adjust the generated signal levels to the requirements of the DUT.

– With the Detail Mode Sequence Editor, create a sequence holding one block that is endlessly looped.

  Adjust the block length. VSR4-01.0 segments require a block length of 311,040 vectors. OC-192 segments require a block length of 77,760 vectors.

4 Save the setting (click *File – Save Setting As ...*).

5 Import the segment to be used by the generator system (click *File – Import – Segments*).

  Depending on the objective of the test, this is either one of the segments generated by the VSR4-01.0 Pattern Generator or a segment generated by the SONET/SDH Frame Generator.

TIP Import to the GlobalSegments pool is recommended. You can then use the segment also within other and different settings.

6 Use the Detail Mode Sequence Editor and replace the default segment by the imported segment.

7 Start the generator system (click the Run button).

  From now on, the generator system will continually generate the specified pattern and clock signal, until you click the Stop button.

Set Up the Analyzer System

Proceed as follows:

1 When you are testing the VSR side: Connect the TRIGGER OUTPUT of the generator system to the CLOCK/REF INPUT of the analyzer system physically. The analyzer system will use the external source clock provided by the generator system.

  When you are testing the OC-192 side: Connect the clock provided by the DUT to the CLOCK/REF INPUT of the analyzer system.

2 Start the user interface of the analyzer system.

3 Inspect the preconfigured analyzer settings (see also *"Preconfigured ParBERT Settings" on page 10*).

You may wish to import one of these settings. This is convenient. If the setting does not fit to your hardware configuration, you can first edit and then import it.

After importing the setting (use *File – Import – Setting*), continue with step 5.

4 If you wish to create your own setting:

- With the Parameter Editor, set the global *Segment Resolution* and the system clock *Frequency*.

  OC-192 requires 622.08 MHz, VSR4-01.0 requires 1244.16 MHz.

  The minimum segment resolution for 622.08 MHz is 16 – for 1244.16 MHz, it is 32. The maximum depends on your hardware configuration.

  On the *Clock/Ref Input* page, enable *External Clock Source*.

  Set the *Clock Multiplier* to a suitable value (1, 2 or 4, depending on the generator setup). Click the Measure button and make sure that the analyzer clock frequency is correct.

- With the Connection Editor, create a DUT output port with 12 (VSR side) or 16 (OC-192 side) terminals and establish the connections to the analyzer frontends.

- Use the Parameter Editor to adjust the expected signal levels.

- Open the the Standard Mode Sequence Editor and enable *Automatic Bit Synchronization*.

  This creates a sequence holding two blocks—one for the synchronization, one for the measurement.

- With the Detail Mode Sequence Editor, adjust the block lengths. VSR segments require a block length of 311,040 vectors. OC-192 segments require a block length of 77,760 vectors.

5 Save the setting under your own name (click *File – Save Setting As ...*).

6 Import the segments to be used by the analyzer system (click *File – Import – Segments*).

For testing the VSR side, two segments have to be imported—one for the synchronization block and one for the measurement block. For

testing the OC-192 side, one segment can be used for synchronization and measurement.

With one exception, the segments to be imported are generated with the VSR4-01.0 Pattern Generator. For details see *"Using the VSR4-01.0 Pattern Generator" on page 25*).

Only if you are analyzing OC-192 SONET frames, import the segment generated with the SONET/SDH Frame Generator.

TIP Import to the GlobalSegments pool is recommended. You can then use the segments also with other and different settings.

7 Use the Detail Mode Sequence Editor and replace the default segments by the imported segments.

You are now ready for running the test.

Using the VSR4-01.0 Pattern Generator

The VSR4-01.0 Pattern Generator generates ASCII files that can be imported as data segments into ParBERT systems.

You need three data segments for testing one side of a VSR4-01.0 converter:

- One segment for the generator system

  This segment holds the generated data. When the test is running, it is repeated until you click the Stop button.

- Two segments for the analyzer system

  These segments define the expected data. Of course, expected data must be correlated with generated data.

  One segment is used for automatic analyzer sampling point adjustment.

  The second segment is used for the measurement.

NOTE If you are analyzing the OC-192 side, you can use the analyzer measurement segment also for the synchronization.

The VSR4-01.0 Pattern Generator allows you to create these segments. This chapter explains the procedures and correlations.

How to Start the VSR4-01.0 Pattern Generator

To start the VSR4-01.0 Pattern Generator:

1 Click the Windows Start button.

2 Select *Programs – Agilent Digital Verification Tools – Utilities*.

3 Click *VSR4-01.0 Frame Generator*.

How to Operate the VSR4-01.0 Pattern Generator

The VSR4 Pattern Generator has the following user interface:

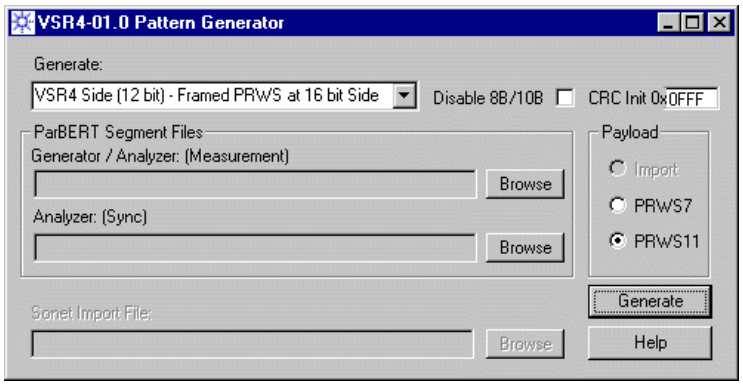


Figure 7 VSR4-01.0 Pattern Generator User Interface

Proceed as follows:

1 Select the kind of segment you wish to generate.

Choices are:

– *VSR4 Side (12 bit) - Framed PRWS at 16 bit Side*

This generates a VSR4-01.0 frame with a payload of PRWS data. After import, the generated segment can be used for stimulating

or analyzing the VSR side of the DUT. Note that pure PRWS is not a SONET frame.

If the segment is used for stimulating the DUT, the analyzing system would expect the same PRWS data, but OC-192 framed.

If the segment is used on the analyzing system for specifying expected data, the stimulating system must produce the same PRWS data, but OC-192 framed.

– *Sonet/SDH Side (16 bit) - Framed PRWS*

This is the counterpart of *VSR4 Side (12 bit) - Framed PRWS at 16 bit Side*.

This function generates an OC-192 frame with a payload of PRWS data. After import, the generated segment can be used for stimulating or analyzing the OC-192 side of the DUT. Note that this is not a fully encoded SONET frame.

If the segment is used for stimulating the DUT, the analyzing system would expect the same PRWS data, but VSR4-01.0 framed.

If the segment is used on the analyzing system for specifying expected data, the stimulating system must produce the same PRWS data, but VSR4-01.0 framed.

– *VSR4 Side (12 bit) - From Sonet/SDH Frame*

This generates a VSR4-01.0 frame. Its payload consists of a SONET/SDH frame. The generated data segment can be used for stimulating or analyzing the VSR side of the DUT.

To generate this kind of segment, you have to specify an input file holding SONET/SDH framed data. Such files of type ".hfm" can be generated with the SONET/SDH Frame Generator.

If the segment is used for stimulating the DUT, the analyzing system would expect OC-192 SONET/SDH framed data.

If the segment is used on the analyzing system for specifying expected data, the stimulating system has to generate the original SONET/SDH data from that ".hfm" file.

The SONET/SDH Frame Generator generates the corresponding segment file.

2 For segments holding PRWS data, decide on the polynomial.

Choices are *PRWS7* ($2^7 - 1$) and *PRWS11* ($2^{11} - 1$).

3 For VSR4-01.0 frames, you can disable the 8B/10B encoding.

Valid VSR4-01.0 frames are always 10-bit encoded. This option may help you to investigate and check the created files with a text editor.

4 Check or change the initialization of the CRC registers.

The CRC is calculated according to the CCITT CRC16 polynomial over 24 bytes of data. The VSR4-01.0 specification proposes a register initialization of 0...0FFF$_{hex}$. You can change that value, if required.

5 Specify the location and name for the ASCII file to be generated. This is done with the *Generator / Analyzer (Measurement)* browser.

- Click the Browse button.
- Choose an existing directory.
- Enter the file name.
- Click Save.

6 If the generated file shall ever be used on an analyzing system, you must also specify a location and name for the corresponding synchronization file.

This is done with the *Analyzer (Sync)* browser.

- Click the Browse button.
- Choose an existing directory.
- Enter the file name.
- Click Save.

NOTE For automatic analyzer sampling delay adjustment, Automatic Bit Synchronization is used. This requires a unique detect word at the beginning of each channel.

To ensure proper synchronization, the synchronization segment is 0x1 encoded and includes don't care bits.

This segment would hide bit errors at the respective bit positions and can therefore not be used for the measurement.

Your window may now look as shown below.

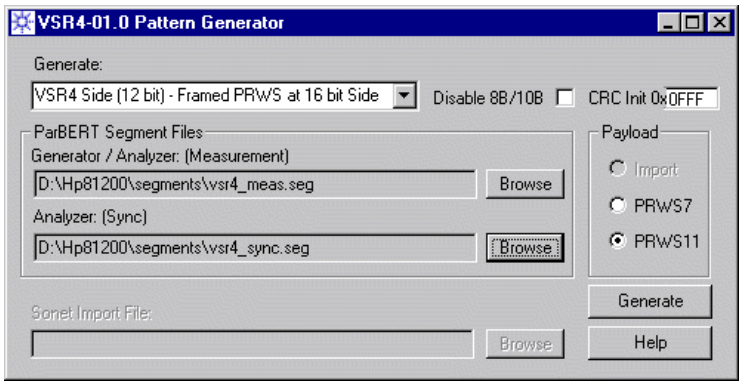


Figure 8 VSR4-01.0 Pattern Generator, Files Specified

7 If you have decided to create a VSR4 frame holding a payload of SONET/SDH formatted data, specify the source file. This file has to be of type ".hfm".

- Click the *Sonet Import File* Browse button.
- Choose the directory.
- Select the file.
- Click Save.

8 Click the Generate button.

The VSR4-01.0 Pattern Generator creates or updates the specified files.

Examples for Setting up VSR4-01.0 Tests

This section presents four setup examples for the following test modes:

From OC-192 to VSR

- Transmit: OC-192 framed PRWS
  Receive and analyze: VSR4-01.0 framed PRWS
- Transmit: OC-192 SONET frames
  Receive and analyze: VSR4-01.0 framed SONET frames

From VSR to OC-192

- Transmit: VSR4-01.0 framed PRWS
  Receive and analyze: OC-192 framed PRWS
- Transmit: VSR4-01.0 framed SONET frames
  Receive and analyze: OC-192 SONET frames

What you will learn

You will learn:

- How to find a suitable, preconfigured setting

NOTE The preconfigured settings require a system configuration as explained in *"Prerequisites" on page 11*.

- How to generate the data segments
- How to create the sequences for the generator and analyzer systems

VSR4-01.0 Test Using PRWS Data

In this example, we send OC-192 framed PRWS data and analyze VSR4-01.0 framed PRWS data.

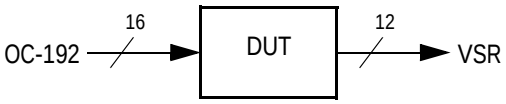


Figure 9 Setup for VSR4-01.0 Tests

Setup of the Generator System

Setting A suitable setting for the generator system can be imported from the file `vsr_sonet_prws_gen_set.txt`.

Segment The generator segment is generated with the VSR4-01.0 Pattern Generator.

Choose *Sonet/SDH Side (16 bit) - Framed PRWS* and a PRWS polynomial according to your needs. Select the file where to place the pattern and click the Generate button.

NOTE This pattern is not a fully coded SONET Frame; it holds 30 “A1” bytes (= 0xF6) and is filled with the selected PRWS.

If a completely coded SONET frame is required, this has to be generated with the SONET/SDH Frame Generator and imported as described in *“VSR4-01.0 Test Using SONET Frames” on page 34*.

Sequence

The test sequence of the generator system is shown in the following figure.

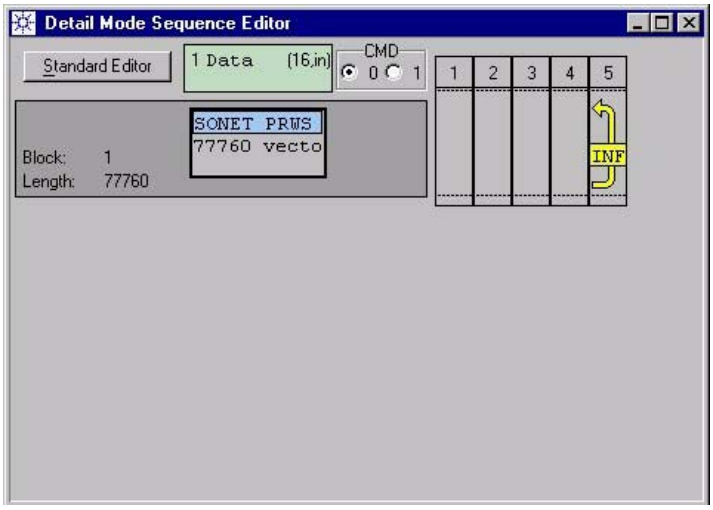


Figure 10 Sequence Editor for the Generator (16 bit)

The sequence contains one block that is endlessly looped. The data is generated and transmitted to a 16-terminal DUT input port.

Further information about block length and frequencies can be found in the Appendix.

Setup of the Analyzer System

Setting

A suitable setting for the analyzer system can be imported from the file `vsr_ana_prbs_set.txt`.

Segment

The analyzer segments are generated with the VSR4-01.0 Pattern Generator.

For the analyzer pattern, choose *VSR4 Side (12 bit) - Framed PRWS at 16 bit Side*, the appropriate PRWS, and the file where to place the segment pattern.

Select also the file where to place the analyzer synchronization pattern and click the Generate button.

Both files are needed. To ensure proper analyzer synchronization, the sync pattern includes don't care's. It is therefore not suitable for BER measurements.

Sequence The following figure shows the created sequence.

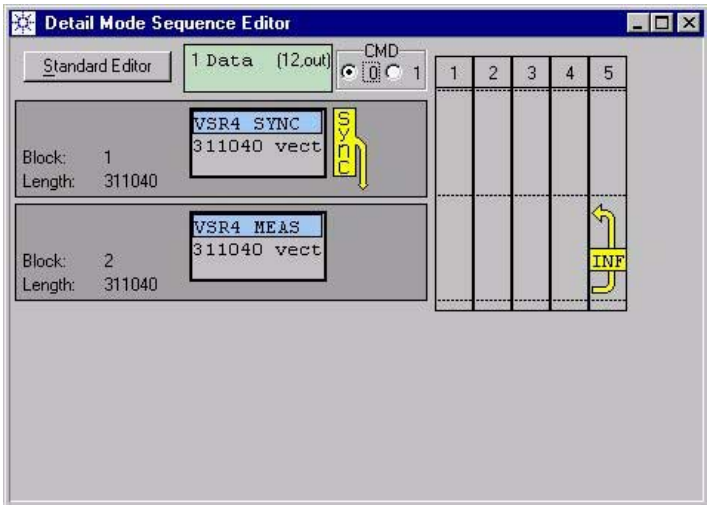


Figure 11 Sequence Editor for the Analyzer (12 bit)

The first block ensures proper synchronization while the second block defines the expected data.

VSR4-01.0 Test Using SONET Frames

In this example, we send OC-192 SONET frames and analyze VSR4-01.0 framed SONET frames.

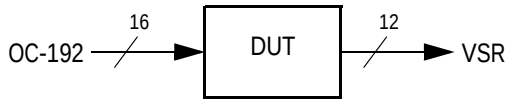


Figure 12 Setup for VSR4-01.0 Tests

Setup of the Generator System

Setting A suitable setting for the generator system can be imported from the file `vsr_sonet_prws_gen_set.txt`.

Segment The segment is generated with the SONET/SDH Frame Generator.

With the SONET/SDH Frame Generator, you can:

- Generate SONET or SDH frame files with arbitrary payload (".hfm" files)
- Generate a SONET/SDH frame file and a ParBERT segment file simultaneously
- Convert edited ".hfm" files to segment files that can be imported into ParBERT

For details see the *SONET/SDH Frame Generator User Guide*.

At the generator system, you have to import the segment file generated by the SONET/SDH Frame Generator.

Sequence The sequence of the generator system is shown in the following figure.

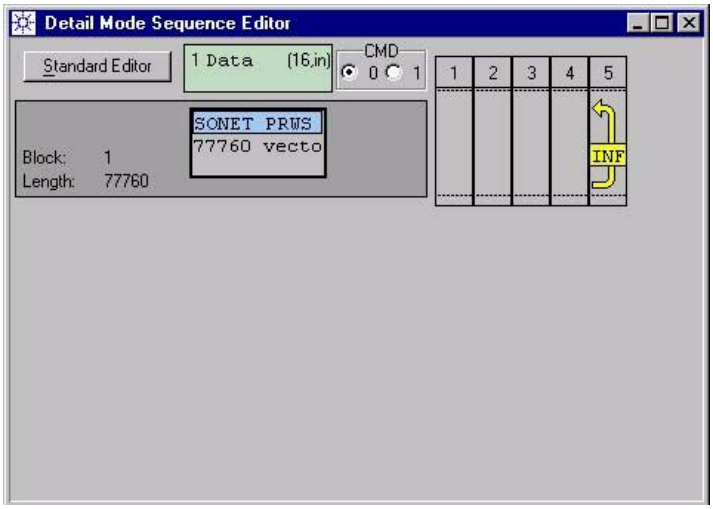


Figure 13 Sequence Editor for the Generator (16 bit)

Further information about block length and frequencies can be found in the Appendix.

Setup of the Analyzer System

Setting A suitable setting for the analyzer system can be imported from the file `vsr_sonet_ana_set.txt`.

Segment The analyzer segments are generated with the VSR4-01.0 Pattern Generator. A ".hfm" file, created with the SONET/SDH Frame Generator, is required. This has to be the frame file that corresponds to the generated segment.

For generating the analyzer pattern, choose *VSR 4 Side (12 bit) - From Sonet/SDH Frame*.

This enables the Browse button for importing the SONET frame file. Select the generated ".hfm" file. This file has to correspond to the generated pattern.

NOTE Only ".hfm" files can be imported. These files can be edited. Please refer to the *SONET/SDH Frame Generator* documentation for editing ".hfm" files and additional information.

For example, setting don't care values in the .hfm file for single bits does not work due to the 8B/10B coding. Only masking of full bytes is supported (e.g. masks like 0xff); other values will lead to unpredictable results.

In the VSR4-01.0 Pattern Generator, choose the file where to place the segment pattern. Select also the file where to place the analyzer synchronization pattern and click the Generate button.

Both files are needed. To ensure proper analyzer synchronization, the sync pattern includes don't care's. It is therefore not suitable for BER measurements.

Sequence The following figure shows the created sequence.

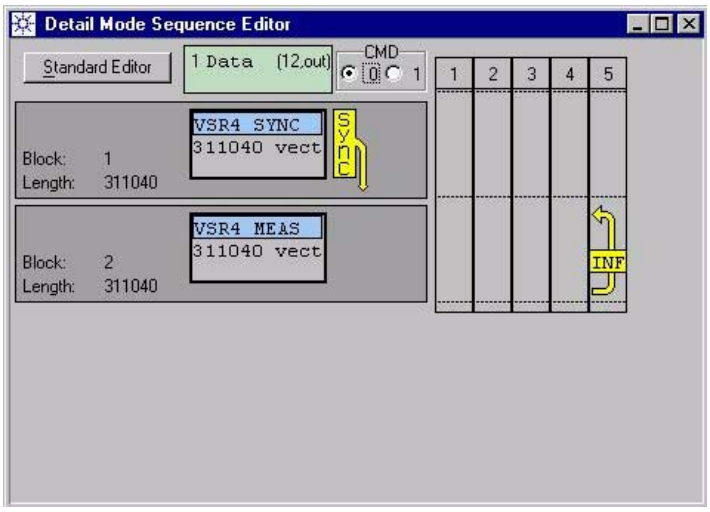


Figure 14 Sequence Editor for the Analyzer (12 bit)

The incoming data is expected from a 12-terminal DUT output port.

The first block ensures proper synchronization while the second block defines the expected data.

OC-192 Test Using PRWS Data

Here, we send VSR4-01.0 framed PRWS data and analyze OC-192 framed PRWS data. For the VSR4-01.0 converter, this is the receive direction.

Figure 15 Setup for OC-192 Tests

Setup of the Generator System

Setting A suitable setting for the generator system can be imported from the file `vsr_gen_prbs_set.txt`.

Segment The generator segment is generated with the VSR4-01.0 Pattern Generator.

Choose *VSR4 Side (12 bit) - Framed PRWS at 16 bit Side* and a PRWS polynomial according to your needs. Select the file where to place the pattern and click the Generate button.

NOTE This pattern consists of a VSR header (three columns: K28.5, D3.1/D21.2, K28.5) and is byte-wise filled with the selected PRWS. The PRWS appears physically only on the 16-bit side. See also *"Structure of the Generated Frames" on page 45*.

Sequence The sequence of the generator system is shown in the following figure.

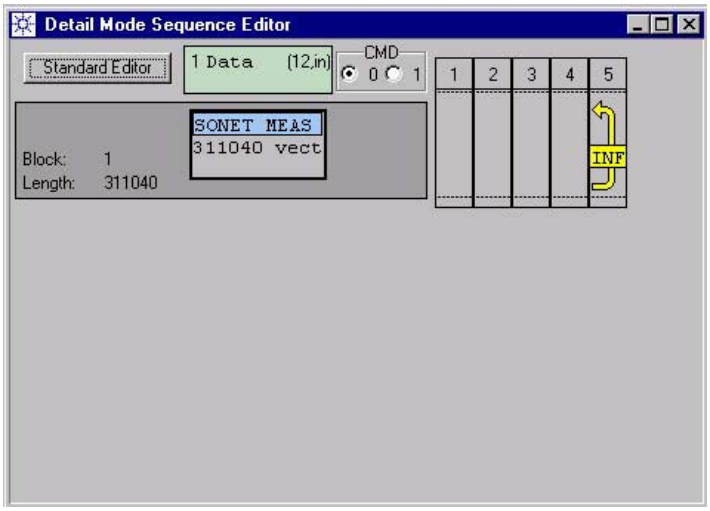


Figure 16 Sequence Editor for the Generator (16 bit)

This sequence contains one block that is endlessly looped. The data is generated and transmitted to a 12-terminal DUT input port.

Further information about block length and frequencies can be found in the Appendix.

Setup of the Analyzer System

Setting A suitable setting for the analyzer system can be imported from the file `vsr_sonet_prws_ana_set.txt`.

Segment The analyzer segments are generated with the VSR4-01.0 Pattern Generator.

For the analyzer pattern, choose *Sonet/SDH Side (16 bit) - Framed PRWS*, the appropriate PRWS, and the file where to place the segment pattern.

For this test, the same segment can be used for synchronization and measurement.

Sequence The following figure shows the created sequence.

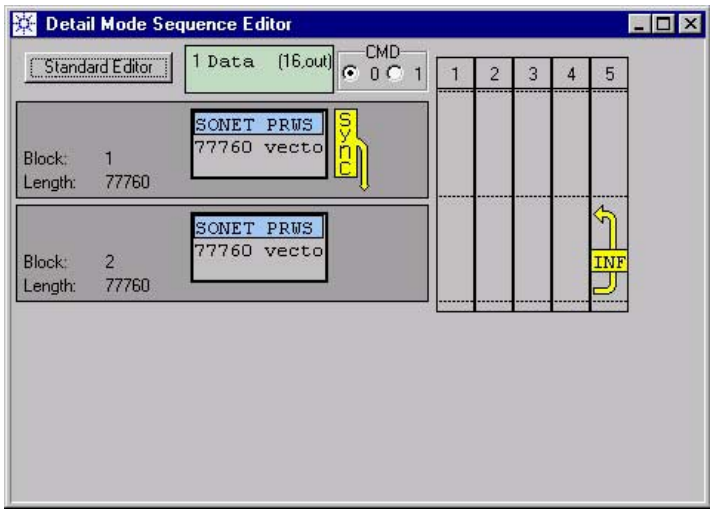


Figure 17 Sequence Editor for the Analyzer (16 bit)

OC-192 Test Using SONET Frames

In this example, we send VSR4-01.0 framed SONET frames and analyze OC-192 SONET frames.

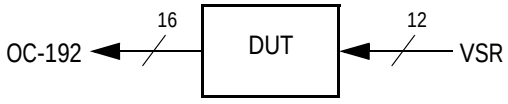


Figure 18 Setup for OC-192 Tests

Setup of the Generator System

Setting A suitable setting for the generator system can be imported from the file *vsr_sonet_gen_set.txt*.

Segment The generator segment is generated with the VSR4-01.0 Pattern Generator. A ".hfm" file, created with the SONET/SDH Frame Generator, is required.

For generating the pattern, choose *VSR 4 Side (12 bit) - From Sonet/SDH Frame*.

This enables the Browse button to import the SONET frame file.

Generate the segment data file and import it as a segment into the generator system.

Sequence The sequence of the generator system is shown in the following figure.

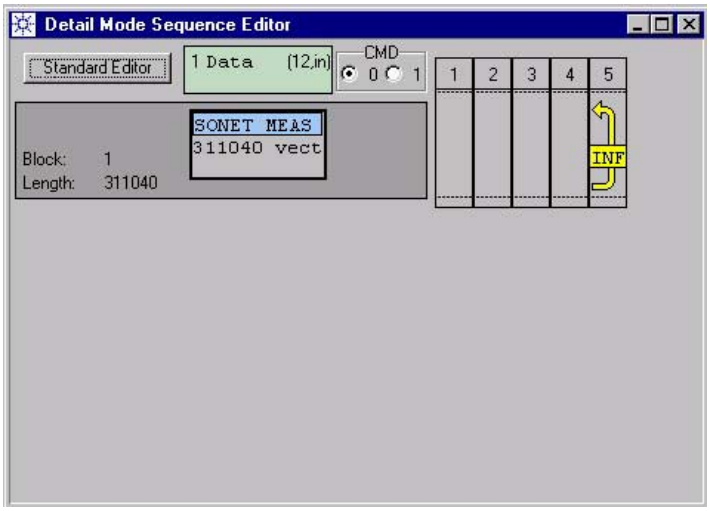


Figure 19 Sequence Editor for the Generator (12 bit)

Further information about block length and frequencies can be found in the Appendix.

Setup of the Analyzer System

Setting A suitable setting for the analyzer system can be imported from the file `vsr_sonet_prws_ana_set.txt`.

Segment The analyzer segment has to be generated with the SONET/SDH Frame Generator. It must correspond to the generated segment (that means, it must conform to the .hfm file used for the generator system).

Import the SONET segment file into the analyzer system.

Sequence The following figure shows the created sequence.

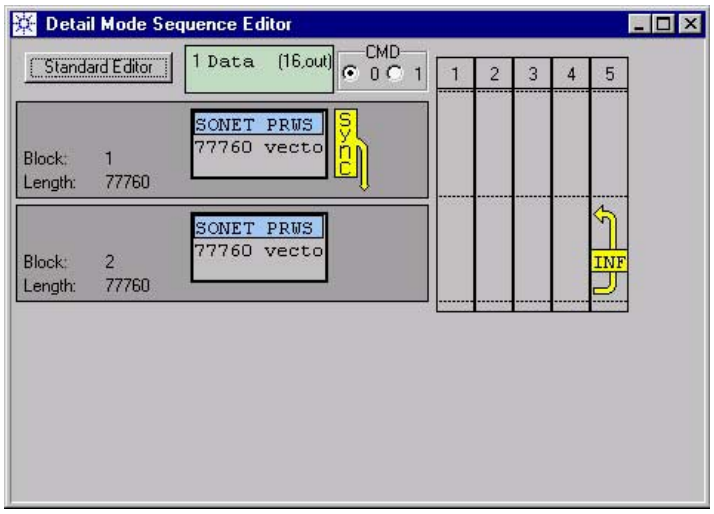


Figure 20 Sequence Editor for the Analyzer (16 bit)

Note that the same SONET segment is used for synchronization and for the measurement.

Appendix

This appendix provides an overview of the preconfigured settings, frequency requirements, and segment/block length calculations.

Provided Settings

The ParBERT software provides six preconfigured settings. You can import these settings, provided that your system has an appropriate hardware configuration (see *"Prerequisites" on page 11*).

The settings include:

- Setup of the clock module
  - Clock source – internal or external clock source

NOTE You need to check and, if necessary, change the settings of the *Trigger Frequency Multiplier* and the external *Frequency Multiplier/Divider*.

  - Segment resolution
  - Clock frequency
- Setup of the DUT and its connections to generator or analyzer frontends
- Generator/analyzer voltage levels

NOTE All the settings use ECL voltage levels and enable the frontend connectors.

- Measurement mode – BER
- Test sequence – executed when the test is started

- References to default segments.

NOTE You need to replace these segments by your own segments.

The following table gives an overview of the preconfigured settings.

Table 1 Provided Settings

Measurement (Analysis)	Frequency	Block Length	Sample Settings
VSR4 Side (12 bit), PRWS, generating	1244,16 MHz	311040	vsr_gen_prbs_set.txt
VSR4 Side (12 bit), PRWS, analyzing	1244,16 MHz	311040	vsr_ana_prbs_set.txt
VSR4 Side (12 bit), SONET, generating	1244,16 MHz	311040	vsr_sonet_gen_set.txt
VSR4 Side (12 bit), SONET, analyzing	1244,16 MHz	311040	vsr_sonet_ana_set.txt
SONET Side (16 bit), PRWS, generating	622,08 MHz	77760	vsr_sonet_prws_gen_set.txt
SONET Side (16 bit), PRWS, analyzing	622,08 MHz	77760	vsr_sonet_prws_ana_set.txt

Segment / Block Length Calculations

Length of a VSR4-01.0 Segment

An OC-192 frame contains

192 x 90 x 9 bytes = 155,520 bytes

After 8B/10B coding, this means 1,555,200 bits.

Separated into 10 data lines: 155,520 bits per line.

Because the Running Disparity (RD) may be different at the end of the repetitive pattern, the frame is doubled to neutralize the effect of the RD.

The length of the resulting pattern is hence:

155,520 x 2 = 311,040 vectors.

Length of an OC-192 Segment

An OC-192 SONET frame contains

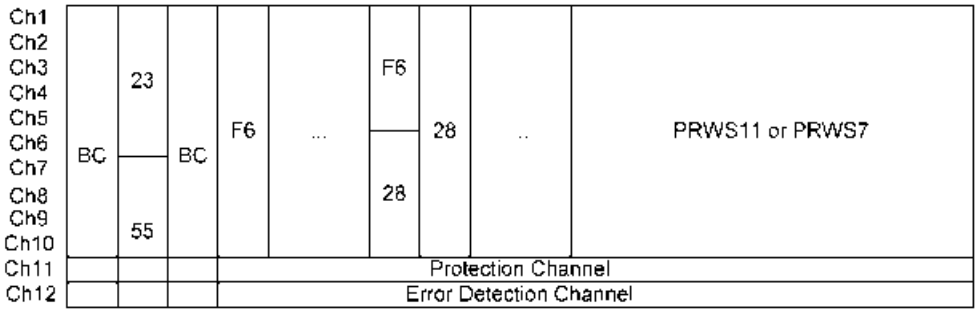
192 x 90 x 9 bytes = 155,520 bytes = 1,244,160 bits

Separated into 16 data lines, the length of the resulting pattern is hence:

1,244,160 / 16 = 77,760 vectors.

Structure of the Generated Frames

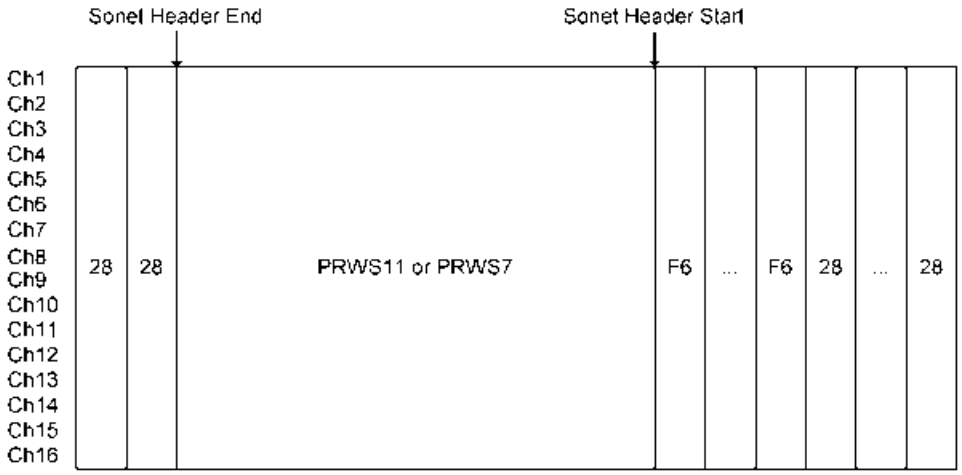
Structure of a VSR4-01.0 frame (payload = PRWS, 8B/10B encoded):



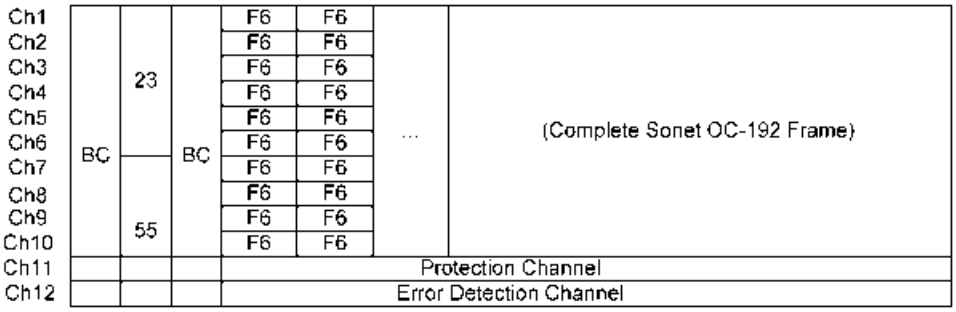
NOTE This is not an encapsulated SONET frame. The PRWS is distributed over 10 channels and the values of the protection channel (parity) and EDC are calculated accordingly.

The counterpart for this frame is an OC-192 formatted PRWS.

Structure of a SONET frame (payload = PRWS):



Structure of a VSR4-01.0 frame (payload = imported SONET frame, 8B/10B encoded):



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