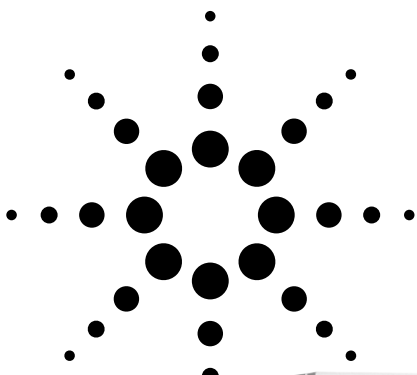


Agilent 4072A Advanced Parametric Test System with Agilent SPECS

Technical Data



1. General Description

The Agilent 4072A Advanced Parametric Test System is designed to perform precision DC measurement, capacitance measurement, Flash memory cell testing, and other high-frequency applications. The system supports up to eight source monitor units (SMUs), two of which may be high-power SMUs (HPSMUs). Each SMU is self-calibrating and may be individually configured to force either current or voltage, and simultaneously measure either voltage or current.

External instruments can be integrated into the system via the eight auxiliary input ports or 48 extended path inputs. The 48 extended path inputs allow the user to connect external signals directly to the DUT pins. A low-leakage switching matrix connects all of the inputs to fully guarded Kelvin output pins, which are customizable from 12 to 48 output pins. One special additional pin is dedicated as a chuck connection.

In addition, the Agilent 4072A has a high-frequency switching matrix with integrated pulse generator control. The high-frequency matrix is organized as two 3 x 24 matrices (6 inputs total), and furnished 1 TO 2 connectors may be used on each matrix pair to create one 3 x 48 matrix (3 inputs total). The system also has one 1.6 A ground unit.

Measurement Functions

DC current, DC voltage, capacitance and conductance, differential voltage, pulse force

DC Measurements: Spot, Sweep, Pulse, and Pulse Sweep

Measurement subsystem: MPSMU (Medium-Power SMU) and HPSMU (High-Power SMU)
Measurement range: 10 fA to 100 mA, 2 μ V to 100 V (using the 2 low current SMU ports)
100 fA to 1 A[†], 2 μ V to 200 V[†] (using the 6 standard SMU ports)

C/G Measurement: C/G, C/G-V

Measurement subsystem: 4284A
Test frequencies: 1 KHz, 10 KHz, 100 KHz, 1 MHz
Measurement range: 1 fF to 100 nF, 0.1 nS to 7.5 mS
DC bias voltage: \pm 40 V

Two-Terminal Differential Voltage Measurement

Measurement subsystem: 3458A
Measurement range: 1 μ V to 100 V

High-frequency Pulse Force

Supported pulse generators 81110A (or 8110A) and 8114A

Maximum number of installable pulse generators:

5 x 81110A or 8110A (without 8114A)
4 x 81110A or 8110A (with 1 x 8114A)
2 x 81110A or 8110A (with 2 x 8114A)

Pulse level (at open load): \pm 19 V (81110A or 8110A), - 49.9 V to + 50 V (8114A)
Pulse period: 350 ns to 999 s (81110A or 8110A), 350 ns to 999 ms (8114A)
Pulse width: 50 ns to 999 ms (81110A or 8110A), 150 ns to 150 ms (8114A)
Pulse delay: 0 s to 998 ms
Transition time: 20 ns to 200 ms (81110A or 8110A), 65 ns (8114A)

Switching Matrix Measurement Pins

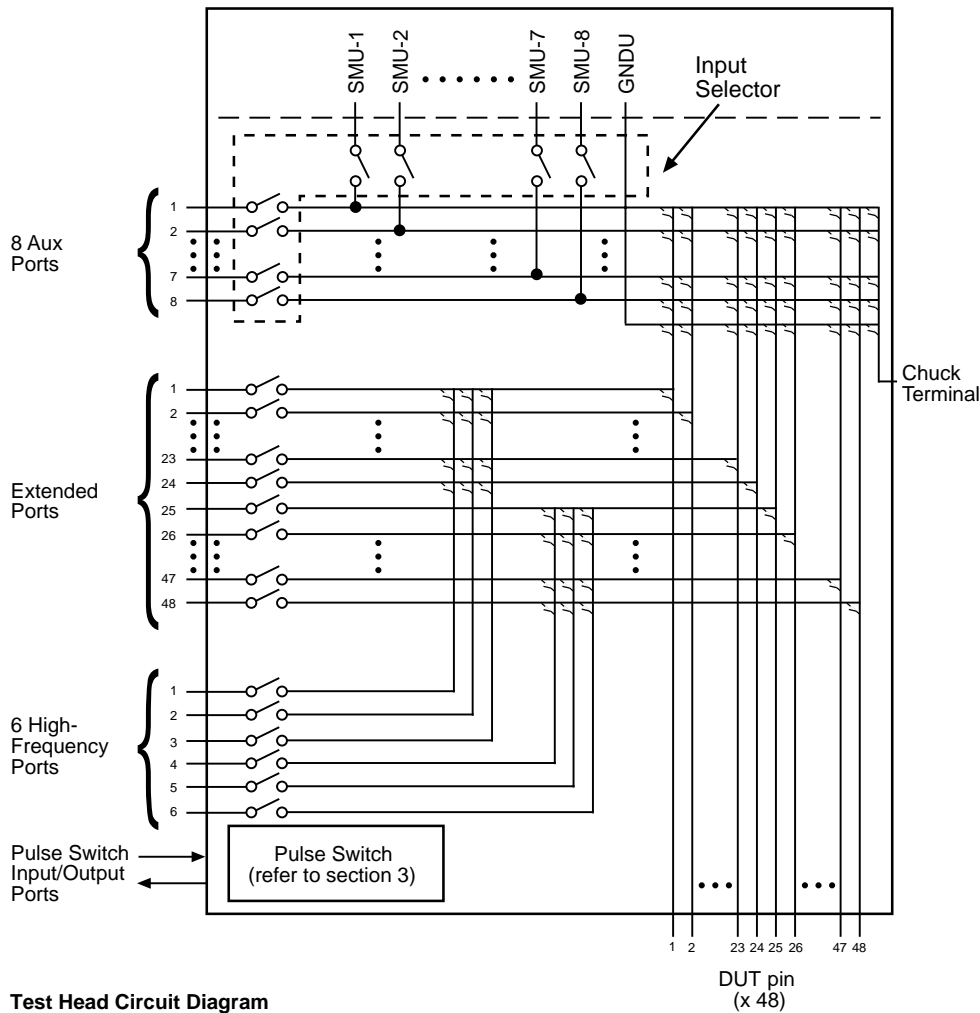
Between 12 and 48 pins (Note: One additional pin is dedicated for the prober chuck connection)

Switching Matrix Instrument Ports

Up to 8 SMUs and 1 ground unit
8 auxiliary (AUX) ports
6 high-frequency (HF) ports
48 extended paths
Pulse switch input / output ports

[†] Using optional HPSMU. Using MPSMU, 100 fA to 100 mA, 2 μ V to 100V

2. Switching Matrix Subsystem



Maximum DUT Pins

48 output pins + 1 pin for prober chuck connection (triax connector)

Maximum Number of Instrument Ports

SMU Port in Test Head: 8 SMU + 1 GNDU

2 ports for low-current measurement (Non-Kelvin)

4 ports (Kelvin)

2 ports (Non-Kelvin)

1 port for GNDU (Kelvin)

Auxiliary port: 8 for external instruments (C-meter, digital voltmeter, etc.)

2 triaxial input ports (Force/Guard/Common, aux input ports 1 and 2)

4 BNC two-pair input ports (Force/Common and Sense/Common, aux input ports 3 to 6)

2 BNC input ports (Force/Common, aux input ports 7 and 8)

High-frequency (HF) port: 6 for pulse generator (81110A or 8110A, and 8114A) or other external instruments.

HF ports 1 through 3 can access measurement pins 1 through 24, and HF ports 4 through 6 can access measurement pins 25 through 48. The user has the option of connecting any of the following HF port pairs together via a 1 TO 2 ADAPTOR in order to access all (1 through 48) measurement pins: ports 1 and 4, ports 2 and 5, and ports 3 and 6.

Extended port: 48 extended paths - The system provides one on/off relay for each path.

Pulse switch input/output ports: Please refer to the next section.

Maximum Voltage at Each Port

SMU port in test head:	±200 V
Auxiliary port:	±200 V (port 1 and 2) ±100 V (ports 3 to 8)
High-frequency port:	±100 V (between force and common of each HF port) ±100 V (between two forces of all HF ports) ±100 V (between any force of HF ports and any force of extended paths)
Extended path:	±100 V (between force and common of each extended path) ±100 V (between any force of HF ports and any force of extended paths)

Maximum Current, Port to DUT Pin

SMU port in test head:	±1.0 A
GNDU:	±1.6 A
Auxiliary port:	±1.0 A
High-frequency port:	±0.5 A
Extended path:	±0.5 A

Maximum Residual Resistance (reference data) through auxiliary port

Low current port:	Force 0.7 Ω
Kelvin port:	Force 1.0 Ω Sense 2.5 Ω
Non-Kelvin:	Force 1.0 Ω

through high-frequency port: 1.0 Ω

Maximum Stray Capacitance between DUT Pins (reference data)

5 pF (between C meter ports)

Isolation Resistance

Low current (with guard): $5 \times 10^{13} \Omega$

HF Port Bandwidth (@-3dB) (reference data)

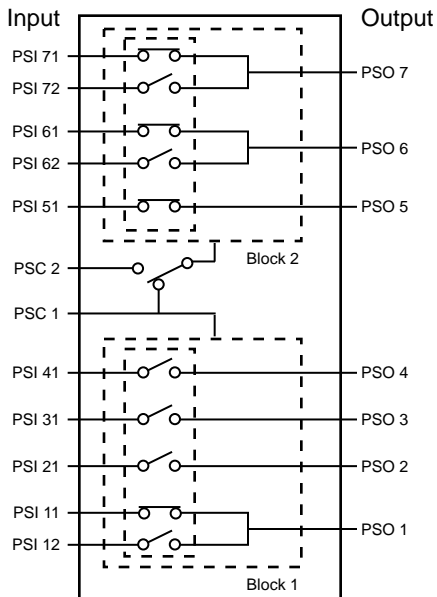
60 MHz (50 Ω load impedance: from port to DUT pin, 3 x 24 configuration)

HF Port Crosstalk between Pins (reference data)

±2 % (5 kΩ load impedance: from port to DUT pin, 20 ns pulse transition time)

3. Pulse Switch

The pulse switch includes seven semiconductor switching relays, for reliable and direct control of pulse shaping by the pulse generator or CPU. The pulse switch is integrated into the 4072A test head.



Number of Blocks: 2

Number of Switches for Each Block

Block 1: 3 relays (make or break, selectable type) and 1 relay (transfer type to create multi-level pulse)

Block 2: 1 relay (make or break, selectable type) and 2 relays (transfer type to create multi-level pulse)

Control Input Port

One input per each block (PSC1 and PSC2)

Control Method

Both the PG and CPU can control all switches. PG or CPU control is independent for every block. In the case of PG control, block 1 can be controlled by the PSC1 input, and block 2 can be controlled by either PSC1 or PSC2 (selectable).

Mode of Relay Control

Make or break, selectable type relay: Normally open or normally closed modes are selectable.

Transfer type relay: Normally open and normally closed modes are not selectable.

Maximum Voltage

±60 V (between force and common of each switch)

±60 V (between PSI 21 and PSO 2, between PSI 31 and PSO 3, between PSI 41 and PSO 4, between PSI 51 and PSO 5)

±60 V (between PSI 11 (or PSI 12) and PSO 1, between PSI 11 and PSI 12, between PSI 61 (or PSI 62) and PSO 6, between PSI 61 and PSI 62, between PSI 71 (or PSI 72) and PSO 7, between PSI 71 and PSI 72)

Maximum Current

±0.4 A (from input to output)

Residual Resistance (reference data)

Nominal 2 Ω (from IN to OUT)

OFF Capacitance (reference data)

80 pF (between IN and OUT: Vin-Vout=0 V)

100 pF (force <-> common @ output of make or break, selectable type relay: Vin-Vout=0 V)

Operating time of switching (reference data)

max. 2 ms

4. DC Measurement Subsystem

MPSMU and SMU (Source and Monitor Unit)

Voltage Source/Monitor Range, Resolution, and Accuracy

Full-Scale Voltage Range	Resolution Ion Force	Resolution Measure	Resolution Precision ADC	Force Accuracy ± (%reading + %range + volt)	Measure Accuracy ± (%reading + %range + volt)
±2 V	100 μV	100 μV	2 μV	0.05% + 0.05%+ (Rmat x Io)	0.04% + 0.04%+ (Rmat x Io)
±20 V	1 mV	1 mV	20 μV		
±40 V	2 mV	2 mV	40 μV		
±100 V	5 mV	5 mV	100 μV	0.045% + 0.04%+ (Rmat x Io)	
±200 V†	5 mV	10 mV	100 μV		

† Using HPSMU

Io = Output current

Rmat = Residual resistance of matrix port force

Note: Rmat is different at each port.

Low current port (Port 1, Port 2): 0.7 Ω

Kelvin port: 3 mΩ

Non-Kelvin port (Port 7, Port 8): 1.0 Ω

When using prober chuck connection pin, add 0.1 Ω to Rmat

Current Source/Monitor Range, Resolution, and Accuracy

When using low-current Port 1 and Port 2

Full-Scale Voltage Range	Resolution Ion Force	Resolution Measure	Resolution Precision ADC	Force Accuracy \pm (%reading + %range + amp)	Measure Accuracy \pm (%reading + %range + amp)
± 100 mA	5 μ A	5 μ A	100 nA	0.12% + [0.1 + (0.0005 x Vo)]%	0.1% + [0.05 + (0.0005 x Vo)]%
± 10 mA	500 nA	500 nA	10 nA		
± 1 mA	50 nA	50 nA	1 nA		
± 100 μ A	5 nA	5 nA	100 pA		
± 10 μ A	500 pA	500 pA	10 pA	0.2% + [0.1 + (0.0005 x Vo)]% + (2 pA/V x Vo)	0.2% + [0.05 + (0.0005 x Vo)]% + (2 pA/V x Vo)
± 1 μ A	50 pA	50 pA	1 pA		
± 100 nA	5 pA	5 pA	100 fA		
± 10 nA	500 fA	500 fA	10 fA	1% + [0.1 + (0.0005 x Vo)]% + 3 pA + (2 pA/V x Vo)	1% + [0.1 + (0.0005 x Vo)]% + 3 pA + (2 pA/V x Vo)
± 1 nA	50 fA	50 fA	10 fA		

Note: The HPSMU cannot be connected to ports 1 or 2.

When using standard Port 3 through Port 8

Full-Scale Voltage Range	Resolution Ion Force	Resolution Measure	Resolution Precision ADC	Force Accuracy \pm (%reading + %range + amp)	Measure Accuracy \pm (%reading + %range + amp)
± 1 A [†]	50 μ A	50 μ A	1 μ A	0.5% + [0.1 + (0.0005 x Vo)]%	0.5% + [0.05 + (0.0005 x Vo)]%
± 100 mA	5 μ A	5 μ A	100 nA	0.12% + [0.1 + (0.0005 x Vo)]%	0.1% + [0.05 + (0.0005 x Vo)]%
± 10 mA	500 nA	500 nA	10 nA		
± 1 mA	50 nA	50 nA	1 nA		
± 100 μ A	5 nA	5 nA	100 pA		
± 10 μ A	500 pA	500 pA	10 pA	0.2% + [0.1 + (0.0005 x Vo)]% + (300 pA + 1000 pA/100V x Vo)	0.2% + [0.05 + (0.0005 x Vo)]% + (300 pA + 1000 pA/100V x Vo)
± 1 μ A	50 pA	50 pA	1 pA		
+100 nA	5 pA	5 pA	100 fA		
± 10 nA ^{††}	500 fA	500 fA	10 fA	1% + [0.1 + (0.0005 x Vo)]% + [300 pA + (1000 pA/100 V x Vo)]	1% + [0.1 + (0.0005 x Vo)]% + [300 pA + (1000 pA/100 V x Vo)]
± 1 nA ^{††}	50 fA	50 fA	10 fA		

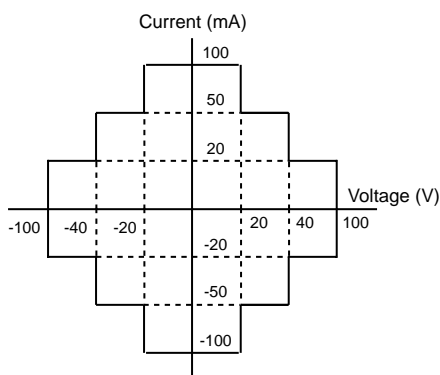
Note: The HPSMU can be connected only to ports 3 and 4.

[†]Using HPSMU

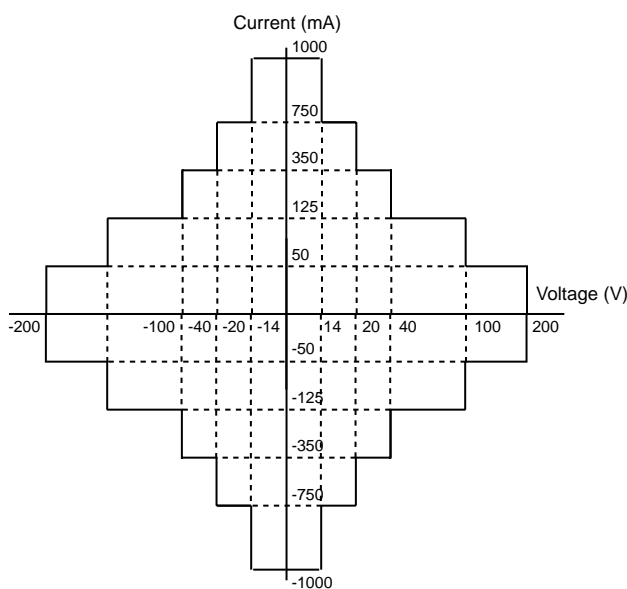
^{††}Reference data when using Port 3 to Port 8

Maximum Output Voltage/Current

Using MPSMU



Using HPSMU



Over current range: 15% of range (0% for 100 mA range of MPSMU, 0% for 1 A range of SMU)
 Over voltage range: (V Force): 0% of range
 (V Measure): 10% of range (0% for 100 V range of MPSMU, 0% for 200 V range of SMU)
 Current compliance setting range: 1 pA to maximum current

In the following section,

Accuracy of converse polar current limit^{††}: ±2% of range (100 nA to 1 A ranges)
 ±10% of range (1 nA and 10 nA ranges)

Maximum capacitive load: ≤1000 pF
 Maximum allowable guard capacitance: 250 pF (between signal line and guard line outside of the matrix)
 Maximum slew rate: 0.2 V/μs

^{††} Reference data

SMU Configuration

Minimum configuration: 3 MPSMUs (default configuration)

A maximum of 2 HPSMUs can be installed and can only be connected to ports 3 and 4. The first HPSMU must be connected to port 3, and the second to port 4. The default configuration of the 4072A has 3 MPSMUs connected to ports 2, 3, and 4. The default MPSMU positions must be changed if HPSMUs are added. For example, if one HPSMU is subsequently installed, it must be installed as port 3, so the MPSMU that was connected to port 3 should be moved to port 5. Similarly, if a second HPSMU is installed, it must be installed as port 4, so the MPSMU that was connected to port 4 should be moved to port 1. The following tables indicate the installation order for additional MSMUs.

No HPSMUs and 3 MPSMUs are installed

Port Number	Installed SMU	Installation order for additional SMUs
1	MPSMU	2
2	MPSMU	Default
3	MPSMU	Default
4	MPSMU	Default
5	MPSMU	1
6	MPSMU	3
7	MPSMU	4
8	MPSMU	5

One HPSMU and 3 MPSMUs are installed

Port Number	Installed SMU	Installation order for additional SMUs
1	MPSMU	1
2	MPSMU	Default
3	HPSMU	Optional HPSMU
4	MPSMU	Default
5	MPSMU	Default
6	MPSMU	2
7	MPSMU	3
8	MPSMU	4

Two HPSMUs and 3 MPSMUs are installed

Port Number	Installed SMU	Installation order for additional SMUs
1	MPSMU	Default
2	MPSMU	Default
3	HPSMU	Optional HPSMU
4	HPSMU	Optional HPSMU
5	MPSMU	Default
6	MPSMU	1
7	MPSMU	2
8	MPSMU	3

Ground Unit (GNDU)

This unit is used for ground when making measurements.

Output voltage:	0 V
Maximum current:	±1.6 A
Offset voltage:	±200 µV
Maximum capacitance load:	1 µF††

† Reference data

Digital Volt Meter (3458A)

Voltage Measurement Range, Resolution, and Accuracy at NPCL ≥ 1

Full-Scale Voltage Range	Resolution	Accuracy ±(% of reading + volt)
1 V	1 µV	0.01% + 300 µV
10 V	10 µV	0.01% + 300 µV
100 V	100 µV	0.02% + 1 mV

5. Capacitance Measurement

Accuracy is specified between any two output pins except chuck connection pin.

Measurement range:	1 fF to 1.2 nF and 10 nS to 7.5 mS	(1 MHz)
	1 fF to 10 nF and 1 nS to 6.3 mS	(100 KHz)
	1 fF to 100 nF and 0.1 nS to 6.3 mS	(10 KHz)
	10 fF to 100 nF and 0.1 nS to 0.63 mS	(1 KHz)
Measurement frequency:	1 KHz, 10 KHz, 100 KHz, and 1 MHz	
DC bias voltage:	±40 V	
Measurement speed:	MEDIUM or LONG	

Note: Above specifications are valid after calibration data measurement and offset cancel.

DC Bias Range and Accuracy

Full Scale Voltage Range	Force Accuracy ± (%reading + %range + volt)
±40V	0.1% + 10 mV

Accuracy is specified between CMH and CML pins.

Test signal level: 30 mV (rms)

Bias current isolation function: OFF

C/G Measurement Range, Resolution, and Accuracy

Frequency	C Range	C Accuracy % of reading + % of range	G Rang	G Accuracy % of reading + % of range
1 MHz	10 pF††	0.8% + [1.0 + (0.6 x Gm/63 µS)]%	63 µS	0.8% + [1.0 + (0.6 x Cm/10 pF)]%
	100 pF	0.8% + [0.3 + (0.6 x Gm/630 µS)]%	630 µS	0.8% + [0.3 + (0.6 x Cm/100 pF)]%
	1 nF	1.5% + [0.2 + (1.7 x Gm/6.3 mS)]%	6.3 mS	1.3% + [0.2 + (2.2 x Cm/1 nF)]%
100 KHz	10 pF††	0.4% + [1.0 + (0.3 x Gm/6.3 µS)]%	6.3 µS	0.4% + [1.0 + (0.4 x Cm/10 pF)]%
	100 pF	0.3% + [0.3 + (0.3 x Gm/63 µS)]%	63 µS	0.3% + [0.3 + (0.3 x Cm/100 pF)]%
	1 nF	0.3% + [0.2 + (0.4 x Gm/630 µS)]%	630 µS	0.3% + [0.2 + (0.4 x Cm/1 nF)]%
	10 nF	0.5% + [0.2 + 1.0 x (Gm/6.3 mS)]%	6.3 mS	0.7% + [0.2 + (0.8 x Cm/10 nF)]%
10 KHz	100 pF	0.3% + [0.2 + (0.3 x Gm/6.3 µS)]%	6.3 µS	0.3% + [0.2 + (0.3 x Cm/100 pF)]%
	1 nF	0.3% + [0.1 + (0.3 x Gm/63 µS)]%	63 µS	0.3% + [0.1 + (0.3 x Cm/1 nF)]%
	10 nF	0.3% + [0.1 + (0.3 x Gm/630 µS)]%	630 µS	0.3% + [0.1 + (0.3 x Cm/10 nF)]%
	100 nF	0.3% + [0.1 + (1.0 x Gm/6.3 mS)]%	6.3 mS	0.7% + [0.1 + (0.7 x Cm/100 nF)]%
1 KHz	100 pF††	0.4% + [0.5 + (0.4 x Gm/0.63 µS)]%	0.63 µS	0.4% + [0.5 + (0.4 x Cm/100 pF)]%
	1 nF	0.3% + [0.1 + (0.3 x Gm/6.3 µS)]%	6.3 µS	0.3% + [0.1 + (0.3 x Cm/1 nF)]%
	10 nF	0.3% + [0.1 + (0.3 x Gm/63 µS)]%	63 µS	0.3% + [0.1 + (0.3 x Cm/10 nF)]%
	100 nF	0.3% + [0.1 + (0.3 x Gm/630 µS)]%	630 µS	0.3% + [0.1 + (0.3 x Cm/100 nF)]%

Gm is measured conductance.

Cm is measured capacitance.

Accuracy is specified between any DUT pins.

Stray capacitance between force and guard must be under 5 pF.

Accuracy of frequency: ±0.1%

Test signal level: 30 mVrms ±5 mVrms

When measurement speed is set to SHORT, add 0.25% to % of reading and 0.1% to % of range.

When Open/Short calibration at DUT pins are carried out, accuracy is same as above table.

Note: The length of cable from output pins must be less than 1 meter, and capacitance to guard must be under 100 pF.

†† Reference data

6. Pulse Force Unit

Supported pulse generators:	81110A (or 8110A) and 8114A
Maximum number of installable pulse generators:	5 x 81110A or 8110A (without 8114A) 4 x 81110A or 8110A (with 1 x 8114A) 2 x 81110A or 8110A (with 2 x 8114A)

Pulse Force Mode

Pulse signal: 2-level and 3-level output

Burst count: 109 (max.) or infinite

Output mode: Normal mode or Pattern mode

Normal mode	All pulse generators (up to 5) can force in synchronization.
Pattern mode	All pulse generators except a master pulse generator can force in synchronization. (more accurate pulse width and pulse delay than normal mode). Note: 8114A does not support pattern mode.

Load impedance:	999 K Ω (default), selectable from 2.5 to 999 K (81110A or 8110A) 999 K Ω (default), selectable from 10 Ω to 999 K Ω (8114A)
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Pulse Setting Range

Pulse period

Normal mode	Range:	350 ns to 999 s, Resolution: 4 digits (min. 100 ps) (81110A or 8110A) Range: 350 ns to 999 ms, Resolution: 3 digits (min. 1 ns) (8114A)
Pattern mode	Range:	120 μ s to 999 s, Resolution: 4 digits (min. 100 ns) (81110A or 8110A) Range: 120 ns to 999 ms, Resolution: 3 digits (min. 1 μ s) (8114A)

Pulse width

Normal mode	Range:	50 ns to 999 ms, Resolution: 3.5 digits (min. 50 ps) (81110A) Range: 50 ns to 999 ms, Resolution: 3 digits (min. 100 ps) (8110A) Range: 150 ns to 150 ms, Resolution: 3 digits (min. 1 ns) (8114A)
Pattern mode	Range:	50 ns to 999 ms (81110A or 8110A in a master unit) 150 ns to 150 ms (8114A in a master unit) 100 ns to 999 ms (in slave units)
	Resolution:	3 digits (min. 100 ps) (81110A or 8110A in a master unit) 3 digits (min. 1 ns) (8114A in a master unit) In slave units, 1 x 10 ⁻ⁿ (at 1000 x 10 ⁻ⁿ < T \leq 4000 x 10 ⁻ⁿ) 2 x 10 ⁻ⁿ (at 4000 x 10 ⁻ⁿ < T \leq 8000 x 10 ⁻ⁿ) 2.5 x 10 ⁻ⁿ (at 8000 x 10 ⁻ⁿ < T \leq 10000 x 10 ⁻ⁿ) T means the maximum value of (pulse width + delay time) among all the channels. For example, if T is 250 μ s, then according to above table, the resolution is 0.1 μ s (1 x 10 ⁻⁷) because T = 250 x 10 ⁻⁶ = 2500 x 10 ⁻⁷ .

Pulse delay

Normal mode	Range:	0 to 998 ms, Resolution: 3.5 digits (min. 5 ps) (81110A) Range: 0 to 998 ms, Resolution: 3 digits (min. 10 ps) (8110A) Range: 0 to 998 ms, Resolution: 3 digits (min. 10 ps) (8114A)
Pattern mode	Range:	0 to 998 ms
	Resolution:	3 digits (min. 10 ps) (in a master unit) In slave units, 1 x 10 ⁻ⁿ (at 1000 x 10 ⁻ⁿ < T \leq 4000 x 10 ⁻ⁿ) 2 x 10 ⁻ⁿ (at 4000 x 10 ⁻ⁿ < T \leq 8000 x 10 ⁻ⁿ) 2.5 x 10 ⁻ⁿ (at 8000 x 10 ⁻ⁿ < T \leq 10000 x 10 ⁻ⁿ) T means pulse period specified in the Force _ pg subprogram. If not specified, T is the maximum value of 1.1 x (pulse width + delay time + 30 ns) among all specified PGs.
Transition time:		20 ns to 200 ms (81110A or 8110A) 65 ns (fixed) (8114A)

Pulse level (at open load)

81110A or 8110A:	\pm 19 V (at 2 level) \pm 19 V (at 3 level) Restriction for "3-level pulse with one PG" output mode: the sum of the absolute values of both amplitudes cannot exceed 20 V.
8114A:	-49.9 V to +50 V (at 2 level) -49.9 V to +50 V (at 3 level) There is no "3-level pulse with one PG" output mode on the 8114A because it has only one output.
81110A (or 8110A) and 8114A:	-49.9 V to +50 V (at 3 level)

Pulse level accuracy (at open load)	
81110A or 8110A level:	$\pm[(2\% \text{ of amplitude}) + 150 \text{ mV}]$
8114A amplitude:	$\pm[(2\% \text{ of amplitude}) + 200 \text{ mV}]$
8114A baseline:	$\pm[(2\% \text{ of baseline}) + (1\% \text{ of amplitude}) + 200 \text{ mV}]$
Pulse shape accuracy (at 50 Ω load impedance)	
81110A width:	$\pm(3\% \text{ of setting} + 2 \text{ ns})$ or $\pm(0.5\% \text{ of setting} + 2 \text{ ns})^*$ (in normal mode, width $\geq 50 \text{ ns}$)
81110A delay:	$\pm(3\% \text{ of setting} + 1 \text{ ns})$ or $\pm(0.5\% \text{ of setting} + 1 \text{ ns})^*$ (in normal mode, width $\geq 50 \text{ ns}$)
8110A width:	$\pm(5\% \text{ of setting} + 2 \text{ ns})$ (in normal mode, width $\geq 50 \text{ ns}$)
8110A delay:	$\pm(5\% \text{ of setting} + 1 \text{ ns})$ (in normal mode)
81110A or 8110A transition:	$(-10\% \text{ of setting})$ to $(+10\% \text{ of setting} + 20 \text{ ns})$ (transition time $\geq 20 \text{ ns}$)
81110A or 8110A overshoot:	$\pm(5\% \text{ of amplitude} + 20 \text{ mV})$ (transition time $\geq 20 \text{ ns}$)
8114A width:	$\pm(5\% \text{ of setting} + 3.5 \text{ ns})$ (width $\geq 200 \text{ ns}$) $\pm(5\% \text{ of setting} + 6.0 \text{ ns})$ (width $\geq 150 \text{ ns}$)
8114A delay:	$\pm(5\% \text{ of setting} + 1 \text{ ns})$
8114A transition:	$\pm 65 \text{ ns} + 20 \text{ ns}$
8114A overshoot:	$\pm(5\% \text{ of amplitude} + 50 \text{ mV})$
Pulse shape accuracy (at 5 K Ω load impedance; reference data)	
81110A or 8110A overshoot/ringing:	$\pm(5\% \text{ of amplitude} + 20 \text{ mV})$
8114A overshoot/ringing:	$(-8\% \text{ of amplitude})$ to $(+4\% \text{ of amplitude})$
81110A or 8110A transition time:	$\pm(10\% \text{ of setting} + 5 \text{ ns})$
8114A transition time:	$56 \text{ ns} \pm 5 \text{ ns}$
Skew between pins:	$\pm 10 \text{ ns}$

*Supplement characteristics after timing calibration

7. System Controller

Supported computers:	HP 9000 Series 700 Models 745/132L and 745I HP Visualize Workstation C3600
Operating systems:	HP-UX 10.20 (Needs some patches for Year 2000; Please contact your local sales representative.) HP BASIC/UX 8.02, SICL or C/ANSI C, SICL
Required memory:	64 MB (128 MB recommended)
Required disk:	2 GB (4 GB recommended)
Required GPIB interface cards:	Agilent recommends two external GPIB interface card for use with: Instruments controlled by 4072A TIS commands (e.g. 4284A, 3458A, 81110A, 8110A, and 8114A) Automatic Wafer Prober

8. System Software

Standard 4072A software provides the following capabilities:

- System management
- Control of subsystems (TIS Library)
- Parameter measurement utility (PARA Library)
- Off-line debugging
- Interactive debugging panel (IDP)
(includes Agilent FASTCode Generating Function)
- Probing pattern generation and wafer maps display (PPG, MAP)
- Prober control library (sample program): Electroglas, TEL, and TSK
- Application program (sample program): Flash memory cell evaluation, charge pumping method
- Automatic diagnostics

9. Semiconductor Process Evaluation Core Software (SPECS)

SPECS is a test shell environment for the 4070 series.

Input:	User interaction occurs via a windows-based graphical interface with spreadsheet-like operation. Test plans require only four simple specifications: wafer, die, test, and probe.
Customization:	Agilent supplies basic development, engineering, and operator test shell frameworks, which users can tailor or modify to create entirely new frameworks.
Analysis & output:	All data is output into a flat ASCII file that users can manipulate to allow for input into database software. In addition, the data management structure supports x-y graphs, histograms, and wafer maps.
UNIX:	Users have full access to the UNIX environment from within the test shell.

10. General Specifications

Accuracy is specified at:	Conditions
Temperature:	23° C to ±5° C
Humidity:	5% to 70% RH
Warm up:	at least 40 min.
Integration Time:	Medium or longer
After Self-Calibration:	N/A

Note: The temperature changes after calibration must be less than 30 C.
Accuracy is doubled at the temperature over the above range.
Isolation and leakage current are specified separately.

Power Requirement:

Nominal Line Voltage†	Allowable Voltage Range	Required Maximum Current
200 Vac	180 - 220 Vac	20 A
208 Vac	188 - 228 Vac	24 A
220 Vac	198 - 242 Vac	20 A
240 Vac	216 - 252 Vac	20 A
240 Vac	216 - 252 Vac	20 A

† Line frequency must be 48 to 63 Hz

Operating temperature range:	5° C to 40° C
Operating humidity range:	5% to 70%
Storage temperature range:	-20° C to 60° C (no condensation)
Warm up time (minimum):	40 minutes
Regulatory compliance	
EMC:	EMC Directive 89/336/EEC, 93/68/EEC
Safety:	Low Voltage Directive 73/23/EEC, 93/68/EEC CSA 1010, CSA Certified SEMI S2/93

Dimensions

System Cabinet:	600 mm (W) by 900 mm (D) by 1600 mm (H)
Test Head:	640 mm (W) by 642 mm (D) by 400 mm (H)

Weight:

System Cabinet:	250 kg (including 4284A, 3458A, 4 x 81110A, 8110A and 8114A)
Test Head:	70 kg (including 4 SMUs and 48 pins)

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