# 5000 SERIES

# SYSTEM USER'S MANUAL

**Part No. 09-0248**

**REVISION K**

**06/02/2014**

## Document History

| | | | |
|---|---|---|---|
| **Rev X1** | **Preliminary** | **03/22/99** | **R. W.** |
| **Rev X2** | **Update** | **02/17/00** | **R. W.** |
| **Rev X3** | **Update** | **03/02/00** | **R. W.** |
| **Rev X4** | **Update** | **05/24/00** | **P. H.** |
| **Rev A** | **ECO 15114** | **10/02/00** | **V.J.B** |
| **Rev B** | **ECO 15185** | **02/02/01** | **J. A.** |
| **Rev C** | **ECO 15383** | **08/16/01** | **J. A.** |
| **Rev D** | **ECO 15886** | **03/01/05** | **P. H.** |
| **Rev E** | **ECO 16429** | **09/29/08** | **J. A.** |
| **Rev F** | **ECO 16646** | **05/12/10** | **J. A.** |
| **Rev G** | **ECO 17183** | **01/02/14** | **S.M** |
| **Rev H** | **ECO 17212** | **01/02/14** | **T.F.** |
| **Rev J** | **ECO 17218** | **04/08/14** | **C.E.** |
| **Rev K** | **ECO 17232** | **06/02/14** | **BH** |

## Proprietary Rights Notice

**This document and the information that it contains are the property of NH Research, Incorporated. The rights to duplicate or otherwise copy this document, the rights to disclose the document and its information to others, and the right to use the information therein may be acquired only by written permission signed by a duly authorized officer of NH Research, Incorporated.**

**Unauthorized duplication of software and documentation provided with the test workstations violates the copyright protection provided by law. However, backup copies of programs are permitted for archives and recovery from hardware failures.**

**The material in this publication is current as of the release date on the cover page and is subject to change without notice. Any questions concerning the product or any questions or comments concerning this manual should be directed to the NH Research Field Service Department during normal business hours Monday through Friday at (949) 474-3900 or FAX (949) 474-7062 or www.nhresearch.com.**

***em*Power® is a trademark of NH Research, Incorporated.**

# TABLE OF CONTENTS

# 1. SAFETY

## 1.1 WARNING: LIVE CIRCUITS

NO INTERNAL ADJUSTMENT OR COMPONENT REPLACEMENT IS ALLOWED BY NON-NH RESEARCH QUALIFIED PERSONNEL. COMPLETE THE FOLLOWING BEFORE ACCESSING THE INSTRUMENT INTERNALS:

- **REMOVE ALL EXTERNAL VOLTAGE SOURCES**
- **DISCONNECT POWER CORD**
- **WAIT A MINIMUM OF 1 MINUTE TO DISCHARGE CIRCUITS**
- **VERIFY CIRCUITS ARE DISCHARGED.**

# 2. INTRODUCTION

The Digital Measurement System (DMS) provides voltage, current, timing, and frequency measurements for the N.H. Research Model 53x and 55xx tester families, and a multiplexer function to connect several inputs to the measurement circuits. It provides digital inputs and outputs and general purpose relays and relay coil driver outputs. Some functions are implemented by digitizing and storing waveforms, others are implemented with dedicated circuitry. A floating point Digital Signal Processor is used to perform analysis of digitized data to compute RMS, THD, and any other required mathematical operations. Up to seven expansion I/O boards can be attached to allow eight total I/O boards with one Core Measurement board. An optional three channel High Speed Digitizer can be installed to add additional waveform analysis capability for high frequency signals using NH Powerscope software.

### 2.1.1 Reference Documents

| | | | |
|---|---|---|---|
| Assy. Drawings | : | N.H. #14-0937 | PCA, DMS Relay I/O |
| | | N.H. #14-0938 | PCA, DMS Core Measurement |
| | | N.H. #14-0949 | PCA, DMS High Freq Peak Detector |
| | | N.H. #14-1002 | PCA, DMS High Speed Digitizer |
| | | N.H. #14-1006 | PCA, DMS High Voltage Protection |
| | | N.H. #14-0991 | PCA, DMS HS Dig Analog Module |
| | | N.H. #14-0973 | PCA, DMS High Speed Dig Power Supply |
| | | N.H. #15-1491 | Sub-Assy, Digital Measurement System |
| | | N.H. #15-1544 | Sub-Assy, Powerscope with HS Digitizer |
| Schematics | : | N.H. #10-4180 | Schem, Digital Measurement System |
| | | N.H. #10-4265 | Schem, Powerscope System |
| | | N.H. #16-0266 | Schem, DMS Relay I/O |
| | | N.H. #16-0267 | Schem, DMS Core Measurement |
| | | N.H. #16-0268 | Schem, DMS High Freq Peak Detector |
| | | N.H. #16-0293 | Schem, DMS High Speed Digitizer |
| | | N.H. #16-0286 | Schem, DMS HS Dig Analog Module |
| | | N.H. #16-0275 | Schem, DMS High Speed Dig Power Supply |
| Manuals | : | N.H. #08-0368 | Specification, DMS Software Command |
| | | N.H. #08-0392 | Specification, DMS HS Digitizer Software Command |
| | | N.H. #09-0244 | Manual, emPower 5500 Series User's |
| | | N.H. #09-0247 | Manual, emPower Cal/Diags User's |
| | | N.H. #09-0280 | Manual, HS Digitizer HW Ref. and Maint. |
| | | N.H. #09-0253 | Manual, emPower Test Routine Reference Manual |

## 2.2 Measurement Capabilities

### 2.2.1 Input Multiplexers

The user has a sixteen input multiplexer available for switching multiple signals to the measurement circuits. The multiplexer inputs are isolated and switched differentially, so no two circuits need to share a common ground. There are two separate isolated output channels from the multiplexer, one optimized for High Frequency using transmission line layout considerations, the other used for Low Frequency or DC measurements. Each output channel of the multiplexer feeds an isolated measurement channel with specialized capabilities. This two channel capability allows timing operation to be performed between pairs of user inputs, and allows a two channel isolated digitizing function. If the option is installed, the two multiplexer outputs are available to HS Digitizer Channels One and Two (Channel 3 is a fixed input connection).

The user inputs have high breakdown voltage ratings between other inputs and ground (See Specifications). The multiplexer has fused protection on every input channel to allow for failure of relays or erroneous connections without damage to the circuit board.

An internal solid state multiplexer is provided for system signal measurement. This multiplexer connects isolated inputs to the lower frequency measurement path. The internal multiplexer has a lower isolation breakdown voltage than the user multiplexer inputs (See below).

When expansion Relay I/O boards are installed, the connections for the two multiplexer outputs are made as shown in the figure below. The low frequency output is bussed from one Relay I/O Board to the next using the redundant monitor output connection. The high frequency output of the expansion Relay I/O Board feeds into one of the user inputs on the base Relay I/O Board, thereby reducing the total number of channels available to the user by one. This is necessary to maintain the terminated transmission line characteristics of the 100 MHz channel and avoid reflections that would be caused by stubs or "T" connectors. The DMS firmware detects expansion Relay I/O Boards and handles the daisy chaining control for the high frequency path. This requires the multiplexer channel interconnect to be kept standardized as shown in the diagram. The same pattern is repeated for multiple expansion boards.

User Input Multiplexer Connections

| Connector | Function | Characteristic | Isolation |
|---|---|---|---|
| MUX 1-8<br>MUX 9-16 | User input connections<br>1-16 | 50 OHM differential,<br>500 V switching, 25 W max.<br>Fused at 500 mA | 500 VDC to ground<br>1000 VDC channel-channel |
| J17 | High Frequency<br>Channel Mux Output | 50 Ohm<br>100 MHz 3db bandwidth | 500 VDC to ground and<br>measurement channels |
| Monitor 1<br>Monitor 2 | Low Frequency<br>Mux Expansion | 50 Ohm<br>10 MHz 3db bandwidth | 500 VDC to ground and<br>measurement channels |
| J21 | AC Source Voltage<br>Monitor Input | 500V switching<br>Fused at 500 mA | 500 VDC to ground and<br>measurement channels |
| J22A<br>J22B | Low Frequency<br>Channel Mux Output<br>to Core Measurement | 50 Ohm<br>10 MHz 3db bandwidth | 500 VDC to ground and<br>measurement channels |

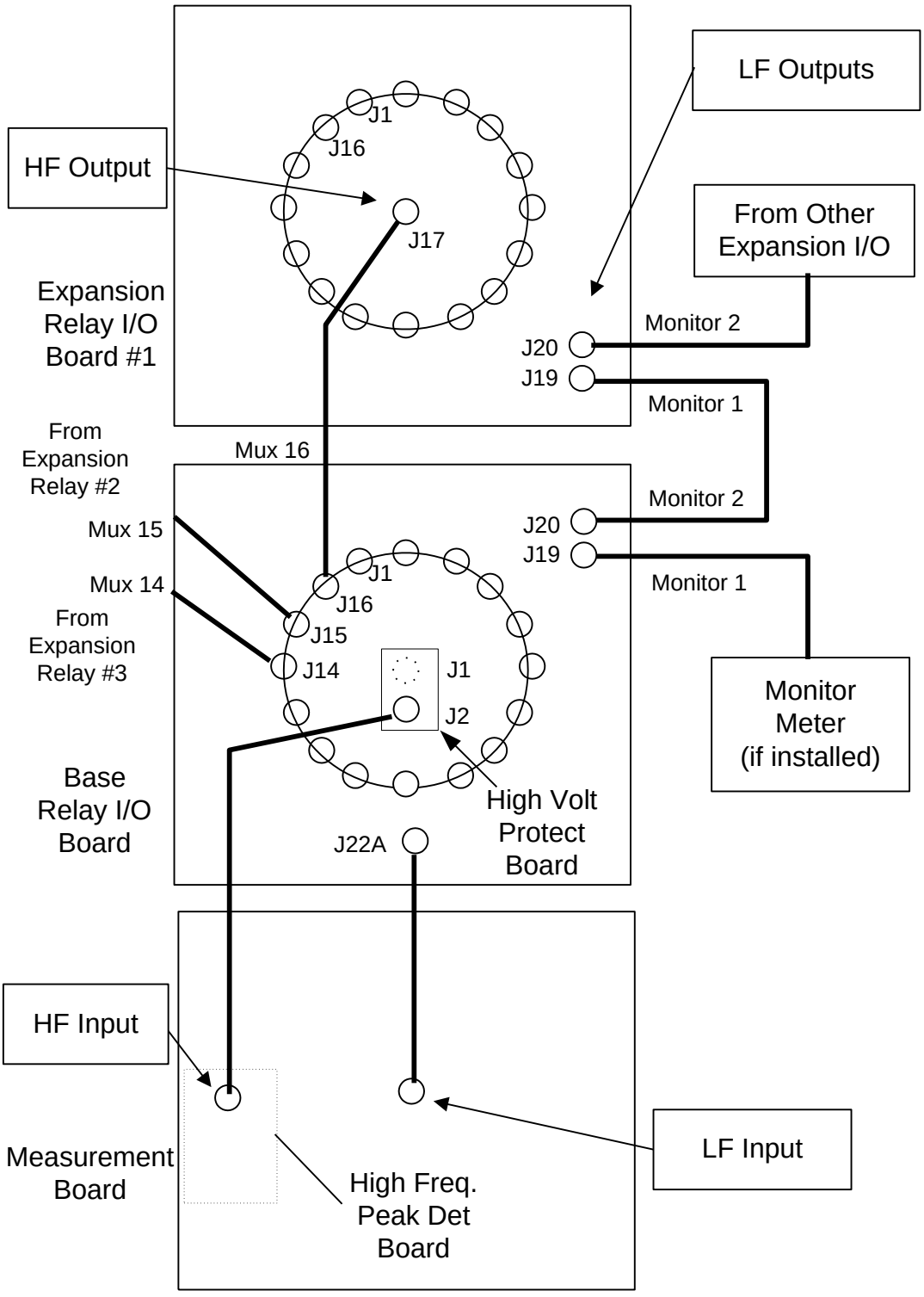



Figure 1 – Multiplexer Connection With Expansion Relay Boards

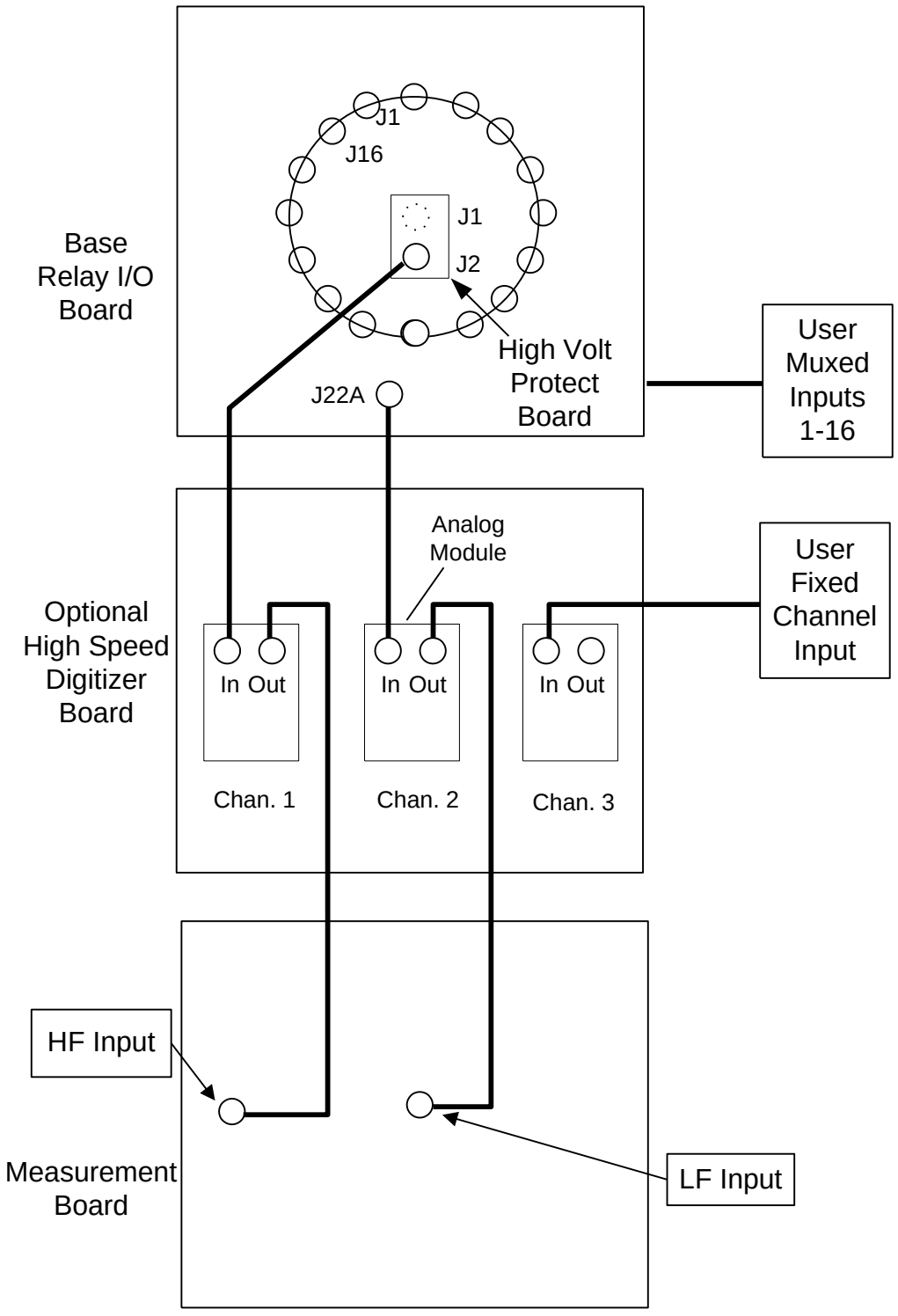



**Figure 2 - Signal Connections With Optional High Speed Digitizer**

### 2.2.2 Internal Multiplexer Connectors

Note: These connectors are located on the Core Measurement Board and are intended for internal system use. The multiplexer channels are distributed across two connectors. Voltage is supplied for powering isolated shunt amplifiers used for current sensing in the system.

Input Characteristic for Internal Mux:
20 KOhm differential input, +/- 5V Maximum peak input full scale with no ranging,
5KHz Bandwidth, 3.125 KHz with Anti-alias filter

Isolation:
100 V Peak channel to channel and channel to ground for open channels.
Selected channel is connected to selected Low Frequency Mux input with 20 KOhm
Power Supplies +/- 15V, sharing a common ground with Low Frequency measurement channel

| Board Connector | Function | Rear Panel Connector Reference |
|---|---|---|
| J4A-1 to 8 | Unused | |
| J4A-9 | Channel 1 negative | J13-9 |
| J4A-10 | Channel 1 positive | J13-10 |
| J4A-11 | Channel 2 negative | J13-11 |
| J4A-12 | Channel 2 positive | J13-12 |
| J4A-13 | Channel 3 negative | J13-13 |
| J4A-14 | Channel 3 positive | J13-14 |
| J4A-15 to 20 | Unused | |
| J4A-21, J44A-22 | -15 VDC | J13-21, J13-22 |
| J4A-23, J44A-24 | Ground | J13-23, J13-24 |
| J4A-25, J44A-26 | +15 VDC | J13-25, J13-26 |
| J4B-1 to 4 | Unused | |
| J4B-5 | Channel 4 negative | J14-5 |
| J4B-6 | Channel 4 positive | J14-6 |
| J4B-7 | Channel 5 negative | J14-7 |
| J4B-8 | Channel 5 positive | J14-8 |
| J4B-9 | Channel 6 negative | J14-9 |
| J4B-10 | Channel 6 positive | J14-10 |
| J4B-11 | Channel 7 negative | J14-11 |
| J4B-12 | Channel 7 positive | J14-12 |
| J4B-13 | Channel 8 negative | J14-13 |
| J4B-14 | Channel 8 positive | J14-14 |
| J4B-15 to 20 | Unused | |
| J4B-21, J44B-22 | -15 VDC | J14-21, J14-22 |
| J4B-23, J44-24 | Ground | J14-23, J14-24 |
| J4B-25, J44B-26 | +15 VDC | J14-25, J14-26 |

### 2.2.3 Low Frequency – High Voltage Measurement Channel

The isolated measurement circuit used for DC and low frequency measurements is connected through the Low Frequency output of the user multiplexer or the Internal multiplexer. A pair of 16 bit A/D converters controlled by a DSP processor capable of sampling at 100 KHz is used for this section. Dual converters are required for synchronously sampling two inputs to compute instantaneous power. This requires one input to be provided to the Internal multiplexer, and the other from the user multiplexer.

The sample rate for this digitizer will be variable with 150 pS resolution. This will allow frequency matching for synchronous sampling of AC line voltages necessary for RMS and THD computations. Sampling can also be done at fixed intervals for waveform capture and display using Powerscope software.

Input to this measurement circuit is DC coupled into a high impedance with ranging provided for line level AC RMS inputs and high voltage DC inputs. The scaled input voltage is available at a comparator input for timing operations using a programmable reference level.

A low pass five pole anti-aliasing filter can be switched in before the digitizer to attenuate frequency components above 3.125 KHz.

### 2.2.4 High Frequency – Low Voltage Measurement Channel

The isolated measurement channel used for AC Peak Noise, Transient Peak Capture, and AC RMS Noise is connected through the high speed output of the user multiplexer. The high frequency content of signals measured in this path requires several specialized circuits. Typically signals input to this channel will have low level DC voltage with high frequency AC noise components. High voltage DC or low frequency AC can be input to this section for timing purposes. The high frequency measurements are AC coupled with input impedance being a function of frequency. Low frequency and DC inputs see a high input impedance. See the High Frequency AC Measurements section for a description of input characteristics.

The AC RMS noise measurement is performed by a special circuit in this channel. An AC coupled pre-amplifier conditions the input signal to drive an RMS to DC converter IC. The output of the RMS to DC circuit is read by a 14 bit A/D converter on the isolated channel. This specialized circuit allows true RMS readings of high frequency noise with a wide range of frequency components without requirements for high sampling rates or large memory storage capacity. The amplified AC coupled input to the converter IC can also be sampled directly for waveform display.

Timing of low frequency transients and pulse widths is performed by a dedicated voltage comparator and reference circuit. Either high voltage DC (with ranged scaling) or amplified AC can be input to the timing comparator.

The scaled DC and amplified AC can also be directly digitized for waveform display on this channel by the 14 bit A/D converter with sample rates up to 125KHz (single channel enabled). Built in firmware uses the digitizing capability to provide transient peak measurements. The Powerscope software can also read waveform data directly to perform other measurements in the host PC.

### 2.2.5 High Frequency Peak Detector PCB (Standard)

The High Frequency Peak detector is a specialized circuit daughter card that plugs into the Measurement Board and receives signals from the High Frequency output of the user MUX. This circuit provides AC coupled low voltage ranging into an ECL comparator circuit that performs a successive approximation algorithm on an input signal. This allows high frequency noise measurement with higher common mode rejection and better resolution than most oscilloscopes. This circuit uses an AC coupled 50 Ohm resistor terminated input to match input cable impedance and avoid errors due to reflections. AC inputs at line frequencies are attenuated to avoid damaging this termination. See High Frequency AC Measurements section.

### 2.2.6 High Speed Digitizer PCB (Optional)

The High Speed Digitizer option for the NH Digital Measurement System provides three eight bit digitizing channels isolated from ground and each other. In addition, it provides 16 channels of digital signal input referenced to one of the channel grounds. This allows high speed digital and analog information to be synchronously captured and displayed with Powerscope software.

The HS Digitizer is implemented as a large PC Board with FPGAs, memory, digital control, and an analog input PCB per channel. With a 200 MSPS sample rate, the HS Digitizer assembly can perform functions that required dedicated circuitry in the Digital Measurement System, such as the peak noise measurement. The HS Digitizer can be installed as an option in the DMS chassis and replace dedicated hardware to perform these functions. The HS Digitizer uses a larger chassis than the original DMS, and requires a separate power supply PCB.

The HS Digitizer communicates with the PC over an IEEE1394 serial bus, it does not use the NH S6000 family interface or protocol. When integrated with the DMS, two of the three channels are connected through the sixteen to two multiplexer, which is controlled using the standard NH6000 serial protocol. The Digital Measurement System emPower driver will incorporate HS Digitizer and multiplexer control to provide the waveform measurement functions.

The sixteen Digital Inputs on the high speed digitizer have fixed LV CMOS level inputs, and are separated on the user interface from the standard DMS Digital Inputs. The eight standard Digital Inputs have programmable thresholds ranging from +/- 10VDC.

This manual describes internal connector pinout and circuitry specifics that will not typically be useful to an end user. The DMS and HS Digitizer are factory wired to a user interface which is documented with a system wiring diagram.

### 2.2.7 Single and Dual Signal Timing

A 32 bit counter-timer is available to measure the time between transitions on the standard Digital Inputs, User multiplexer inputs, or system signals (AC or DC Present, System Trigger). The edge polarity is programmable for all events, and the signal level is programmable on the multiplexer inputs and Digital Inputs. See Specifications for timer resolution and accuracy.

Positive edge triggering from a DIN or multiplexer channel requires that an input pass from below the programmed threshold to above it to initiate the timing sequence. For positive edge trigger on system signals, the input must pass from a low logic level to a high logic level.

Negative edge triggering requires the signal to pass from above to below a threshold, or from logical high to logical low.

The timer has programmable modes for Single Shot or Averaged period measurement. The Averaged method can be used on repetitive events to give a more accurate reading made up of an average of multiple Start to Stop sequence events. If the Start to Stop sequence is non-repetitive (occurs only once), the reading will be the result of a single value. The number of readings averaged is a function of the programmed Aperture time – see the Algorithm section.

To capture only the first occurrence of a repetitive Start/Stop sequence, the Single Shot mode can be used. This forces the reading to result from only the first timing sequence captured, regardless of the programmed Aperture time.

The timing operation is most accurate using the Digital Inputs or System Signal inputs for Start/Stop events. Timing operations from multiplexer inputs have reduced accuracy due to the high impedance inputs and capacitive parasitics causing slight phase shifts. See Specification section for details. DIN inputs can be used for timing only on the first Relay I/O Board if expansion Relay I/O Boards are installed.

## 2.3 Input/Output Capabilities

The Digital Measurement System can be expanded with Expansion Relay I/O Boards. There will be only one Measurement Core Board in any DMS system, but there can be up to eight Relay I/O Boards attached. Only one Relay I/O Board in the system can be used for DIN timing, the others will have their DIN timing drivers disabled. The DIN logic values can be read from any Relay I/O Board.

### 2.3.1 Relay Coil Drivers

Available to the user under program control as outputs, these signals are used to control relays in the test fixture.

> **NOTE: There is no make-before-break, or other delay operation built into the control of these drivers, since the type of relay that can be supplied by the user is unknown. Any required switching delay or settling time must be provided in the user test program.**

A +12 VDC supply fused at 3A is available for user convenience. User can use any other external supply up to 48 VDC for relay coils, but proper polarity must be observed. Individual driver current rating cannot be exceeded and drivers cannot be paralleled. See figure 1.3.1 and 1.3.2 for typical connections.

## Relay Coil Driver Characteristics

| Signal Type | Driver Quantity | Contact Rating | Characteristics | Isolation Rating |
|---|---|---|---|---|
| Relay Driver Output | 16 | 48 VDC Max<br>500 mA Max @40°C<br>Roff: $10^8$ Ohm Min<br>Ron: 1.5 Ohm Max<br>Off State DVDT: 1000 V/uS | Unidirectional FET switch with diode in parallel<br>600W 58 V Peak transient clamp<br>No pull-up | 500 VDC Peak Dielectric Strength to earth ground or measurement channels.<br>Two groups of common relay driver returns. |

## Relay Driver Connector

J24 is a PC mounted female 25 pin DSUB connector. The rear panel designation is J9. Relay drivers are in two groups sharing common returns.

| Pin No. | Function |
|---|---|
| 1 | Relay Driver Return- Group 1 |
| 2 | Relay Driver Coil 1+ Group 1 |
| 3 | Relay Driver Coil 3+ Group 1 |
| 4 | Relay Driver Return- Group 1 |
| 5 | Relay Driver Coil 5+ Group 1 |
| 6 | Relay Driver Coil 7+ Group 1 |
| 7 | Relay Driver Return- Group 2 |
| 8 | Relay Driver Coil 9+ Group 2 |
| 9 | Relay Driver Coil 11+ Group 2 |
| 10 | Relay Driver Coil 13+ Group 2 |
| 11 | Relay Driver Coil 15+ Group 2 |
| 12 | 12VDC– (Ground) |
| 13 | 12VDC– (Ground) |

| Pin No. | Function |
|---|---|
| 14 | 12VDC+ (fused @ 3A) |
| 15 | Relay Driver Coil 2+ Group 1 |
| 16 | Relay Driver Coil 4+ Group 1 |
| 17 | 12VDC+ (fused @ 3A) |
| 18 | Relay Driver Coil 6+ Group 1 |
| 19 | Relay Driver Coil 8+ Group 1 |
| 20 | 12VDC– (Ground) |
| 9 | Relay Driver Coil 10+ Group 2 |
| 22 | Relay Driver Coil 12+ Group 2 |
| 23 | Relay Driver Coil 14+ Group 2 |
| 24 | Relay Driver Coil 16+ Group 2 |
| 25 | Relay Driver Return- Group 2 |

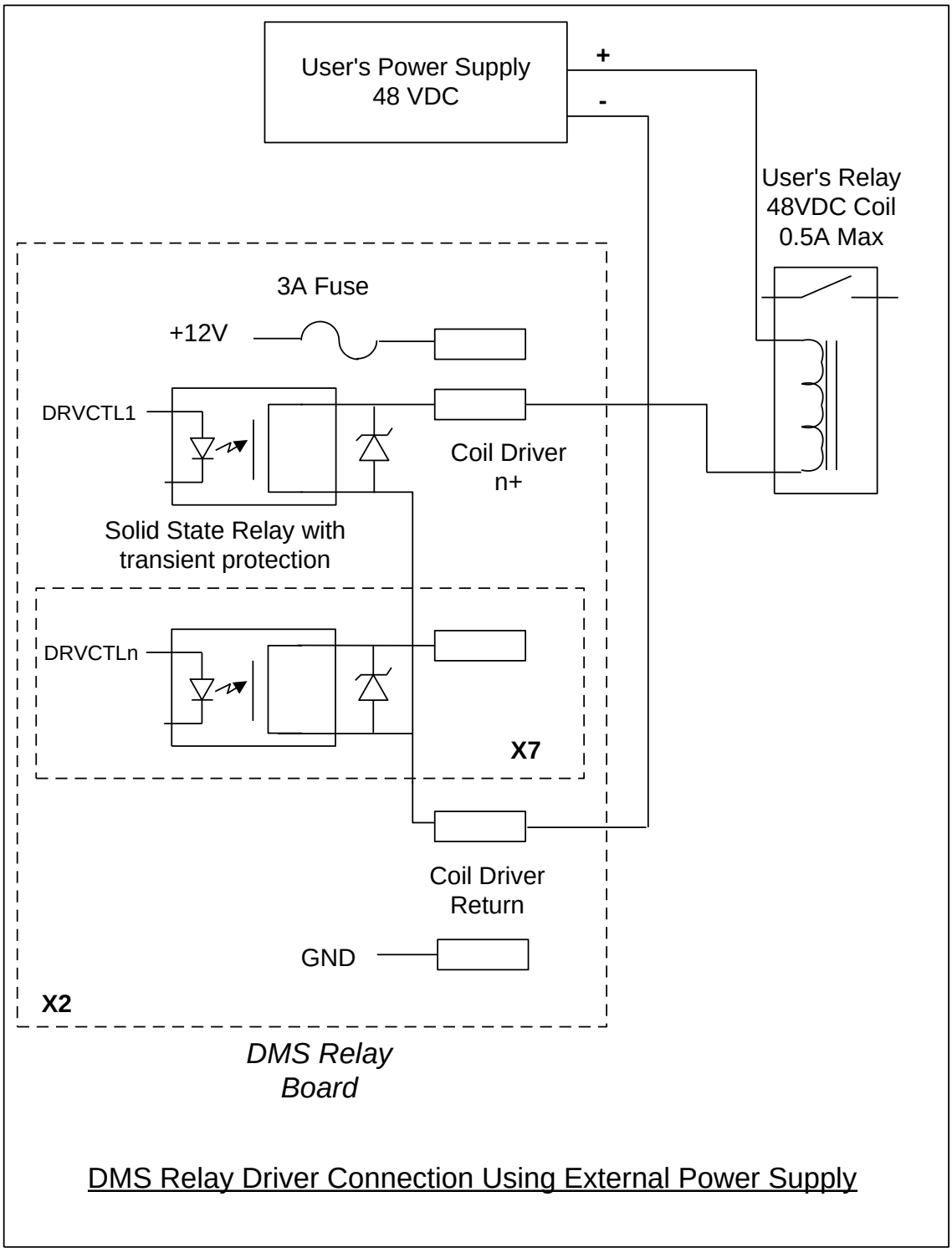
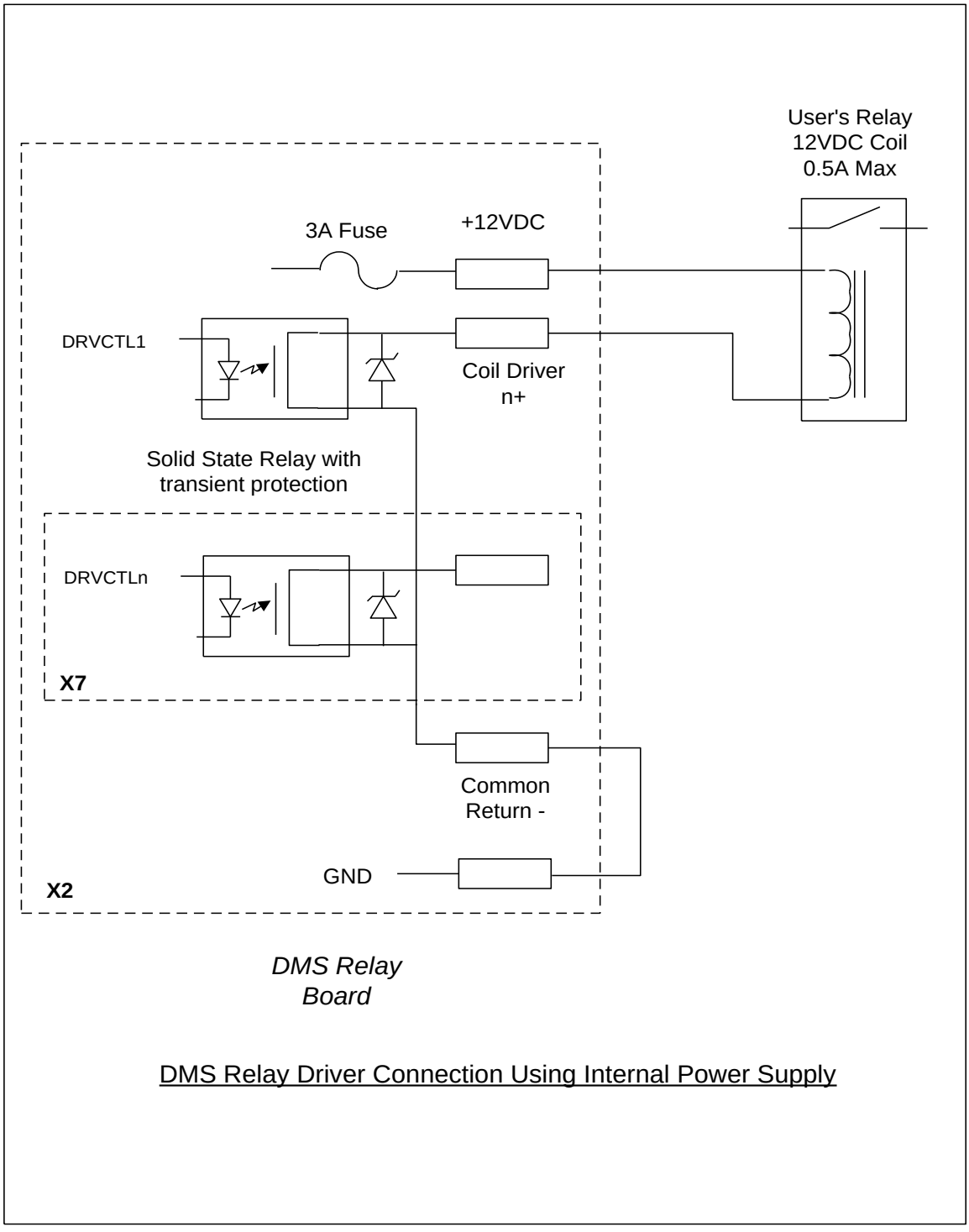



Figure 1.3.1 – Relay Coil Driver Connection With External Power Supply




DMS Relay Driver Connection Using Internal Power Supply

Figure 1.3.2 – Relay Coil Driver Connection With Internal 12VDC Power Supply

### 2.3.2 Digital Outputs

The digital outputs are implemented with solid state relays and have no pull-up resistors or sourcing voltage. They are used like a contact closure between the DOUT pin and the associated return. The low order eight DOUT outputs share a common return, and share a connector with the eight digital inputs. The upper eight DOUTs have individual returns. The default power up condition is for all the Digital Output contact pairs to be low impedance (on). This would give the equivalent of all zeros if pull up resistors were used on the DOUT pins.

Digital Output Characteristics

| Signal Type | Output Quantity | Contact Rating | Characteristics | Isolation Rating |
|---|---|---|---|---|
| Digital Outputs | 16 | 70 VDC Max<br>100 mA Max @50°C<br><br>Roff: $10^8$ Ohm Min<br>Ron: 5.0 Ohm Max<br>Off State DVDT: 1000 V/uS | Bidirectional FET switch<br>No pull-up | 500 VDC Peak Dielectric Strength to earth ground or measurement channels.<br>DOUT 1-8 common return, DOUT 9-16 individual returns. |

Digital Input/Digital Output Shared Connector

J29 is a PC mounted male 25 pin DSUB connector.
The corresponding rear panel designator is J11.

| Pin Number | Function |
|---|---|
| 1 | Digital Output 1 |
| 2 | DOUT Common 1-8 |
| 3 | Digital Output 3 |
| 4 | Digital Output 5 |
| 5 | DOUT Common 1-8 |
| 6 | Digital Output 7 |
| 7 | Unused |
| 8 | DIN Reference 1-4 |
| 9 | Digital Input 1 |
| 10 | Digital Input 2 |
| 11 | Digital Input 3 |
| 12 | Digital Input 4 |
| 13 | DIN Return 1-4 |

| Relay PCB Connector | Function |
|---|---|
| 14 | Digital Output 2 |
| 15 | DOUT Common 1-8 |
| 16 | Digital Output 4 |
| 17 | Digital Output 6 |
| 18 | DOUT Common 1-8 |
| 19 | Digital Output 8 |
| 20 | DIN Reference 5-8 |
| 21 | Digital Input 8 |
| 22 | Digital Input 7 |
| 23 | Digital Input 6 |
| 24 | Digital Input 5 |
| 25 | DIN Return 5-8 |

Digital Output Connector

J28 is a PC mounted male 25 pin DSUB connector.

The corresponding rear panel designator is J10.

| Pin Number | Function |
|---|---|
| 1 | Digital Output 9 |
| 2 | Unused |
| 3 | Digital Output 10 |
| 4 | Unused |
| 5 | Digital Output 11 |
| 6 | Unused |
| 7 | Digital Output 12 |
| 8 | Unused |
| 9 | Digital Output 13 |
| 10 | Digital Output 14 |
| 11 | Digital Output 15 |
| 12 | Digital Output 16 |
| 13 | Unused |

| Pin Number | Function |
|---|---|
| 14 | Digital Output 9 Return |
| 15 | Unused |
| 16 | Digital Output 10 Return |
| 17 | Unused |
| 18 | Digital Output 11 Return |
| 19 | Unused |
| 20 | Digital Output 12 Return |
| 21 | Unused |
| 22 | Digital Output 13 Return |
| 23 | Digital Output 14 Return |
| 24 | Digital Output 15 Return |
| 25 | Digital Output 16 Return |

### 2.3.3 Digital Inputs

The standard Digital Inputs are high impedance comparator inputs for determining a signal's level compared to a +10VDC to –10 VDC programmable reference. Selected DIN inputs can be used for trigger signals or timer start and stop signals. The most accurate timing measurement of a low voltage signal pulse can be made using a single DIN input for the Start and Stop event source. The reference voltage should be set at about half the pulse peak amplitude value for this measurement.

The DIN Reference voltages are brought out on pins for factory testing. These outputs can source approximately 30 mA.

Digital Input Characteristics

| Signal Type | Number | Input Impedance | Characteristics | Isolation Rating |
|---|---|---|---|---|
| Digital Inputs | 8 Total<br>2 sets of 4 | 100 KOhm min.<br>30 pF max.<br>1 MOhm pull-up to +15V<br>Overvoltage protection to 500V | Comparator input with programmable reference level from –10V to +10 VDC.<br>Response time:<br>200 nS | 500 VDC Peak to ground, measurement channels, or other DIN group.<br>DIN 1-4 common<br>DIN 5-8 common |

For DIN connector pinout, see shared DIN/DOUT connector table above.

### 2.3.4 General Purpose Relays

These relays are typically used to control test fixture and UUT operation. Each relay has two sets of DPDT contacts. The default power up condition is for all the Normally Open contacts to be open.

**NOTE: The DMS firmware does <u>not</u> enforce break before make operation on these relays. Although settling-time delay is provided, users should select Normally Open and Normally Closed contacts in their fixturing with these considerations in mind. Care should be taken to include delays in the test program if the fixture uses other contact configurations and potentially damaging shorts could occur.**

<u>General Purpose Relay Characteristics</u>

| Signal Type | Number | Contact Rating | Characteristics | Isolation Rating |
|---|---|---|---|---|
| General Purpose Relay Contact | 8 DPDT | 5A,30VDC<br>120VAC/240VAC<br>1/3 HP @ 120VAC<br>1/2 HP @ 240VAC | 10M operations at no load<br>200K operations at full resistive load | 500 VDC Peak Dielectric Strength to earth ground or measurement channels |

## General Purpose Relays 1-4 Connector

J18 is a PC mounted female 25 pin DSUB connectors.
The corresponding rear panel reference is J7.

| Pin Number | Function |
|---|---|
| 1 | GP Relay 3 – Common #1 |
| 2 | GP Relay 3 – NC #1 |
| 3 | GP Relay 4 – NO #1 |
| 4 | GP Relay 4 – NC #2 |
| 5 | GP Relay 4 – Common #2 |
| 6 | GP Relay 3 – NO #2 |
| 7 | |
| 8 | GP Relay 1 – NO #1 |
| 9 | GP Relay 2 – Common #1 |
| 10 | GP Relay 2 – NC #1 |
| 11 | GP Relay 2 – NO #2 |
| 12 | GP Relay 1 – NC #2 |
| 13 | GP Relay 1 – Common #2 |

| Pin Number | Function |
|---|---|
| 14 | GP Relay 3 – NO #1 |
| 15 | GP Relay 4 – Common #1 |
| 16 | GP Relay 4 – NC #1 |
| 17 | GP Relay 4 – NO #2 |
| 18 | GP Relay 3 – NC #2 |
| 19 | GP Relay 3 – Common #2 |
| 20 | GP Relay 1 – Common #1 |
| 21 | GP Relay 1 – NC #1 |
| 22 | GP Relay 2 – NO #1 |
| 23 | GP Relay 2 – NC #2 |
| 24 | GP Relay 2 – Common #2 |
| 25 | GP Relay 1 – NO #2 |

## General Purpose Relays 5-8 Connectors

J23 is a PC mounted female 25 pin DSUB connectors.
The corresponding rear panel reference is J8.

| Pin Number | Function |
|---|---|
| 1 | GP Relay 7 – Common #1 |
| 2 | GP Relay 7 – NC #1 |
| 3 | GP Relay 8 – NO #1 |
| 4 | GP Relay 8 – NC #2 |
| 5 | GP Relay 8 – Common #2 |
| 6 | GP Relay 7 – NO #2 |
| 7 | |
| 8 | GP Relay 5 – NO #1 |
| 9 | GP Relay 6 – Common #1 |
| 10 | GP Relay 6 – NC #1 |
| 11 | GP Relay 6 – NO #2 |
| 12 | GP Relay 5 – NC #2 |
| 13 | GP Relay 5 – Common #2 |

| Pin Number | Function |
|---|---|
| 14 | GP Relay 7 – NO #1 |
| 15 | GP Relay 8 – Common #1 |
| 16 | GP Relay 8 – NC #1 |
| 17 | GP Relay 8 – NO #2 |
| 18 | GP Relay 7 – NC #2 |
| 19 | GP Relay 7 – Common #2 |
| 20 | GP Relay 5 – Common #1 |
| 21 | GP Relay 5 – NC #1 |
| 22 | GP Relay 6 – NO #1 |
| 23 | GP Relay 6 – NC #2 |
| 24 | GP Relay 6 – Common #2 |
| 25 | GP Relay 5 – NO #2 |

## 2.4 Measurement Algorithms

### 2.4.1 Channel Setup

Based on the idea that user inputs to the multiplexer will generally be fixed to certain UUT outputs, a set up vector is kept in DMS memory for each channel. This set up vector has frequency and range information for the characteristics of the input signal that should rarely need to be modified during test execution. DMS firmware will use the fields of the setup vector to determine the best method, or dedicated circuit, to use to make a measurement.

The set up parameters that effect measurement execution are Bandwidth Limit and Voltage Ranges. The table below shows how channel setting affects readings.

Channel Set Up Parameters Effecting Measurement Methods

| Set Up Parameter | Measurement Type | Criteria | Effect |
|---|---|---|---|
| Bandwidth Limit | Timing/Frequency | <1KHz or < 10 KHz | Use High Frequency output of Mux for filtered signal path, even if Start event forced to low frequency channel |
| AC Voltage Range | AC RMS volts | >=14 VRMS | Sample waveform synchronously and compute RMS<br>Bandwidth 40-500Hz<br>16 bit reading from low frequency measurement channel |
| AC Voltage Range | AC RMS volts | <14 VRMS | Use AC Preamp and RMS to DC converter IC<br>Bandwidth 5KHz-1MHz<br>14 bit reading from high frequency measurement channel |

### 2.4.2 DC Voltage Readings

This is an averaging type of measurement used for DC Voltage, Maximum Voltage, Minimum Voltage, and DC Current. In this measurement, the Aperture value specified is used to determine how many readings can be taken at the maximum sample rate of the A/D converter. The DSP firmware sets up a counter in the measurement control structure for the allowed number of readings. When the Measure function begins, the computed number of readings taken at the maximum rate is summed. The final sum is divided by the sample count and calibrated to produce the final answer. The maximum and minimum sample values are updated and saved during the summing process so that their values are available if requested.

The user can increase the programmed Aperture time to increase the number of samples averaged to reject random noise. If a less accurate reading is sufficient, the Aperture time can be

reduced to a minimum of two sample periods. The default Aperture size provides for one hundred samples, the minimum required to meet the stated accuracy.

DC voltages are read using the 16 bit A/D converters on the low frequency measurement channel. If the voltage source specified is one of the user multiplexer inputs, or the AC Source voltage input, the Voltage A/D converter is used. If the source is an internal system multiplexer channel or the AC source current readback, the Current A/D converter is used.

### 2.4.3 AC Line Voltage and Frequency Readings

AC voltage readings use a synchronous sampling technique to capture waveform cycles and compute the RMS value explicitly from the samples taken. This same captured data can be used for THD and FFT computation. Synchronous sampling requires the DMS timing circuit to determine the period of the input signal and set the sampling rate to an exact binary multiple of the waveform frequency. The timing comparator edge threshold is set at 50% of range initially, and lowered after several cycles to 50% of the dynamically sampled peak value if no start event has occurred. The threshold is not set at zero due to excessive transitions near zero in many UUT simulated sine wave outputs.

Every input waveform cycle is sampled and timed. Sampled cycles are flagged valid if the period measured matched the synchronous sample rate during that cycle within a small timing error tolerance. If any cycles are valid at the end of the aperture period, all cycles captured after the first valid one are used in the RMS calculation. If no cycles are valid, then all cycles are used in the calculation so a value of some kind can be returned.

Memory is allocated dynamically to store the sampled cycles based on the Expected Frequency value in the Channel Set Up parameter and the Aperture time specified. Enough memory space is allocated to hold 128 samples for each of the number of expected cycles that would fit in the programmed Aperture time. A maximum of 400 cycles can be stored (400 Hz for one second), if sufficient memory is available. Increasing the Aperture time will not increase the number of cycles averaged beyond this limit. The number of cycles averaged within an Aperture time can vary depending on the amount of time required to find a valid threshold for period measurement, and lost cycle time due to synchronization. The number of cycles sampled will typically be something less than half of the possible cycles within an aperture period due to DSP processing overhead between cycles.

The frequency measurement for line frequency voltages uses this same measurement routine. The frequency value is computed as an average of the period measurements of each of the sampled cycles during the entire aperture. All non-zero measured period values are averaged. If a frequency value of zero is returned, it indicates a DC input or no signal present.

### 2.4.4 Timing Measurements

Timing measurements use a 32 bit counter internal to the DSP processor, with external state machine logic to select start and stop event edges to gate a clock to this counter. This state machine enforces the edge requirement that a condition must be false before it transitions true to initiate an event. Polarity is programmable on both Start and Stop events, so that either logic state of the input can made true. A Start event must occur before a Stop event will be detected, and the Stop event must have the false-true transition after the Start event has happened.

Timing measurements will normally use two inputs for Start and Stop events. If both of these signals are connected to the user multiplexer input, then one is routed through the High Frequency Mux output, and the other through the low frequency output. Separate timing comparators are provided on the low and high bandwidth measurement channels, each with its own ranging input and programmable reference level. This allows timing to be performed between any two user inputs of low or high voltage, with isolation maintained between the signals.

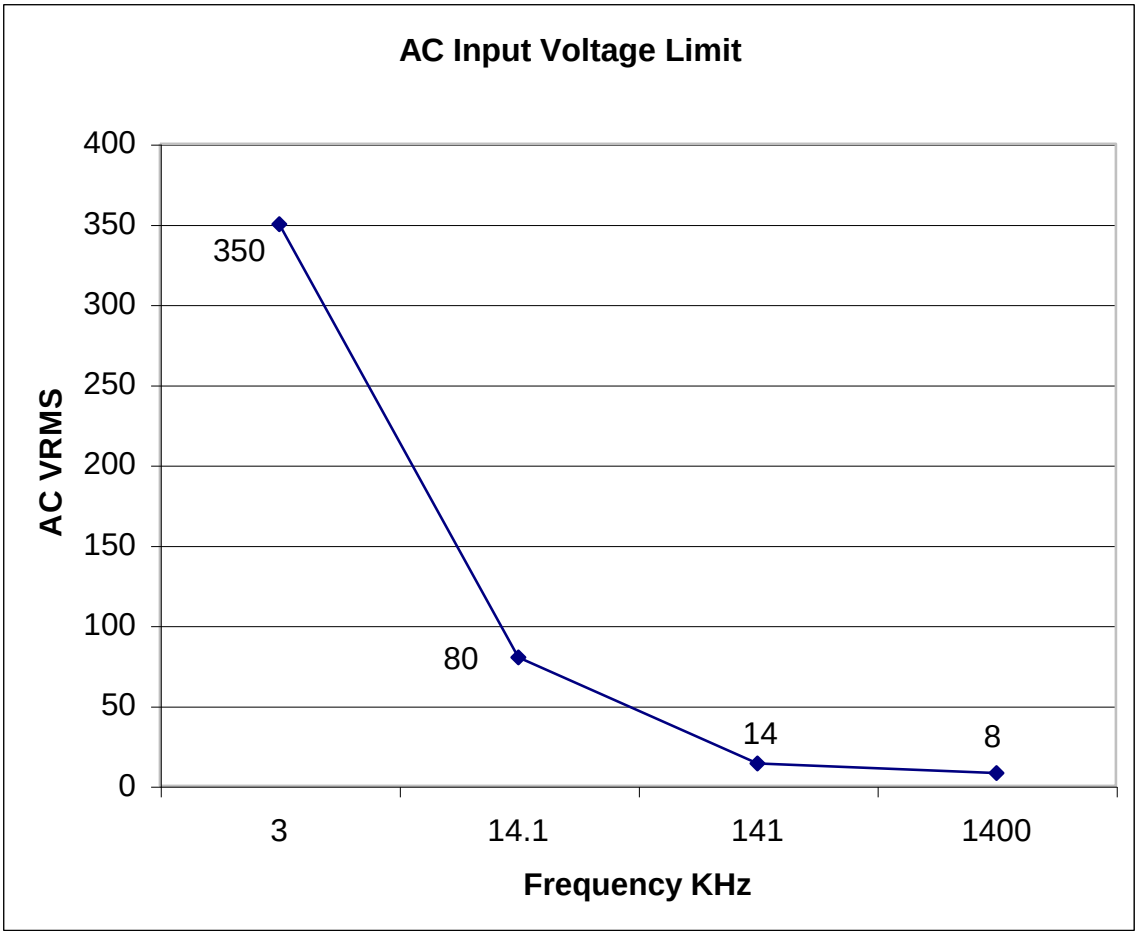
The algorithm for selecting whether the Start or Stop event is routed through the Low or High Frequency Mux output takes into account differing capabilities on the two measurement channels. If a bandwidth limit is required on an input signal, the High Frequency signal path is used since it has programmable roll-off filtering. Other than this special case, the general rule is to use the High Frequency output first and the Low Frequency output last. If only one Mux input is used in a timing operation, the High Frequency Output will be used whether it is the Start or Stop event. The lowest numbered User Mux channel is assigned first, and will typically be assigned to the High Frequency output, and the next higher User Mux number will go to the Low Frequency Mux output.

Other system inputs that can be used for timing operations include selected Digital Inputs, AC Present, and DC Present. AC and DC Present are internal system logic signals with their timing accuracy dependent on the source. The DIN inputs have thresholds programmable in a single low voltage range, and offer the most accurate timing operation for small amplitude signals.

The timing operation normally performs an averaged reading on multiple cycles of a repetitive waveform. The Aperture setting determines how much time the Start and Stop edge detecting state machine has to reset and retry to capture cycles. If multiple cycles do complete, they are averaged to provide the final reading. If a reading from a single cycle is desired, the Single Shot mode can be used to keep the Start/Stop sequencer from recycling regardless of aperture length.

### 2.4.5 High Frequency AC Measurements

Noise measurements are taken with specialized circuits - optimized for small amplitude, high frequency AC voltages with DC offsets that are much larger than the noise level. These circuits use AC coupling to reject any DC offset and utilize the High Frequency Mux output channel. They also rely on the low frequency blocking characteristic of the input capacitor to protect them from damage at line AC voltage. Any input with high frequency components must have limited voltage amplitude to avoid overheating the ranging and terminating resistors. See the safe input range graph below. This limit applies to any signal connected to the user multiplexer. Normal line voltages of 400 Hz or less pose no problem. Signals with higher frequencies of 1.4 MHz and above with RMS amplitudes over 8 Volts will need to be externally attenuated.




The AC RMS noise circuit has a blocking capacitor to reject frequencies below 5 KHz, and a pre-amplifier to boost high frequency noise within the 1 MHz frequency bandwidth. An RMS to DC converter IC is used to measure the amplified input noise, and a 14 bit A/D converter reads the resulting DC value.

High frequency peak noise is measured with either the standard Peak Noise Detector board, or the optional High Speed Digitizer board. Both have a 100 MHz frequency bandwidth (3db down). At these frequencies, maintaining a transmission line signal path from the UUT to the measurement device requires special consideration to keep reflections and common mode noise from corrupting any measurements. The signal is AC terminated to 50 ohms at the input to the peak circuit to match input cable impedance.

The standard Peak Noise Detector is a surface mount daughter card, which mounts on the Core Measurement Board and receives input from the High Frequency Mux output. An ECL comparator and programmable reference are used to perform a successive approximation routine on the input signal to determine the level of the most positive and most negative peak. The Expected Frequency channel setup parameter is used in this case to describe the lowest frequency component of interest. This parameter determines the waiting period at each step in the successive approximation routine. Time for two periods of the lowest frequency of interest is allowed between each successive step.

The optional High Speed Digitizer captures data at 200 MSPS performing real time hardware peak detection for noise signals. The expected frequency is used to determine a measurement aperture for the digitizing operation. The Analog module of the HS Digitizer provides the same AC Coupling and 50 Ohm AC termination provided by the standard Peak Noise Detector, and has more ranging and gain for low level signals.

### 2.4.6 Power Measurement

The DMS takes active power readings by simultaneously sampling voltage from the User Mux input (or the system AC Source monitor input) and a current signal from the Internal Mux. Dual 16 bit A/D converters provide two data values, which are saved for later multiplication and processing. This is a simultaneous sampled reading synchronized to the voltage input. Power is computed on a cycle by cycle basis, with multiple cycle values averaged to provide the reading. The Aperture can be extended to increase the number of sampled cycles. See the description of AC Line Voltage and Frequency Readings algorithm above for details on the synchronizing and memory storage functions.

Power measurements for multi-phase AC sources can be made by selecting pairs of input signals from the User Mux and Internal Mux that sense voltage and current for successive phases, and reading each phase in turn.

The Internal Mux has no ranging on its inputs, so external shunt amplifier gain and shunt rating are used to scale the expected full scale current sensing voltage to +/- 5.0V Peak. This external scaling circuitry should be able to accommodate whatever crest factor is anticipated on AC current sensing waveforms to keep the peak voltage under this limit.

### 2.4.7 Waveform Capture and Transient Measurements

The built in measurement capability of the standard DMS allows calculations to be done locally on captured data so that only the resulting measurement is returned to the host PC. This minimizes data transmission time, but users still have the option of transferring all captured waveform data to the host PC for display or further processing. The standard DMS can capture small sample buffers of 4096 samples for each of two channels, and transmit them over the standard NH 6000 serial bus. The standard DMS has limed capture mode and trigger point position options. Sample rates are adequate for moderate speed transient captures, ranging from 100 KHz to 125 KHz maximum. There are two isolated channels available, although there are restrictions on what input coupling selections are available with both channels enabled.

The hardware path used for waveform capture in the standard DMS varies with the type of operation selected. A high priority is placed on using the hardware with the greatest bandwidth whenever possible. If a single channel waveform capture is selected, the High Frequency output of the Mux is used to pass the signal to a 14 bit A/D converter sampling at 125 KSPS. If two channel capture is selected, the Low Frequency output of the Mux must be used to pass a signal to the 16 bit A/D converter that has a maximum sample rate of 100 KSPS, which becomes the sample rate on both channels. The High Frequency Mux output is assigned by the DMS firmware to the User Mux input with the lowest channel number, then the Low Frequency Mux output will

go to the higher numbered channel. Users may wish to construct their test fixturing so that higher bandwidth signals are on lower number User Mux inputs to take advantage of this operation.

The standard DMS digitizer also has limited AC/DC coupling capability. If AC coupling is required, only one channel can be enabled for capture and the trigger is also AC coupled. Only low amplitude signals can be measured when AC Coupled, with an upper range of 5 VRMS.

The standard DMS Transient Peak measurement uses a single channel waveform capture function, and uses the 125 KSPS capture rate on an AC coupled signal read from the High Frequency Mux output.

The High Speed Digitizer provides more memory, faster sample rates, and more sampling and triggering options than the standard DMS waveform capture. Each channel can be independently AC or DC coupled, and Digitizer channels have a fixed relationship to MUX outputs so there is no ambiguity about hardware paths. The High Frequency Mux output is connected to High Speed Digitizer Channel 1, the Low Frequency Mux output to Digitizer Channel 2. Digitizer Channel 3 and the 16 Digital Inputs are brought to the user interface directly without switching or multiplexing.

Each channel of the High Speed Digitizer has 8Mbyte of sample storage with factory options for 16 or 32 Mbytes. Capture can be performed in peak, sampled, or averaged modes. Trigger can be positioned anywhere in the waveform aperture. See the Waveform Test Routine section of NH Document 09-0253 Manual, emPower Test Routine Reference Manual, for a full description of waveform test capabilities.

Both standard and optional High Speed Digitizer share the same restrictions in trading-off sample rate for memory size. When the aperture (seconds/division) is increased so that the amount of allocated memory isn't sufficient to hold enough samples at the maximum sample rate, the sample rate is effectively reduced by storing only a subset of captured samples and discarding the rest. The effective sample rate is displayed on the waveform "scope" panel display so that users can be aware of loss of timing resolution.

## 2.5 DMS Configuration Setup

### 2.5.1 Relay I/O Board Configuration Jumpers

Jumpers are provided on the Relay I/O Board for addressing and configuration. This allows each expansion I/O Board to be uniquely addressed and provides a way for software to determine any special features of the board. The first relay board is at address 0. Any expansion Relay I/O Boards are at addresses which increase by one sequentially. Timing operations can only use the DIN inputs on the board at address 0.

The W5-W8 jumpers are encoded as follows;

Relay I/O Board Address Jumpers

| W5 | W6 | W7 | W8 | Board Address | Function |
|---|---|---|---|---|---|
| X | 0 | 0 | 0 | 0 | Standard I/O Board |
| X | 0 | 0 | 1 | 1 | Expansion I/O Board 1 |
| X | 0 | 1 | 0 | 2 | Expansion I/O Board 2 |
| X | 0 | 1 | 1 | 3 | Expansion I/O Board 3 |
| X | 1 | 0 | 0 | 4 | Expansion I/O Board 4 |
| X | 1 | 0 | 1 | 5 | Expansion I/O Board 5 |
| X | 1 | 1 | 0 | 6 | Expansion I/O Board 6 |
| X | 1 | 1 | 1 | 7 | Expansion I/O Board 7 |

(0 = jumper installed, 1 = jumper removed )

Relay I/O Board Configuration Jumpers

The PCB revision configuration jumper is for internal use by the DSP firmware.

| Jumper | Function | Encoding |
|---|---|---|
| W9 | Solid State Scan Multiplexer Option | 0 = mux relays only, 1 = mux with SSR scanner |
| W10 | Unused | |
| W11 | Unused | |
| W12 | PCB Revision | 0= Revision A PCB, 1= Any later revision |

(0 = jumper installed, 1 = jumper removed )

### 2.5.2 Core Measurement Board Configuration Jumpers and Switches

Jumpers on the core board are used for test and debug and to enable operations that may be optional.

The RS232 serial interface has configuration jumpers to enable the transmit line received from the PC to drive the S6000 bus. This allows the PC to control downstream S6000 devices using the PC RS232 port. If the DMS is to be controlled by an upstream S6000 device, the jumpers must be in the other position.

Serial Communication Interface Configuration Jumpers

| Config Jumpers | Position | Function |
|---|---|---|
| W5/W6 | A (furthest from U10) | DMS controlled by RS232, but control not passed to other S6000 devices |
| W5/W6 | B (nearest U10) | DMS controlled by RS232 and passed to other S6000 devices |
| W1-W4 | Not Applicable | These jumper positions are not presently for configuration functions, but provide access points to S6000 interface signals for future enhancements. |

Address and Configuration Switch Settings

The Address Switch must be set to a unique value within the S6000 system. The DMS will respond only to commands at the selected address, or to broadcast commands, per the NH Research S6000 Protocol specification. Address 0 is used for a special boot operation for FLASH memory fault recovery. When the address is set to 0, the onboard microcontroller will run only from the boot EPROM and can download to corrupted FLASH memory.

| Switch Number | Function |
|---|---|
| SW1-SW6 | S6000 Address. LS Bit = SW1, MS Bit = SW6, Off = 1, On = 0 |
| SW7 | Spare |
| SW8 | Baud Rate Setting, On = 38400, Off = 19200 |

Watch Dog Timer Configuration Jumper

If this jumper (W10) is installed, the microcontroller is reset every 1.6 seconds if a software routine doesn't toggle a control strobe. If the jumper is removed, the watchdog timer is disabled. The jumper is installed (or not) at the factory and shouldn't be modified by the user.

## 2.6 System Control Interfaces

### 2.6.1 Front Panel Interface

The Relay I/O Board includes an interface for a user control panel made up of pushbuttons and indicator lights. Power for the lights and holding relay coil activated by the Power On button is provided by a low voltage AC transformer elsewhere in the system. Other system interlock connections must be made before the holding relay will be energized. Control signals from other error sensing sources in the system can break the holding relay circuit to shut off power to the system.

The front panel control pushbuttons and indicator lights are connected via a redundant connector pair (J35A/J35B) to the front panel 'System Control' DSUB connector to provide remote control capabilities. The mating connector parts for the 'System Control' connector are:

| NH Part # | Description | Manufacturer Part # |
|---|---|---|
| 6200799 | Conn, Dsub 15 Pin Socket | ITT Cannon DA15-P |
| 6200800 | Conn, Dsub Shell 'A' size | ITT Cannon DA24658 |
| 6201309 | Conn, Dsub Screw Lock .25" | ITT Cannon D20419-21 |

The connections to the Front Panel Interface are described on the following pages.

## Test Control Interface Connections

Note: This interface is isolated to 500 V peak from the measurement channels and earth ground. It is referenced only to the externally supplied low voltage AC source.

| J35 Pin * | Characteristic | Function |
|---|---|---|
| 1 | Open Collector Output to FPANEL Rtn | Fail Indicator Lamp, Low True |
| 2 | Open Collector Output to FPANEL Rtn | Pass Indicator Lamp, Low True |
| 3 | Open Collector Output to FPANEL Rtn | Busy Indicator Lamp, Low True |
| 4 | Open Collector Output to FPANEL Rtn | Ready Indicator Lamp, Low True |
| 5 | 24VDC FPANEL source | Positive side of rectified low voltage AC, common supply to indicator lights |
| 6 | Input with 10K pull-up to FPANEL 24VDC | Stop Switch, set by momentary connect to FPANEL Rtn |
| 7 | FPANEL Rtn | Return for logic signals and power, common sink to Start and Stop switches |
| 8 | Input with 10K pull-up to FPANEL 24VDC | Start Switch, set by momentary connect to FPANEL Rtn |
| 9 | Open Collector Output to FPANEL Rtn | Stop Indicator Lamp, Low True |
| 10 | Open Collector Output to FPANEL Rtn | Start Indicator Lamp, Low True |

* Note: Pin Numbers are same for J35A/B and 'System Control' DSUB

## Utility I/O Connector

This connector groups several system control and voltage signals into a single connector.

| PCB Connector | Rear Panel Utility I/O Connector | Characteristic | Function |
|---|---|---|---|
| J34-1 | J6-1 | 24 VAC input high side | Powers front panel interface section |
| J34-2 | J6-2 | 24 VAC input low side | Powers front panel interface section |
| J34-3 | J6-3 | 24 VAC switched | 24 VAC input high side returned through Power On momentary switch and holding relay contact |
| J32-1 | J6-4 | 5 VDC from alarm circuit | Supplies power to coil of kill relay |
| J32-2 | J6-5 | Return from alarm circuit | Supplies power to coil of kill relay |
| | J6 – 6, 7,8,9 | Spare | |
| J21-1 | J6-10 | 120-240 VAC | AC Source Line In |
| J21-2 | J6-11 | 120-240VAC | AC Source Line In |
| | J6 – 12 | Spare | |

## Front Panel Power Control Connections

| Pin | Characteristic | Function |
|---|---|---|
| J33-1 | 24 VAC supply high side | Power for front panel interface section |
| J33-2 | 24 VAC switched | 24 VAC input high side returned through Power On momentary switch and holding relay contact |
| J33-3 | 24 VAC supply low side | Power for front panel interface section |
| J33-4 | Current limited 24 VAC | Power for dimmed Power Off indicator light |
| J33-5 | 24 VAC high side interlocked return | Power for holding relay through interlock switch circuit |
| J33-6 | FPANEL ground | Rectified supply ground |

### 2.6.2 Current Loop Control Interface

Connectors are provided on the DMS core board to transmit and receive commands and data via a 20 mA current loop serial communication interface to legacy instruments. Each of the return inputs from these instruments is isolated with optocouplers. All these optocoupler outputs are tied together to form a wired-or function. The common control output signal to these legacy devices is referenced to the measurement channel and isolated at the receiving end.

PC connector J5 is a 2x13 pin header
Corresponding rear panel reference is J16

| Pin | Characteristic | Function | Isolation |
|---|---|---|---|
| 1 & 2 | Spare | | |
| 3 | 20 mA current limited 5VDC | Serial communication data TX | 100 VDC to ground<br>100 VDC channel to channel |
| 4<br>6 | 5VDC | High side for receiving end optocouplers | same as above |
| 5 | 20 mA current limited 5VDC | Serial communication address TX | same as above |
| 7+/8- | same as above | data rx – AC source | same as above |
| 10+/9- | same as above | data rx – Load 4 | same as above |
| 12+/11- | same as above | data rx – Load 5 | same as above |
| 14+/13- | same as above | data rx – Load 6 | same as above |
| 16+/15- | same as above | data rx – Load 7 | same as above |
| 18+/17- | same as above | data rx – Load 8 | same as above |
| 20+/19- | same as above | data rx – OVPS | same as above |
| 22+/21- | same as above | data rx – Load 1 | same as above |
| 24+/23- | same as above | data rx – Load 2 | same as above |
| 26+/25- | same as above | data rx – Load 3 | same as above |

### 2.6.3 S6000 Control Interface Connection and Configuration

The DMS can be controlled using the NH Research S6000 Family serial interface. It can join with other instruments in this family anywhere along the communication "chain". It has an RS232 signal translator, and is capable of providing translation from a PC RS232 port to the S6000 RS422/485 differential signal protocol. Configuration jumpers must be set on the Core Measurement Board to enable or disable the RS232 translation function. See the Core Measurement Board configuration section. The DMS should either receive control commands from an RS232 cable from a PC, or from the J8 COMM IN connector from the S6000 bus. It should not receive RS232 and COMM IN control input at the same time.

S6000 Serial Communication Interface Connections

PC connector J8
Corresponding rear panel reference for Communication Output J20
Corresponding rear panel reference for Communication Input J21

| | COMM OUT - FEMALE | | COMM IN - MALE |
|---|---|---|---|
| 1 | TX_IN- | 1 | TX_IN- |
| 2 | TRIGIN+ | 2 | TRIGIN+ |
| 3 | 10 OHM to GND | 3 | GND |
| 4 | TX_IN+ | 4 | TX_IN+ |
| 5 | INTLKIN+ | 5 | INTLKIN+ |
| 6 | INTLKIN- | 6 | INTLKIN- |
| 7 | LCLOUT0+ | 7 | LCLIN0+ |
| 8 | LCLOUT- | 8 | LCLIN0- |
| 9 | RX_IN- | 9 | RXOUT- |
| 10 | TRGOUT+ | 10 | TRGOUT+ |
| 11 | TRGOUT- | 11 | TRGOUT- |
| 12 | RX_IN+ | 12 | RXOUT+ |
| 13 | TRIGIN- | 13 | TRIGIN- |
| 14 | LCL1OUT+ | 14 | LCLIN1+ |
| 15 | LCL1OUT- | 15 | LCLIN1- |

Signal levels on this connector are differential with levels conforming to RS422 specification. GND refers to earth referenced ground (non-isolated). Communication protocol is described in the NH Research S6000 Interface Specification.

### 2.6.4 RS 232 Interface Connection

This connector pinout will mate with a PC compatible nine pin RS232 port if a one-to-one cable is used. Jumpers inside the source must be set to enable passing RS232 controls to other instruments. The RS232 cable should not be connected if the DMS is under S6000 bus control, or if there is another possible return to earth ground somewhere in the system S6000 bus.

The ground connection in this interface is fused with a socketed 1A fuse near the J17 connector. If the interface will not operate after a large power transient, the fuse may need to be replaced.

PC connector J17, corresponding rear panel reference J22

| Pin | Description |
|---|---|
| 1 | No Connect |
| 2 | RXOUT – output from DMS to PC |
| 3 | TXIN – input from PC to DMS |
| 7 | RTS – input from PC used for trigger signal |
| 5 | GND – fused at 1A, possibly tied to earth on PC |

Signal levels on this connector conform to RS232C signal levels.

### 2.6.5 User Trigger Input/Output Connection

| Connector | Description |
|---|---|
| J12 Trigger In | Negative true TTL level signal with 1K Ohm pull-up to +5V supply referenced to communication ground (earth ground) |
| J13 Trigger Out | Positive true TTL level output, 74VHC14 with 50 Ohm series resistor |

Mating Connector type is;

| NH Part | Description | Commercial Part # | Manufacturer |
|---|---|---|---|
| 6200262 | SMB Co-ax 50 Ohm | 131-1403-016 | EF JOHNSON |

This connector is used with RG178 type 50 ohm co-axial cable.

### 2.6.6 Core Measurement to Relay PCB Control Interface

A parallel interface having differential signal pairs is used by the DMS Core Measurement Board to control the DMS Relay I/O Board. This interface uses 8 address lines, 8 data lines, and 3 control lines arranged in the same configuration as the NH IOP legacy bus. This bi-directional interface allows operation of multiple Relay I/O expansion boards (up to 8 total including the base Relay I/O unit. Only the base Relay I/O board can drive the two signal pairs used for DIN timing control. The cable must break these wires between the base board and any expansion Relay I/O Boards.

Core Measurement to Relay I/O Board Connections

The PCB connector J27 is a 2X25 ribbon cable header.

The corresponding rear panel connector reference is J1.

| Pin | Description | Pin | Description |
|---|---|---|---|
| 1 | Ground | 26 | A3- |
| 2 | Ground | 27 | A4+ |
| 3 | D0+ | 28 | A4- |
| 4 | D0- | 29 | A5+ |
| 5 | D1+ | 30 | A5- |
| 6 | D1- | 31 | A6+ |
| 7 | D2+ | 32 | A6- |
| 8 | D2- | 33 | A7+ |
| 9 | D3+ | 34 | A7- |
| 10 | D3- | 35 | RLYSTB+ (Strobe) |
| 11 | D4+ | 36 | RLYSTB- (Strobe) |
| 12 | D4- | 37 | RLYRDB+ (Read control) |
| 13 | D5+ | 38 | RLYRDB- (Read control) |
| 14 | D5- | 39 | Spare |
| 15 | D6+ | 40 | Spare |
| 16 | D6- | 41 | RLYRST+ (Reset) |
| 17 | D7+ | 42 | RLYRST- (Reset) |
| 18 | D7- | 43 | Spare |
| 19 | A0+ | 44 | Spare |
| 20 | A0- | 45 | DIN START+ *(see note) |
| 21 | A1+ | 46 | DIN START- *(see note) |
| 22 | A1- | 47 | DIN STOP+ *(see note) |
| 23 | A2+ | 48 | DIN STOP- *(see note) |
| 24 | A2- | 49 | Ground |
| 25 | A3+ | 50 | Ground |

*Note – On daisy chain cables, these signals must be No Connect between the base Relay I/O Board and any expansion boards.

### 2.6.7 DSP Emulation Interface

Connector J19 is for a Boundary Scan type emulator pod provided on the DMS Core Measurement board to control the DSP Processor. This connector may be used for factory test and firmware development, but has no user application.

## 2.7 Power Distribution and Supply Ratings

The DMS has many different isolated power sections, each requiring high common mode noise rejection to keep measurements from being corrupted. The DMS system therefore uses an inverter on the Relay I/O Board to produce a 400 HZ (nominal) trapezoidal waveform that is

distributed to multiple transformers. Each transformer has shielded windings and a split bobbin design to minimize capacitance that would couple common mode voltage. These transformers also use laminated iron core material and traditional E-I design to minimize passing high frequency noise into each isolated power plane. The inverter output must be capable of supplying power to one Relay I/O Board and one Core Measurement Board. Expansion Relay I/O Board inverters supply only their own voltages.

The inverter is supplied by commercial switching power supplies providing +/- 12 VDC. The output of these supplies is also used directly for GP relay coils and the fused 12 VDC output provided to the user for relay driver operation. All isolated supplies provide 500V Peak isolation from earth ground and each other. Cabling may lower the isolation value on multiple pin connectors if mass terminated wiring is used.

The inverter will also power the optional High Speed Digitizer power supply if installed. This power supply has four isolated output channels for the three HS Digitizer measurement channels and one supply for the control and communication logic. The HS Digitizer communication power supply is returned to earth ground via the IEEE1394 cable and the host PC.

The +/- 12VDC supplies are rated for the standard DMS with up to one Expansion Relay I/O board, or a DMS with the optional High Speed Digitizer and no Expansion Relay I/O board. Additional switching supplies will be required for expanded systems.

DMS Isolated Power Supplies from Inverter

| Isolated Supply | Location | Description |
|---|---|---|
| Isolated 1<br>+5V | Relay I/O Board<br>Board | Control section – ground common to Core Measurement Board |
| Isolated 1<br>+5V, +/-15V | Core<br>Measurement | DSP and microcontroller power and low frequency measurement channel |
| Isolated 2<br>+5V, +/-15V | Core<br>Measurement | High frequency measurement channel |
| Isolated 3<br>+5V, +/-15V | Relay I/O Board | Power for DIN inputs 1 - 4 |
| Isolated 4<br>+5V, +/-15V | Relay I/O Board | Power for DIN inputs 5 - 8 |
| Communication<br>+5V | Core<br>Measurement | RS232 and S6000 communication interfaces, Talk, Listen, Error, Status indicators |

HS Digitizer Isolated Power Supplies from Inverter

| Isolated Supply | Location | Description |
|---|---|---|
| Channel 1-3<br>+5VA, -5VA,<br>+5VD, +3.3V | HS Digitizer<br>Power Supply | Digitizer Measurement Channels |
| Communication<br>+5V, +3.3V | HS Digitizer<br>Power Supply | Digitizer Control and IEEE1394 interface |

The requirements for the commercial switching power supplies used to power the inverter are:

| Configuration | Supply Capacity |
|---|---|
| Measurement Board + Base Relay I/O Board + 1 Expansion Relay I/O Board | 4.3 A @ +12 VDC<br>4.3 A @ -12 VDC |
| Measurement Board + Base Relay I/O Board + High Speed Digitizer | 4.3 A @ +12 VDC<br>4.3 A @ -12 VDC |
| For each additional expansion relay I/O board, add | 2.0 A @ +12 VDC (4.0A if providing another 2.0A fused output for user relays)<br>1.0 A @ -12 VDC |

Relay I/O Board Power Connections

| Pin | Characteristic | Function |
|---|---|---|
| J30-1/2 | +/- 22V RMS 400 Hz | AC inverter output high side to Core Board |
| J30-3/4 | +/- 22V RMS 400 Hz | AC inverter output low side to Core Board |
| J30-5/6 | Ground | Inverter ground common to input side shields on isolated supply transformers and 12V input supply ground. |

Core Measurement Board Power Connections

The J15 PCB connector is a 6 pin header.

The corresponding rear panel reference designator is J17.

| Pin | Characteristic | Function |
|---|---|---|
| 1&2 | +/- 22V RMS 400 Hz | AC inverter output high side to Relay Board |
| 3&4 | +/- 22V RMS 400 Hz | AC inverter output low side to Relay Board |
| 5&6 | Ground | Inverter ground – common to input side shields on isolated supply transformers and 12V input supply ground. |

Core Measurement Board Fan Power Connector

| Pin | Characteristic | Function |
|---|---|---|
| J4-1 | +12V regulated | Cooling fan supply voltage |
| J4-2 | +12V regulated ground | Cooling fan supply voltage |

## DMS System Power Connections

The J31 PCB connector is a 6 pin header.
The corresponding rear panel connector reference designator is J5.

| Pin | Characteristic | Function |
|---|---|---|
| 1,2 | + 12VDC | Inverter supply input |
| 3,4 | - 12VDC | Inverter supply input |
| 5,6 | Ground | Inverter ground – see above |

## DMS AC Present and DC Present Input Connections

The J3 PCB connector is a 10 pin header.
The corresponding rear panel connector reference designator is J15.

| Pin | Characteristic | Function |
|---|---|---|
| 1 | ACP- | AC Present optocoupler diode input cathode<br>500 Ohm series resistor |
| 2 | ACP+ | AC Present optocoupler diode input anode<br>Drive with 7 mA at 1.4V forward voltage |
| 3 | NC | Reserved for Isolation Voltage |
| 4 & 5 | +5VDC fused .5A | Available for pull-up on optocoupler inputs -<br>Common to ground on Low Frequency Mux output |
| 6 & 7 | Isolated Ground Return | Available for return on optocoupler inputs –<br>Common to ground on Low Frequency Mux output |
| 8 | NC | Reserved for Isolation Voltage |
| 9 | DCP- | DC Present optocoupler diode input cathode<br>500 Ohm series resistor |
| 10 | DCP+ | DC Present optocoupler diode input anode<br>Drive with 7 mA at 1.4V forward voltage |

## 2.8 Physical Properties

### 2.8.1 Mechanical Properties

DMS Front Panel Rack Mount Height - 7.0 Inch

DMS Expansion I/O Front Panel Rack Mount Height – 3.5 Inch

DMS Chassis

18.0 inch deep rack mount clearance for standard DMS chassis
24.0 inch deep rack mount for optional High Speed Digitizer chassis
17.0 inch width to edge of mounting ears
16.5 inch center to center hole spacing

Standard DMS Chassis weight – approximately 15 lbs

Optional High Speed Digitizer DMS Chassis weight – approximately 20 lbs

DMS Expansion I/O Chassis weight – approximately 5 lbs

### 2.8.2 Environmental Operating Requirements

Operating Temperature: 15-35°C

Operating Humidity: 20%–80% non-condensing

Air flow enters the front of the cabinet and exits through the rear and top. There should be 24" unobstructed area behind the cabinet and 18" in front. Refer to the hardware reference manuals provided with each load and source to determine specific cooling needs.

## 2.9 Specifications

### 2.9.1 Calibration Cycle

All measurement specifications are based on a twelve month calibration cycle.

### 2.9.2 Multiplexer

Number of relays: 32 DPST configured as 16 X 2 to support measurement and timing operations.

One channel bandwidth -3db at 100 MHz, second channel -3db at 10 MHz.

Isolation: Both channels isolated ±500V Peak from each other and earth ground.

Rating: 100mA, ±500V Peak, channels fused at 500mA.

### 2.9.3 General purpose relays

Number of relays: 8 DPDT

Rating: 5A, 30VDC/120VAC/240VAC, 1/3 HP @ 120VAC, ½ HP @ 240VAC

Relay Drivers: 16 capable of sinking 500 mA from 48 VDC. 2A maximum with standard supply (other voltages and supplies available). All outputs share a common return.

### 2.9.4 Digital outputs

Number of outputs: 16 (8 common + 8 isolated), Open Collector, individual optical isolation, no pull-up resistor provided.

Rating: 100mA, 70VDC, 0.5W

### 2.9.5 Digital inputs – Standard DMS

DIN organization: Two groups of four comparators, each group with a common programmable level. Groups are isolated from each other, all eight are isolated from ground to +/- 500V.

Input voltage range: -10V to 10V

Input impedance: 100 KOhm, 30pF

Accuracy: DIN 1 – 8: 1%, DIN > 8 (I/O Expansion units): 2.5%

Resolution: 0.02% FS

The Digital Inputs of the Optional High Speed Digitizer are described in TBD.

### 2.9.6 AC Source Inputs

The DMS provides a dedicated Low Frequency MUX input internal connection for a system AC source. This can be used with two additional User MUX input connections and three Internal MUX connections to measure up to three phases of voltage and three phases of current. Using this feature with emPower software adds the full range of DMS measurements to any AC source.

Input voltage range: Voltage – same as VRMS; Current +/- 5V Peak Input

Input impedance: Voltage same as VRMS; Current 20 KOHM Differential Input

Accuracy: Voltage - same as ACRMS; Current - .01% + .03% FS + external shunt error

Resolution: 0.002% FS

### 2.9.7 Measurements taken from User MUX

#### 2.9.7.1 VDC – 10 Ms Measurement Aperture Time

| Range | Resolution | Input Resistance | Accuracy @ Aperture |
|---|---|---|---|
| ±2V | 0.003% FS | 1MOHM | ±0.1% Rdg + ±0.1% FS @ 10 Ms<br>±0.01% Rdg + ±0.01% FS @ 100 Ms |
| ±20V | 0.003% FS | 1MOHM | ±0.1% Rdg + ±0.1% FS @ 1 Ms<br>±0.01% Rdg + ±0.01% FS @ 10 Ms |
| ±200V | 0.003% FS | 1MOHM | ±0.1% Rdg + ±0.1% FS @ 1 Ms<br>±0.01% Rdg + ±0.01% FS @ 10 Ms |
| ±500V | 0.003% FS | 1MOHM | ±0.1% Rdg + ±0.1% FS @ 1 Ms<br>±0.01% Rdg + ±0.01% FS @ 10 Ms |

#### 2.9.7.2 VRMS / VAVG (Operating frequency from 45Hz to 440Hz, AC+DC < 500 V)

| Range | Resolution | Input Resistance | Accuracy |
|---|---|---|---|
| 0 to 14V | 0.004% FS | 1MOHM /100pF | ±0.1% Rdg + ±0.065% FS +<br>±.05% FS per 100Hz above 100Hz |
| 0 to 140V | 0.004% FS | 1MOHM /100pF | ±0.1% Rdg + ±0.065% FS +<br>±.05% FS per 100Hz above 100Hz |
| 0 to 350V | 0.004% FS | 1MOHM /100pF | ±0.1% Rdg + ±0.065% FS +<br>±.05% FS per 100Hz above 100Hz |
| | | | |

### 2.9.8 Measurements taken from Internal MUX

These voltages are scaled by conversion factors to represent AC or DC current. Any external shunt accuracy should be considered in final current reading accuracy. This input must be driven by a fairly low impedance source, such as a shunt amplifier or current monitor signal.

#### 2.9.8.1 VDC – 10Ms Measurement Aperture Time

| Range | Resolution | Input Resistance | Accuracy |
|---|---|---|---|
| 0 to ±5V | 0.003% FS | 20 KOHM differential | ±0.01% Rdg + ±0.03% FS |

#### 2.9.8.2 VRMS

| Range | Resolution | Input Resistance | Accuracy |
|---|---|---|---|
| 0 to ±5V Peak<br>3.5 VRMS<br>For crest factor = 1 | 0.003% FS | 20 KOHM differential | ±0.01% Rdg + ±0.065% FS |

### 2.9.9 Power

#### 2.9.9.1 DC Power

Full scale current value is taken from the rating of the current sense element (shunt, Hall effect sensor, etc.)

Accuracy = User Mux VDC Error + Internal Mux VDC Error + Current Sense Error

#### 2.9.9.2 AC Power

Full scale current value is taken from the rating of the current sense element (shunt, current transformer, etc.)

Accuracy = User Mux VRMS Error + Internal Mux VRMS Error + Current Sense Error

#### 2.9.9.3 Peak-to-peak Noise with standard Peak Noise Detector

Peak-to-peak noise measurement bandwidth: 5 KHz to 100 MHz with programmable 3dB single-pole roll-off filters at either 20 MHz or 50 MHz.

Peak to peak noise accuracy for the optional High Speed Digitizer is described in section TBD.

| Range | Resolution | Input Resistance | Accuracy |
|---|---|---|---|
| +/- 100mV | 0.02% FS | 50 OHM @ 1MHZ | ±1.0% Rdg + ±0.1% FS |
| +/- 500mV | 0.02% FS | 50 OHM @ 1MHZ | ±1.0% Rdg + ±0.1% FS |
| +/- 5.0 V | 0.02% FS | 50 OHM @ 1MHZ | ±1.0% Rdg + ±0.1% FS |

#### 2.9.9.4 AC RMS Noise

AC RMS noise measurement bandwidth: 10 Hz to 1 MHz

Voltage Range: 0 to 70 mVRMS, 350 mVRMS, and 3.5 VRMS with crest factor < 2.5

| Range | Resolution | Input Resistance | Accuracy |
|---|---|---|---|
| 70 mVRMS | 0.012 % FS | 10 KOHM @ 100KHZ | ±1.0% Rdg + ±0.14% FS |
| 350 mVRMS | 0.012 % FS | 10 KOHM @ 100KHZ | ±1.0% Rdg + ±0.14% FS |
| 3.5 VRMS | 0.012 % FS | 10 KOHM @ 100KHZ | ±1.0% Rdg + ±0.14% FS |

#### 2.9.9.5 Timing

Types of timing measurements: Start to Stop in either Averaged or Single Shot mode. Applications include; rise time, fall time, transfer time, pulse width, and other general timing from any trigger source, (as defined below) to any trigger source. The start and stop trigger can be from the same or different sources.

Trigger input: Input On/Off signals (from AC or DC sources), voltage signals of any MUX input, and voltage signal of any DIN.

Counter resolution: 32 bit counter running at 5 MHz provides 100 nS resolution up to seven minutes

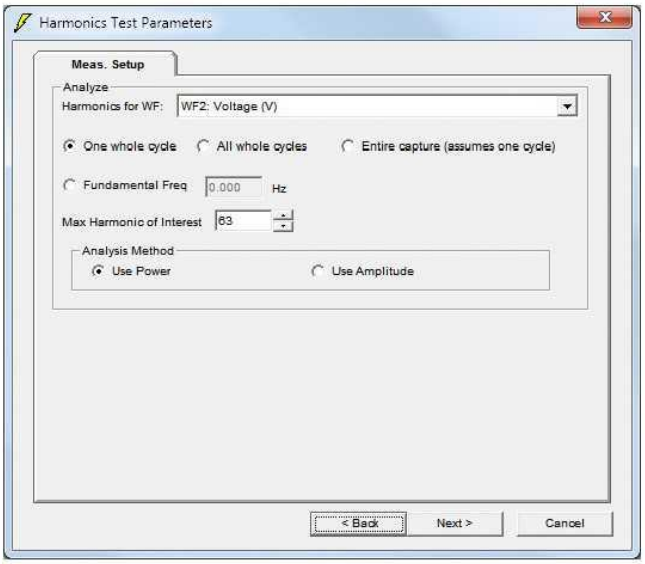
Accuracy: 0.02% ±200 nS from DIN inputs, 0.2% ±200 nS from MUX inputs.

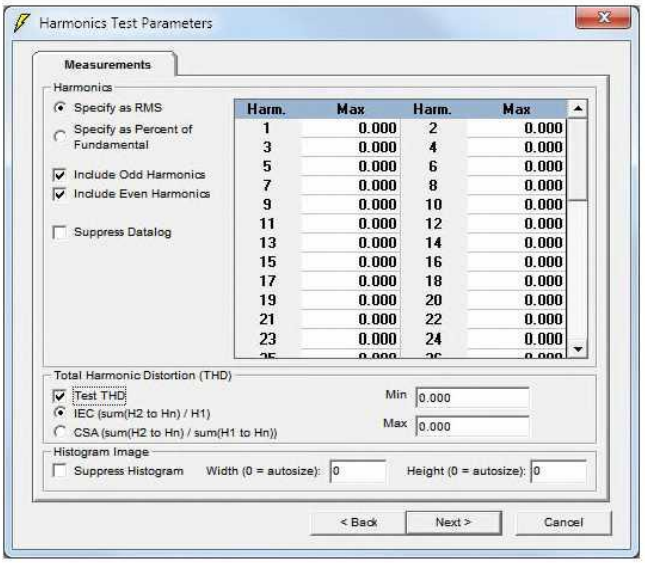
### 2.9.9.6 Harmonics

**Total Harmonics Distortion(THD) is analyzed by one of two methods:**

1) **Power**
2) **Amplitude**

**THD Accuracy: 1% Rdg**



## Overview

NHR harmonics analysis uses the National Instruments Measurement Studio math library for analysis of waveform harmonics. The basic flow is:

1. Create a data set from the raw samples that has an even power of two number of samples containing exactly one cycle, all whole cycles, or all raw samples as specified by the user.
2. Determine individual harmonics based on Power Spectrum or Amplitude Spectrum (see below).
3. Calculate THD based on desired computation method (note, the terminology "IEC" and "CSA" is incorrect) however the two methods used are described in detail below.

## Analysis Method: Use Power

nierr = NI::CNiMath::AutoPowerSpectrum(nivectorData, nivectorHarmonics, df, dt);

Calculates the single-sided, scaled auto power spectrum of a time-domain signal. The auto power spectrum is defined as shown in the following figure:

$$\frac{FFT(X)\ FFT^{*}(X)}{n^{2}}$$

where numberOfElements is the number of points in the signal array X

* denotes a complex conjugate

Output is Single-sided power spectrum in volts rms squared, if the input signal is in volts. If the input signal is not in volts, the results are in input signal units rms squared.

AutoPowerSpectrum converts the auto power spectrum to a single-sided form.

## Analysis Method: Use Amplitude

nierr = NI::CNiMath::AmpPhaseSpectrum(nivectorData, nivectorHarmonics, phaseSpectrum, df, true, dt);

Calculates the single-sided, scaled amplitude and phase spectra of a time-domain signal, X. AmpPhaseSpectrum calculates the amplitude spectrum as

$$\left|\frac{FFT(X)}{n}\right|$$

and converts it to single-sided form.

Output is single-sided amplitude spectrum magnitude in volts, root-mean-square, if the input signal is in volts. If the input signal is not in volts, the results are in input signal units, root-mean-square.

## Calculate THD: "IEC" Method

THD as a % of the fundamental. This method can result in values > 100%.

Using the output of the analysis shown above, calculate as:

$$THD = \frac{\sqrt{V_{RMS,2}^2 + V_{RMS,3}^2 + \cdots + V_{RMS,n}^2}}{V_{RMS,1}} * 100$$

## Calculate THD: "CSA" Method

THD as a % of the total RMS. This method results in values <= 100%.

Using the output of the analysis shown above, calculate as:

$$THD = \frac{\sqrt{V_{RMS,2}^2 + V_{RMS,3}^2 + \cdots + V_{RMS,n}^2}}{V_{RMS,total}} * 100$$

#### 2.9.9.7 Frequency measurement – AC Line Voltage

Range: 10 Hz to 500 Hz

Accuracy: 0.016% Rdg.

Resolution: 1/100 nS

### 2.9.10 Waveform and Transient Measurements – Standard DMS

Waveform measurement specifications for the optional High Speed Digitizer are in section 2.10.

#### 2.9.10.1 Isolation:

±500 VDC from earth ground.

#### 2.9.10.2 Sample Resolution and Accuracy

Low Frequency path; 16 bits vertical resolution, ±0.025% of range ±0.025% reading

High Frequency path; 14 bits vertical resolution, ±0.1% of range ±0.1% reading

DC Coupled Ranges: +/- 20, 200, 500 VDC

AC Coupled Ranges: +/- 0.2, 1, 10 V Pk-Pk

Bandwidth DC Coupled: DC-100MHz single channel, DC-10 MHz dual channel

Bandwidth AC Coupled: 10 Hz to 10 MHz

Maximum Sampling Rate: 125 KSPS single channel, 100 KSPS dual channel

#### 2.9.10.3 Trigger Control

Trigger input from User MUX inputs, Selected Digital Input, AC Present, DC Present, Trigger In connector.

Trigger delay resolution: 200 nS

#### 2.9.10.4 Capture Modes

Sample Mode – sample at maximum rate, save only last sample if effective sample rate reduced.

## 2.10 High Speed Digitizer Option

### 2.10.1 Introduction

The High Speed Digitizer option for the NH Digital Measurement System provides three eight bit digitizing channels isolated from ground and each other. In addition, it provides 16 channels of digital signal input referenced to one of the channel grounds.

The HS Digitizer is implemented as a large PC Board with the FPGA, memory, and digital control, and a small analog input conditioning piggyback PCB per channel. The HS Digitizer assembly can perform functions that required dedicated circuitry in the Digital Measurement System, such as the peak noise measurement and high frequency RMS noise measurement. The HS Digitizer can be installed as an option in the DMS chassis and replace dedicated hardware to perform these functions. The DMS with HS Digitizer installed uses a larger chassis than the original DMS, and requires a separate power supply PCB.

This manual also covers connector pinouts and operation of the power supply PCB. The HS Digitizer communicates with the PC over an IEEE1394 serial bus, it does not use the NH S6000 family interface or protocol. When integrated with the DMS, two of the three channels are connected through the sixteen to two multiplexer, and that device will require control using the standard NH6000 serial protocol. The Digital Measurement System emPower driver will incorporate HS Digitizer and multiplexer control to provide the waveform measurement functions.

### 2.10.2 HS Digitizer PCB Configuration

#### 2.10.2.1 I/O Interfaces

**IEEE 1394 Interface Connector – J16**

Connector Type - 6 Pin IEEE1394
Mating Cable - Assmann AK1394-30

This connector implements the industry standard IEEE1394 interface. This port will connect directly to a PC port using a standard IEEE1394 cable. This connector is isolated from all measurement channels, and has it's shield and ground pins tied to tester and host computer chassis ground.

| Pin | Signal | Function |
|---|---|---|
| 1 | Power | Provide power to simple devices - not used on HS Digitizer |
| 2 | GND | Ground return for power |
| 3 | TPB* | Negative side of twisted pair B |
| 4 | TPB | Positive side of twisted pair B |
| 5 | TPA* | Negative side of twisted pair A |
| 6 | TPA | Positive side of twisted pair A |
| - | Shield | Carries bias voltage |

**Power Input Connectors – J1, J5, J9, and J14**

Connector Type - 1X8 headers, 0.156 in spacing (J1,J5,J9)
Mating connector - NH 6300080 (MOLEX 09-50-3081)
Connector Type - 1X6 headers, 0.156 in spacing (14)
Mating connector - NH 6300074 (MOLEX 09-50-3061)

These connectors bring the isolated voltage supplies for each channel into the PCB. They all have identical pinouts that match the source connector on the Power Supply PCB. Each channel is isolated from ground and other channels to 500 V Peak. Suitable wiring should be used in any cabling to these connectors to maintain this isolation.

J1, J5, J9 Pinout

| Pin | Signal | Function | Power Required |
|---|---|---|---|
| 1 | AGND | Analog ground | Return for +5VA,-5VA) |
| 2 | +5VA | Analog positive 5 volts | 0.4 A |
| 3 | -5VA | Analog negative 5 volts | 0.25 A |
| 4 | +5V | Digital positive 5 volts | 0.180 A (DIN channel) |
| 5 | +3_3V | Digital positive 3.3 volts | 0.42 A |
| 6 | +3_3V | 3.3 volts redundant | |
| 7 | GND | Digital ground | Return for 5, 3.3V |
| 8 | GND | Digital ground redundant | |

J14 Pinout

| Pin | Signal | Function | Power Required |
|---|---|---|---|
| 1 | GND | Chassis Ground | Return for 3.3V, 5V |
| 2 | +5V | 5V Not Isolated | 0.7 A |
| 3 | +3_3V | 3.3V Not Isolated | 0.2 A |
| 4 | +5V | 5V Not Isolated redundant | |
| 5 | GND | Chassis Ground | |
| 6 | +3_3V | 3.3V Not Isolated redundant | |

**FPGA Download Configuration Connector - J4, J8, J12, and J15**

Connector Type - 10 pin .025 square pin header – 2X5
Mating Connector - supplied by Xilinx

These connectors are used only for development and are not normally used in system operation. They provide a path for downloading configuration information into the RAM based FPGA devices via a PC cable during development. During normal operation, this download is performed by the 8032 microcontroller, so the connectors are not used.

| Pin | Signal | Function | Pin | Signal | Function |
|---|---|---|---|---|---|
| 1 | TCLK1 | JTAG Port clock | 6 | TDI | JTAG Port Data In |
| 2 | - | | 7 | TDO | JTAG Port Data Out |
| 3 | GND | FPGA ground | 8 | TMS | JTAG Port Strobe |
| 4 | - | | 9 | CHINIT | FPGA initialize pin |
| 5 | 2.5V | FPGA power | 10 | CBLPROG | FPGA programming pin |

**Analog Module Board-Stack Connectors – J2, J6, and J10**

Connector Type – Single Row 20 Pin Header 0.3" spacing, NH 6301739

This connector passes power and range control signals up to the Analog Module, and carries the differential analog signal to be digitized down to the A/D inputs on the HS Digitizer base board.

| Pin | Signal | Function | Note |
|---|---|---|---|
| 1 | VIN- | Inverted side of differential analog input | +/- .756V Max |
| 2 | VIN+ | Non-inverted side of differential analog input | +/- .756V Max |
| 3 | N/C | | |
| 4 | N/C | | |
| 5 | TERM50 | 50 Ohm Termination Relay Control | 5V, 22 mA |
| 6 | DC_CPL | AC/DC Coupling Relay Range Control | 5V, 22 mA |
| 7 | BYPASS | Bypass to DMS Core PCB Relay Control | 5V, 35 mA |
| 8 | DIV10 | Divide by 10 Relay Control | 5V, 22 mA |
| 9 | MYEN | Connect Input to Digitizer Relay Control | 5V, 35 mA |
| 10 | DIV100 | Divide by 100 Relay Control | 5V, 22 mA |
| 11 | SEL0 | Future Use | |
| 12 | SEL1 | Future Use | |
| 13 | GAIN10 | Gain of 10 Relay Control | 5V, 22 mA |
| 14 | DCTERM50 | DC Couple 50 Ohm Termination Control | 5V, 22 mA |
| 15 | BW20M | 20 MHz BW roll-off Filter Relay Control | 5V, 22 mA |
| 16 | OVLD | 50 Ohm Termination Resistor Overload Flag | 5V, 22 mA |
| 17 | GNDA | Analog Ground | |
| 18 | GNDA | Analog Ground redundant | |
| 19 | -5VA | +5V Analog Supply | 5V, 0.4A |
| 20 | +5VA | -5V Analog Supply | 5V, 0.25A |

**Analog Module Input Connector – J1 and J2**

The input connector is rated for 500 V Peak input and has a frequency bandwidth from DC to 200 MHz. Mating cable and connectors should have a 50 Ohm characteristic impedance. The input circuit is expected to carry less than 100 mA. All channel inputs are isolated from other channels and ground to 500 V Peak. Input Connector receives signal from DMS MUX board, Output Connector passes signal down to DMS Core PCB.

Connector Type – SMB 50 Ohm
Mating Connector – Right Angle SMB - NH 6000278 (EF Johnson 131-1403-116)

**Digital Input Connector - J13**

Connector Type - 2X17 header with latches, 0.1 in. spacing
Mating Connector - NH 6150603 (3M 3431-2302)

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | Din input 1 | 2 | Channel 3 Ground | 19 | Din input 10 | 20 | Channel 3 Ground |
| 3 | Din input 2 | 4 | Channel 3 Ground | 21 | Din input 11 | 22 | Channel 3 Ground |
| 5 | Din input 3 | 6 | Channel 3 Ground | 23 | Din input 12 | 24 | Channel 3 Ground |
| 7 | Din input 4 | 8 | Channel 3 Ground | 25 | Din input 13 | 26 | Channel 3 Ground |
| 9 | Din input 5 | 10 | Channel 3 Ground | 27 | Din input 14 | 28 | Channel 3 Ground |
| 11 | Din input 6 | 12 | Channel 3 Ground | 29 | Din input 15 | 30 | Channel 3 Ground |
| 13 | Din input 7 | 14 | Channel 3 Ground | 31 | Din input 16 | 32 | Channel 3 Ground |
| 15 | Din input 8 | 16 | Channel 3 Ground | 33 | Channel 3 Ground | 34 | Channel 3 Ground |
| 17 | Din input 9 | 18 | Channel 3 Ground | | | | |

This cable has every other pin grounded and is connected to the user interface with twisted pair ribbon cable. The Digital Inputs share a common ground with measurement channel 3, but are isolated from the other two channels and ground to 500 V Peak. All individual DIN inputs share a common ground. Socketed resistor packs on the DIN inputs allow for termination with 22k Ohm pull up resistors to +5V.

There are socketed series input resistor packs (100 Ohm standard) allow inputs to tolerate voltages from 7 V to –2 V. The 74VHC244 receivers have clamping diodes to high and low power rails rated at 20 mA. Input thresholds are standard LVCMOS, 1.5V Maximum for low and 3.5V Minimum for high.

**Trigger Input Connector – J19**

This connector is ground referenced and accepts a TTL level signal. It has a 2.2K pull up to a ground referenced 5 VDC supply, and a 100 Ohm series input resistor with diode clamping. This signal is meant to connect to the DMS Core PCB "Trigger Output" connector so the HS Digitizer has access to all system triggers.

Input Level: Vih = 2.0 V, Vil = 0.8 V, input current from 0- 5 VDC = 10 uA
Connector Type – SMB 50 Ohm
Mating Connector – Right Angle SMB - NH 6000278 (EF Johnson 131-1403-116)

**Trigger Output Connector – J18**

This connector can output a TTL level signal that transitions on a trigger condition detected by the FPGA. The FPGA can compare samples to programmed values in real time and send the trigger when a level or edge is detected. The trigger status can also be read via the 1394 interface by software.

Output Level: Voh @ 3.2 mA = 2.8 V, Vol @ 16 mA = 0.4 V
Connector Type – SMB 50 Ohm
Mating Connector – Right Angle SMB - NH 6000278 (EF Johnson 131-1403-116)

### 2.10.2.2 Jumpers

**Watch Dog Timer Enable - JMP 7**

When this jumper is installed, there must be a write to the Watch Dog Timer Address by the 8032 firmware every 1.6 seconds to avoid a hardware reset. When the jumper is removed, only power up will initiate a hardware reset. Presently no jumper is installed.

**Configuration Jumpers – JMP4, JMP5, JMP6**

Hardware configuration jumpers readable by the 8032 as part of its hardware status byte. The following table describes the jumper correspondence to the Status Byte. All jumpers read 0 when installed and 1 when removed.

| Jumper Number | Status Byte Bit | Result if installed |
|---|---|---|
| JMP4 | 0 | Inhibit 8032 from configuring FPGAs – allows emulator pod config. |
| JMP5 | 1 | Force 8032 continued operation from EPROM after start up |
| JMP6 | 2 | Not presently used |

**FPGA Configuration Load Mode Jumpers JMP1 – JMP3**

When downloading the FPGA configuration from the Xilinx JTAG cable, the Boundary Scan with Pull Up (Mode 5) is used. The jumper must be installed to select this mode. When downloading from the 8032, the Serial Slave Mode with Pull Up (Mode 7) is used, and the jumper must be removed.

| Jumpers In | Mode | Configuration Option | Jumper Position |
|---|---|---|---|
| JMP1-JMP3 | 5 – Cable Download | Boundary Scan w/Pull Up | In |
| JMP1-JMP3 | 7 – 8032 Download | Serial Slave w/Pull Up | Out |

### FPGA Programming Jumper J3, J7, J11, J17

This jumper is used only during development for download to the FPGA. It determines whether the PROGRAM signal to the FPGA is driven by the JTAG cable or the 8032. A power up resets the program state and prepares the FPGA for configuration download. The normal Digitizer configuration process relies on power up reset, so no jumpers are installed to enable the Program signal. This helps keep the FPGA from being put into a re-configuration state due to transients on the Program signal.

Channel 1 Jumper = J3, Channel 2 Jumper = J7, Channel 3 Jumper = J11, J17

| Jumper Position | Function |
|---|---|
| Pin1 - Pin2 | Cable downloads configuration (development) |
| No Jumpers | 8032 downloads configuration (normal) |

## 2.10.3 Digitizer Power Supply PCB Configuration

### 2.10.3.1 I/O Interfaces

### Channel Power Output Connectors - J1, J2, J3, and J4

These connect to the HS Digitizer power input connectors. They have the same pinout as those connectors (see 34041344.0.1073774592.24) so that one to one cables can be used. The inter-board connections are:

| Power Board Connector | HS Digitizer Connector |
|---|---|
| J1 | J1 |
| J2 | J5 |
| J3 | J9 |
| J4 | J14 |

Due to the low voltages in use, gold plated connectors must be used for the power connector pin headers as well as the crimp terminals in the channel power connectors.

### AC Power Input Connector - J5

This input takes in the 400 Hz trapezoidal sine wave input produced on the DMS Relay I/O PCB. This AC voltage passes through the isolating transformers and is rectified for each channel. The connector pinout matches J30 on the Relay PCB so one to one cabling can be used. The connector pins are:

| Pin | Signal | Function |
|---|---|---|
| 1 | AC1 | AC input high side |
| 2 | AC1 | AC input high side |
| 3 | AC2 | AC input low side |
| 4 | AC2 | AC input low side |

| | | |
|---|---|---|
| 5 | Earth | AC voltage return |
| 6 | Earth | AC voltage return |

Due to the low voltages in use, gold plated connectors must be used for the power connector pin headers as well as the crimp terminals in the channel power connectors.

### 2.10.4 Digitizer programmble setup and configuration

#### 2.10.4.1 Factory Configuration Options

Some options stored in the Digitizer FLASH memory are read by the 80c320 and used to set up FPGA configuration registers. Some data stored in FLASH is just used by NH for field diagnostic information. Information like build date, serial number, and part number are not used by the operational firmware, but may be retrieved for troubleshooting purposes. The Memory field MUST be filled with a value corresponding to the type of SRAM devices installed for proper operation. The calibration program includes a utility to save and retrieve these values.

| Memory Device Installed | Memory Per Channel | Memory Configuration Value |
|---|---|---|
| 0.5 MWord | 4 Mbyte | 0x0400000 |
| 1 MWord | 8 Mbyte | 0x0800000 |
| 2 MWord | 16 Mbyte | 0x1000000 |
| 4 MWord | 32 Mbyte | 0x2000000 |

### 2.10.5 Specifications

#### 2.10.5.1 Physical Specifications

One PCB with piggyback connectors for three analog modules. A separate power supply PCB with four isolated output groups is required to power three digitizer channels and the 1394 interface. The power supply PCB requires a 22 VAC 400 Hz input.

**Size & Weight**

Size: Base PCB approximately 15.0 x 17.5 inches. Weight: Approximately 2.5 lbs.

Size: power Supply PCB approximately 3.5 x 15.0 inches. Weight: Approximately 1.5 lbs.

Size: Analog Module (with shield) approximately 3.5 x 4.5 inches. Weight Approximately 0.36 lbs.

**Communication**

Communicates with PC using IEEE1394 interface. Serial data in SBP-2 protocol, NH proprietary command values defined in NH Document 08-0392 - High Speed Digitizer S/W Specification.

### Control

An emPower 1394 SBP-2 driver is used to control the digitizer in a system. The digitizer is controlled separately from the MUX, which is controlled via the existing DMS RS232/RS422 interface.

### Isolation

Waveform channels - 500 V Peak isolation from any channel to earth ground or another channel.

Digital Inputs - All 16 inputs share a common ground with each other and Waveform Channel 3. That ground has 500 V Peak isolation to earth ground.

### Calibration

Calibration factors for the three installed Analog Modules are stored in FLASH memory on the HS Digitizer base PCB. The host computer downloads these at power up and performs all calibration calculations.

### Self-test

Power-up self test is implemented in 8032 firmware. Self test will perform simple memory tests, and some communication and logic tests.

### Temperature

Operating from 10 to 50°C. Specifications apply at 20-40°C after 10-minute warm-up

### Power Source

400 Hz 22 V Pk-Pk voltage supplied by DMS Relay PCB.

Estimated requirement for inverter input: 0.6A @ 12VDC, 0.6A @ -12VDC

### Processor

Intel 8032 family processor will be used to initialize and control specialized interface ICs and the FPGA.

### 2.10.5.2 Performance Specifications

| | | |
|---|---|---|
| Channels | Three Analog, Sixteen Digital | |
| Resolution | 8 Bit | |
| Sample Rate | 200 MSPS Maximum | |
| Input Coupling | AC or DC on all channels.<br>AC Coupling low frequency corner at 7.2 Hz | |
| DC Accuracy | 1.5% Reading + 1% Range | |
| AC Accuracy – DC Coupled or AC Coupled High Impedance | 1.5% Reading + 1% Range @ 50 KHz | |
| AC Accuracy –<br>50 Ohm AC Coupled | 1.5% Reading + 1% Range @ 2 MHz | |
| Hardware Ranges; +/- V Peak | 0.05, 0.125, 0.25, 0.5, 1.25, 2.5, 5, 12.5, 25, 50 | |
| Input Impedance | 1 MOhm 1%<br>50 Ohm AC termination: 2% > 1.4 MHz (141 KHz corner) | |
| Bandwidth Control | 100 MHz 3 pole Roll off - default (-60db/decade)<br>20 MHz 3 pole Roll off - selectable per channel | |
| Bandwidth Flatness 1db | Ranges 5V and below: | Channels 1,3: 50 KHz - 50 MHz<br>Channel 2: 50 KHz -10 MHz |
| | Ranges above 5V: | Channels 1,3: 50 KHz -20 MHz<br>Channel 2: 50 KHz - 2 MHz |
| Bandwidth 3db down<br>(100 MHz Roll off default) | Ranges 5V and below: | Channels 1,3: 150 MHz<br>Channel 2: 20 MHz |
| | Ranges above 5V: | Channels 1,3: 40 MHz<br>Channel 2: 20 MHz |
| 20 MHz Roll off filter<br>Attenuation at 40 MHz (octave) | Ranges 5V and below: | Channels 1-3: -18 db |
| | Ranges above 5V: | Channels 1,3: -9 db<br>Channel 2: -15 db |
| Voltage Protection | High impedance: 500 V Peak input non-destructive<br>50 Ohm termination: 1 Watt limit – See Power Limit Curve | |
| Isolation | All channels individually isolated 500 V Peak to Earth ground | |
| Input Capacitance | 60 pF Maximum | |
| Digital Inputs | Sixteen at 100 MSPS<br>Common ground to Channel 3, Fixed Level: 3.3VIH, 1.5 VIL<br>22 KOhm Pullup to 5V, 100 Ohm in series<br>20 mA current clamp limit to +5V and ground | |
| Memory Capacity | 8 MByte per Channel, two 8 bit samples per 16 bit location. | |
| CMRR | > 40db: DC-20 MHz<br>>35 db: 20-100MHz | |

| | |
|---|---|
| Trigger Position Accuracy<br>*See Note 1 | Channels 1 & 2 Relative to Each Other, DIN, and System:<br>+/- {4 X (1/Sampling Rate)}<br>Channel 3 Relative to Channels 1 & 2, DIN, and System:<br>+/- {6 X (1/Sampling Rate)} |
| Trigger Level Accuracy | Any Waveform Channel – Rising or Falling Edge;<br>Same as channel accuracy above<br>Digital Input Pattern – False-Then-True Match<br>DIN threshold range 1.5 – 3.5V (LVCMOS)<br>System Trigger Input – Falling Edge<br>Receiver threshold range 1.5 – 3.5V (LVCMOS) |
| Trigger Coupling Sensitivity | DC – Hysteresis is 1.5% of full range<br>Noise Rejection – Hysteresis is 5.5% of full range<br>High Frequency Reject –<br>Pulse > 2.5 uS at 200 MSPS or Pulse > 5us @ 100 MSPS<br>High Frequency and Noise Reject –<br>Trigger Arm Hysteresis 5.5% of full range and<br>Pulse > 2.5 uS at 200 MSPS or Pulse > 5us @ 100 MSPS |
| Capture Mode Memory Usage | Sample – Saves last two values at end of sampling period<br>Peak – Saves highest and lowest values found during sampling period in the order they occurred<br>High Resolution – samples at highest possible rate using all available installed memory and averages multiple samples for each display point<br>Fixed Average – similar to High Resolution with the number of averaged samples fixed at 10 maximum. |
| FPGA real time functions<br>(200 MSPS Maximum) | Peak Detect, Threshold compare, Trigger position delay count, SRAM Memory control |
| 8032 Microcontroller functions | Initialization of FPGA and IEEE1394 chip set |
| Communication | SBP-2 Protocol Implementation with IEEE1394 chip set at 200 Mbps |
| Host PC Processing | Raw data calibration and Waveform Measurements as described in NH Research document 09-0253 |

Note 1:

Trigger time accuracy at system UUT interface – does not include fixture wiring.
1/Sampling Rate = Sampling Period.
Sampling Period x 2 = Memory Address Counter Resolution
Channel to Channel Quantization Error = +/-2 Memory Address Counts
Channel 1 & 2 relative to Channel 3 (non-multiplexed) skew = +/- 1 Memory Address Count

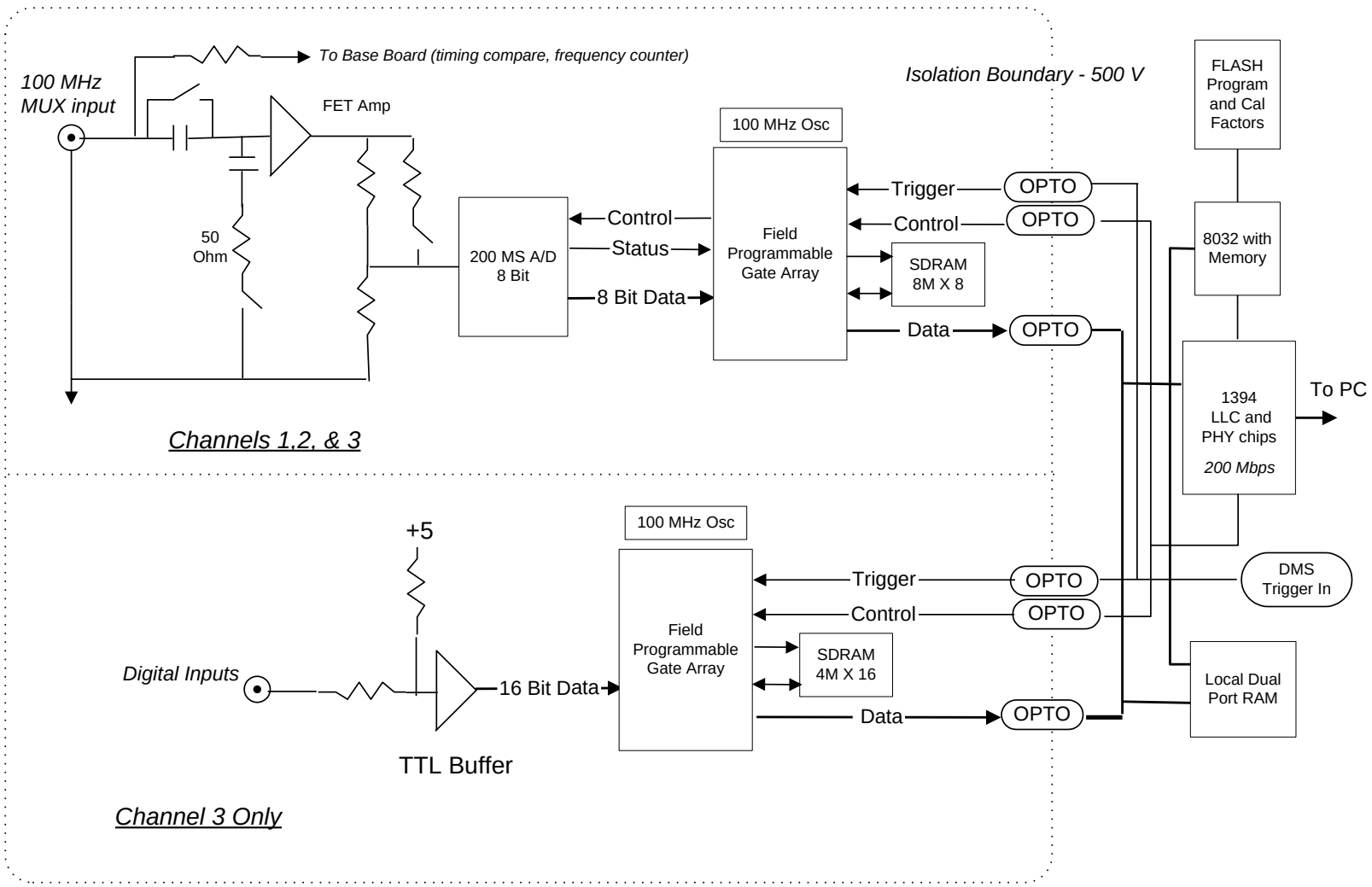
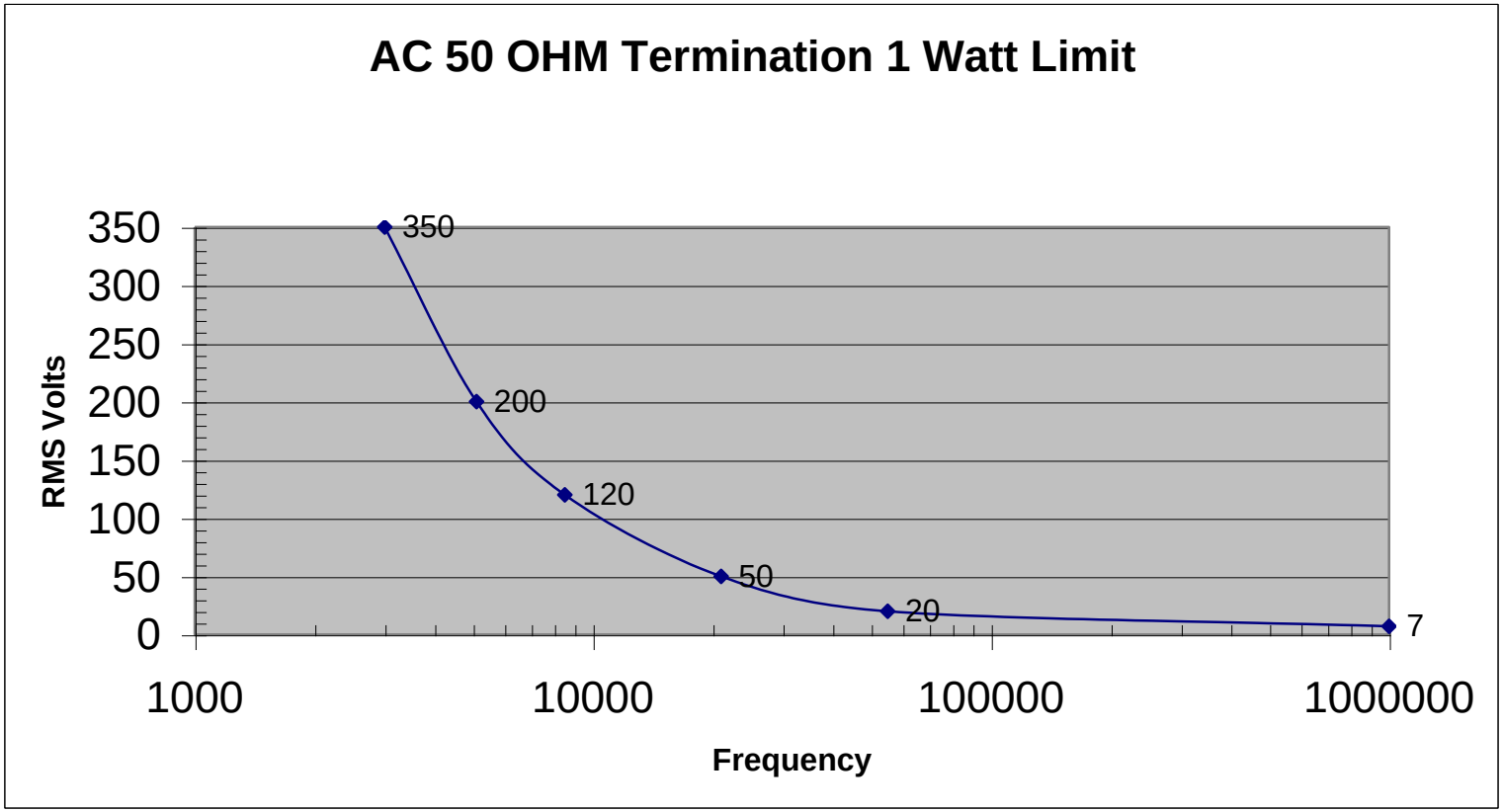



**Figure 3 - HS Digitizer Block Diagram**

**Appendix A**


AC 50 OHM Termination 1 Watt Limit
RMS Volts
350
300
250
200
150
100
50
0
350
200
120
50
20
7
1000
10000
100000
1000000
Frequency